2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS 2019)

Dallas, Texas, USA
4-7 August 2019

Pages 1-597

IEEE Catalog Number: CFP19MID-POD
ISBN: 978-1-7281-2789-7

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IEEE Catalog Number:	CFP19MID-POD
ISBN (Print-On-Demand):	978-1-7281-2789-7
ISBN (Online):	978-1-7281-2788-0
ISSN:	1548-3746

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Session A1L-B: Analog Building Blocks

Chair: Aydin Karsilayan, *Texas A&M University*
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Location: Preston Trail I & II

A current mirror based low voltage single supply CMOS level up–shifter (fcm–ls) for upconverting signals from 0.4 to 0.8V power supply domain is presented in this work. Based on the post–layout simulation, fcm–ls provides 48.5% lower energy consumption and 29.7% better speed than a similar circuit topology (vl–ls). Both circuits are evaluated on UMC 65nm CMOS process and low threshold voltage transistors. Using a power supply of 0.8V, and an input voltage range of 0.4V, we obtain up to 63.4% energy–delay–product (EDP) improvement at 500MHz frequency, at 590fF output loading, over reference circuit. Active area is optimized to achieve low static and dynamic energy consumption at the maximum load capacitance. The limits of proposed circuit are verified using the post–layout simulation results.

For spaceborne sensors power-efficient and lightweight circuitry is required, therefore, integrated solutions are preferred. In this paper an integrated current source is presented that can be used in the front-end of a fluxgate- magnetometer. A "radiation aware" design paradigm was followed to account for parameter shifts due to ionizing radiation and allow for radiation hardening without changing the topology. The digital current source achieves a dynamic range of more than 19 bits. It is based on a Delta-Sigma modulator with a digital pulse-width modulator as a quantizer. The digital-to- analog conversion is performed using a current-steering cell that employs chopping to minimize flicker noise. A fully-differential amplifier is used to drive an improved Howland current source.

Session A1L-C: Low Power and Power Management Circuits

Chair: Ayman Fayed, *Ohio State University*
Time: Monday, August 5, 2019, 8:00 - 9:30
Location: Mesquite I

A two-stage hybrid power management unit (PMU) is presented with a highly-efficient novel ON-OFF LDO as the second stage. The proposed design targets IoT sensor nodes that require sub-microwatt power levels with regulated supply voltages. The first stage provides the initial step-down using a switched-capacitor based DC-DC converter with the power efficiency of >97% at sub-microwatt levels. The output voltage from the first stage is then regulated using the proposed ON-OFF LDO. The LDO can regulate the output voltage with a dropout voltage of <30mV. To minimize quiescent power loss, the LDO control structure is all digital and consumes no static current. The hybrid structure achieves an aggregate peak power efficiency of 85% at a load of 0.8µW with low ripples <10mV. The control circuitry for both stages consumes static current <60nA. The design is implemented in 28-nm CMOS and occupies an active area of 0.0043mm^2.

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Session A2P-M: Image/Video Processing

Chair: *Qualcomm*
Time: Monday, August 5, 2019, 11:30 - 12:30
Location: Salon F

Four families of new matrix linear filters are established and being used for the approximation to directional derivatives. These filters are also used for representations of image energy, which, in turn, are used for representing image edges. The first three families are for approximations of first order digital directional derivatives, while the fourth family is for the approximations to the second order digital directional derivatives. Examples are demonstrated.

Mobile Crowdsourcing (MCS) photo-based is an arising field of interest and a trending topic in the domain of ubiquitous computing. It has recently drawn substantial attention of the smart cities and urban computing communities. In fact, the built-in cameras of mobile devices are becoming the most common way for visual logging techniques in our daily lives. MCS photo-based frameworks collect photos in a distributed way in which a large number of contributors upload photos whenever and wherever it is suitable. This inevitably leads to evolving picture streams which possibly contain misleading and redundant information that affects the task result. In order to overcome these issues, we develop, in this paper, a solution for selecting highly relevant data from an evolving picture stream and ensuring correct submission. Simulation results indicate that the implemented framework can effectively reduce false submissions and select a subset with high utility coverage with low redundancy ratio from the streaming data.

A face recognition system which represents each of the augmented facial images as a superposition of the dominant components in two transform domains is proposed. Each face in the spatial domain is divided into horizontal, vertical halves and diagonal format. These partitions are concatenated to generate four more faces per subject in any database used. All images are first preprocessed then compressed using two different domains. The Discrete Wavelet Transform (DWT) and the Discrete Cosine Transform (DCT). Accordingly, each face will have two feature matrices. A voting scheme is used to define ground truth identity. The performance of the proposed system is evaluated using k-fold cross validation of ORL, Yale and FERET databases. Sample results are presented. The proposed technique achieves higher recognition rates while retaining 44% savings in storage recently reported.

Session A2P-N: Digital Electronics and Trust

Chair: *Qualcomm*
Time: Monday, August 5, 2019, 11:30 - 12:30
Location: Salon F

A LMS (Least Mean Square) algorithm used as an adaptive noise canceller has been implemented on an Artix 7 FPGA (Field Programmable Gate Array) board. The FPGA is used for this research due to its advantages of real-time processing and pipelining which are not possible with other implementation boards. The purpose of implementing the LMS algorithm is to create a noise canceling device that removes noise from the input to achieve the appropriate output. Noise cancelation devices are needed for many environments and can be used to reduce the noise added to speech in airplanes, helicopters, and cars.

A Physical Unclonable Function (PUF) is often used to uniquely identify an integrated circuit by extracting its internal random differences using so-called Challenge Response Pairs (CRPs). On the other side, It has been realized that quantum computing is one of the latest technologies using reversible logic. It is observed that increasing growth of transistor density, power consumption will reach their limits in conventional technologies. In conventional Circuits, during the logic operations, bits of information is erased resulting dissipation of energy insignificant amount. Thus, if Circuits are designed so that information bits can be preserved, the power use can be reduced. We can use reversible logic technology for minimizing the power consumption, heat dissipation, increasing speed etc. In this paper, we propose the reversible logic design for an existing XOR Gate based Low- Cost Configurable RO PUF structure based on Feynman gate as a reversible logic block. A comparative analysis between classical and quantum logic function is also given on various parameters along with limitations of conventional computing. The proposed approach is implemented using VHDL on Xilinx-7 FPGA.

Session A2P-P: System Architectures and Embedded Systems I

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Session A4L-C: Power Converters

Chair: Narayan Kar, *University of Windsor*
Time: Monday, August 5, 2019, 15:30 - 17:00
Location: Mesquite I

In many of today's solid-state lighting applications, Critical Conduction Mode (CCM) Flyback PFC converter is a popular solution due to its limited component count and simple structure with respect to other SMPS topologies. As described in international standards documents (IEC/EN 61000-3-2), drivers are required to demonstrate a power factor results greater than 0.9 and lower THD for power levels above 25W. Due to non-sinusoidal input current waveform of the traditional constant-on-time control method, achieving improved PF and THD is quite difficult. In this paper, a new control method is introduced in an effort to improve power factor and total harmonic distortion of Voltage Mode CRM Flyback PFC Converter. The work proposes injection of a compensating sin(ωt) signal component in the feedback path utilizing an additional primary transformer winding to linearize the current from the source. The detailed theoretical analysis is presented along with measurement results of a 30W high-power system prototype.

Interleaved topologies are popular in high-power high-current applications due to the reduction in device current stresses and filter sizes. Despite its popularity, a proper design procedure for bidirectional interleaved dc-dc converter operating in CCM including the selection of appropriate number of phases and passive component design to optimize converter efficiency is missing in the literature. This paper presents a comprehensive design procedure for a bidirectional interleaved buck/boost dc-dc converters for high-current applications. Use of silicon carbide devices in the converter will further improve its efficiency and power density.

This paper provides small-signal analysis of a pulse width modulated (PWM) tapped-inductor buck dc-dc converter with complex load running in continuous conduction mode (CCM). Circuit averaging technique is used to obtain its small-signal model. The obtained model is then used to obtain duty cycle-to-output voltage and input-to-output voltage transfer functions. The equations representing the exact effect of the complex load these transfer functions have been derived. The obtained theoretical results are validated through circuit simulations.

This paper documents the requirements, modeling, design and testing of a 400kW 1kV full-bridge water-cooled power electronics building block for use as a low frequency current injector for an industrial load. The evolution of the buss bar, buss capacitance and gate driver mother-board are discussed. Both modeling and hardware test results are presented.

Session A4L-D: RFIC, Microwave, and Optical Systems II

Chair: Vishal Saxena, *University of Idaho*
Time: Monday, August 5, 2019, 15:30 - 17:00
Location: Quorum I & II

In this paper, an approach to achieving a microwave photonic notch filter based on the use of the chromatic dispersion parameter and the length of an optical link is presented. The proposed photonic notch filter has the ability to adjust its bandwidth by varying the length of the optical link. A set of simulations are carried out for lengths of 25 km, 38 km , 50 km and 63 km. Theoretical, simulated and experimental results are in good agreement for every location of the notches obtained. The filter has potential application in the field of optical communications systems.

Session A4L-E: Neural Network II

Chair: Fathi Salem, *Michigan State University*
Time: Monday, August 5, 2019, 15:30 - 17:00
Location: Salon G & H

Session A4L-F: SPECIAL SESSION: Emerging Topics in Hardware Security and Trust

Chair: Rashmi Jha, *University of Cincinnati*
Co-Chair: Marty Emmert, *University of Cincinnati*
Time: Monday, August 5, 2019, 15:30 - 17:00
Location: Addison

Session A4L-G: Machine Learning to Enhance the Internet of Things and Environmental Monitoring

Chair: Mohsin Jamali, *University of Texas Permian Basin*
Time: Monday, August 5, 2019, 15:30 - 17:00
Location: Salon I & J

Although there is no cure for Alzheimer's disease (AD), an accurate early diagnosis is extremely important for both the patient and social care, and it will become even more significant once disease-modifying agents are available to prevent, cure, or even slow down the progression of the disease. In recent years, classification of AD through deep learning techniques has been one of the most active research areas in the medical field. However, most of the existing techniques cannot leverage the entire spatial information; hence, they lose the inter-slice correlation. In this paper, we propose a novel classification algorithm to discriminate patients having AD, mild cognitive impairment (MCI), and cognitively normal (CN) using an ensemble of hybrid deep learning architectures to leverage a more complete spatial information from the MRI data. The experimental results obtained by applying the proposed algorithm on the OASIS dataset show that the performance of the proposed classification framework to be superior to that of the conventional methods.

Tuesday, August 6, 2019

Session B1L-A: Sigma-Delta Modulators

Chair: Jose M. de la Rosa, *Instituto de Microelectrónica de Sevilla*
Time: Tuesday, August 6, 2019, 8:00 - 9:30
Location: Bent Tree I & II

A sampling technique for X-ray detectors is presented, which performs a two channel single-ended-to-differential sampling, and buffers the sampled signals serially to the incremental Sigma Delta ADC. This sampling technique maximizes the readout speed of the X-ray detectors, while allowing the ADC to sample the input signal multiple times for reduced thermal noise and higher resolution. The sampler is implemented in 0.25 um CMOS technology, as a part of a mixed signal processing backend for the pixel signal, consists of buffering, ADC conversion and readout circuits. Measured performance shows a high linearity of >77 dB SNDR at 3.5 Kfps, which emphasizes the speed advantage and high linearity of the proposed approach.

This paper studies the impact of process uncertainty on a time-based all-digital $\Delta\Sigma$ time-to-digital converter (TDC) with a differential pre-skewed bi-directional gated delay line (BDGDL) time integrator. The principle and design of the TDC are presented first. It is followed with an in-depth investigation of the impact of process uncertainty on the building blocks of the TDC. An effective calibration technique capable of minimizing the impact of process uncertainty on the performance of the TSC is proposed. The TDC is designed in a 130 nm 1.2 V CMOS technology and analyzed using Spectre with BSIM4 device models. Simulation results demonstrate that process spread has a significant impact of the delay of the building blocks of the TDC subsequently the performance of the TDC. The detrimental impact of process uncertainty can be minimized by optimizing the TDC at SS (slow NMOS/slow PMOS) corner and adjusting the delay of the key delay blocks and that of the gated delay stages of the TDC in TT (typical NMOS/typical PMOS) and at FF (fast NMOS/fast PMOS) corner to their respective SS-corner value.

This paper presents an all-digital 1st-order 1-bit $\Delta\Sigma$ time-to-digital converter (TDC) with a differential current-starved bi-directional gated delay line (CS-BDGDL) time integrator with built-in quantization. Current-starved gated delay cells are used to improve the linearity of the time integrator subsequently the SNDR of the TDC. Differential time integration is performed by simultaneously issuing right-shift and left-shift commands to the CS-BDGDL so as to minimize integration time. The error caused by current mismatch between NMOS and PMOS transistors of gated delay cells is eliminated using a digital comparator. Design methodologies for process uncertainty are explored. The TDC is designed in an IBM 130 nm 1.2 V CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM4 device models. Simulation results show that the figure-of-merit (FOM) of the proposed all-digital TDC outperforms that of all reported TDCs alike.

Session B1L-B: Voltage References and Bandgaps

Chair: Anuraj Veerabathini, *Maxim Integrated*
Time: Tuesday, August 6, 2019, 8:00 - 9:30
Location: Preston Trail I & II

Session B1L-C: Power Systems

Chair: Ali Mehrizi-Sani, *Washington State University*
Time: Tuesday, August 6, 2019, 8:00 - 9:30
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Session B1L-D: Communication Circuits I

Chair: Rushi Vyas, *University of Calgary*
Time: Tuesday, August 6, 2019, 8:00 - 9:30
Location: Quorum I & II

Session B1L-E: Internet of Vehicles (IoV) and Internet of Things (IoT)

Chair: Steven Bibyc, *Ohio State University*
Time: Tuesday, August 6, 2019, 8:00 - 9:30
Location: Salon G & H

Session B1L-F: Trusted Electronics and Security I

Chair: Srinivas Katkoori, *University of South Florida*
Time: Tuesday, August 6, 2019, 8:00 - 9:30
Location: Addison

Physical Unclonable Functions (PUFs) have emerged as a promising solution to identify and authenticate Integrated Circuits (ICs). In this paper, we propose a novel NAND-based Set-Reset (SR) Flip-flop (FF) PUF design for security enclosures of the area constrained Internet-of-Things (IoT). Such SR-FF based PUF is constructed during a unique race condition that is (normally) avoided due to inconsistency. We incorporate the process variations to leverage the capability of SR-FF to generate the unique identifier of an IC. The SPICE-level simulations presented for 90nm, 45nm, and 32nm technologies in both intra- and inter-chip variations show the robustness of SR-FF PUF in terms of uniqueness, randomness, uniformity, and bit(s) biases. Furthermore, we perform physical synthesis to evaluate the applicability of SR FF PUF on five designs from OpenCores. The estimated overhead for power, timing, and area in three design corners are negligible.

This paper proposes an analog weak physical unclonable function (PUF). The proposed PUF derives its unique key from random mismatch in a cascode current steering thermometer digital-to-analog converter (DAC). The DAC drives a voltage-controlled 7-stage ring oscillator (RO). MSB of the difference in phase outputs of two ROs generate the PUF response. An N-bit PUF key can be produced from a single proposed PUF cell by running the VCOs for N sampling periods which results in the proposed PUF having the lowest area/bit among weak PUFs. A prototype fabricated in 65nm has an intra-HD of 0.0906 and inter-HD of 0.4859 for 2048-bit PUF key.

Manufacturers normally buy and/or fabricate communication chips using third-party suppliers, which are then integrated into a complex hardware-software stack with a variety of potential vulnerabilities. This work proposes a compact supervisory circuit to classify the operation of a Bluetooth (BT) SoC at low frequencies by monitoring the input power and radio frequency (RF) output of the BT chip passed through an envelope detector. The idea is to inexpensively fabricate an envelope detector, power supply current monitor, and classification algorithm on a custom low-frequency integrated circuit in a trusted legacy technology. When the supervisory circuit detects unexpected behavior, it can shut off power to the BT SoC. In this preliminary work, we proto-type the supervisory circuit using off-the-shelf components. We extract simple yet descriptive features from the envelope of the RF output signal. Then, we train machine learning (ML) models to classify different BT operation modes, such as BT advertising and transmit modes. Our results show ~100% classification accuracy.

In this paper, we implemented a lightweight reconfigurable pseudo-random number generator (PRNG). The map generates discrete-time chaotic signals. The chaotic oscillator requires two map circuits to generate chaotic signals. The design is reconfigurable because two map circuits have two bifurcation parameters which can be leveraged to generate multiple random sequences. The design of the PRNG utilizes two chaotic oscillators, analog mux, 10 bit ADC, 2 bit shift register and an XOR gate. The circuit has been implemented in 65 nm CMOS technology with a supply voltage of 1.2 V. The estimated power consumption of the circuit is 2.12 mW and the area overhead is 0.132 mm2. The throughput of the proposed PRNG is 100 MS/s. The proposed PRNG can be used for security applications in IoT devices which requires circuits to consume less area and power overhead. The PRNG design passes all the tests in NIST SP 800-22 test suite.

Session B1L-G: Image/Video Processing and Multimedia Systems

Chair: Hongbin Sun, *Xi'an Jiaotong University*
Time: Tuesday, August 6, 2019, 8:00 - 9:30
Location: Salon I & J

Visual preservation and reproduction of subtle and feeble scene details is challenging during conversion from Hyper-spectral Image (HSI) to Low Dynamic Range (LDR) color images due to poor scene area to pixel density ratio, where a large geographical plane is mapped to a single pixel. This results in an averaging effect or a partial volume effect that affects the visual distinction of fine subtle details. Secondly, HSI data reduction to LDR color image involves sub-band averaging which again affects details distinction, especially structures of feeble strength. The proposed approach addresses this issue and improves the details in the scene for preservation and enhancement by modifying an existing HSI to LDR color image conversion method. An interim, detail enhancement stage is introduced. The results show a clear improvement in visual content reproduction and the numerical quantification also agrees to the same. The results are compared using three data sets and two other methods including the original method being modified.

Session B2P-H: Neural Systems and Deep Learning

Chair: Fakhreddine Ghaffari, *University of Paris Seine*
Time: Tuesday, August 6, 2019, 11:30 - 12:30
Location: Salon F

Serial arc is one of factors causing electrical fires. Over past decades, a variety of researches have been carried out to detect arc signals using frequency characteristics, wavelet analysis and statistical features. However, the usage of those features has shown low arc-detection performance. To solve this, we employ variational mode decomposition (VMD) to generate more time-domain signals, from which statistical features are computed from VMD mode signals, providing more informative features. Using a deep neural network (DNN) as an arc classifier, experiments validate that the VMD could improve the arc-detection performance by 4 percent.

Neural networks are commonly used in learning applications. The hardware implementation of a neural network is one challenge of a neural network. It is required to design a network to be general for any application. This paper presents a reconfigurable feed-forward neural network which can be used for any application. The proposed method has the flexibility to change the node organization to be suitable for an application. The network is divided into two parts: one part has a fixed node in each layer and the second part includes the reconfigurable nodes. The reconfigurable nodes have the ability to switch from one layer to another until reaching the optimum result. The proposed method is compared with the traditional network, and the result shows the proposed method improves the performance of the network. The hardware implementation of the proposed method is presented using VHDL and Altera 10 GX FPGA.

Neural Network can be used for many applications and it is important to keep it works without fault. Self-healing neural network became important towards reliable Neural Network (NN). Self-healing is the ability to detect and fix a fault in the system. Most of the current self-healing NN are based on replication of hardware nodes which spend higher area overhead. The proposed self-healing approach is used to reduce the area overhead and it is suitable for complex NN. The proposed method a shared operation and spare node in each layer which compensates any faulty node in the layer. Each faulty node will be recovered by its neighbor node, and the neighbor node performs the faulty node and its operations sequentially. In the case of the neighbor is faulty, the spare node will compensate them. The proposed method is implemented using VHDL and the simulation results are obtained using Altira 10 GX FPGA for a different number of nodes. The area overhead is very small for a complex network. The reliability of the proposed method is studied and compared to the traditional NN.

In this paper, we introduce, to the best of our knowledge, the first FPGA-accelerated stochastically binarized DNN implementations, and compare them to implementations accelerated on both GPUs and FPGAs. All our developed networks are trained and benchmarked using the popular MNIST and CIFAR-10 datasets. For our binarized and conventional FPGA-based networks, we achieve a >16-fold improvement in power consumption, compared to their GPU-accelerated counterparts. Also, our binarized FPGA-based networks require >25% shorter inference times, compared to their GPU-based counterparts.

Security vulnerabilities in machine learning (ML), especially in deep neural networks (DNN), is becoming a concern. Various techniques have been proposed, including data manipulations and model stealing. However, most of them are focused on ML algorithms and target threat models that require access to training dataset. In this paper, we present a methodology that analyzes the DNN weight parameters under the threat model that assumes the attacker has the access to the weight memory only. This analysis is then used to develop an attack that manipulates weight parameters with respect to their sensitivity. To evaluate this attack, we implemented our methodology on a MLP trained on IRIS dataset and LeNet (DNN architecture) trained on MNIST dataset.

Session B2P-J: Linear and Nonlinear Systems

Chair: *University of Paris Seine*
Time: Tuesday, August 6, 2019, 11:30 - 12:30
Location: Salon F

A transimpedance amplifier (TIA) graphical design technique including transimpedance gain, signal bandwidth, feedback loop stability, and noise performance is presented. The proposed graphical method allows for a more extensive design tradeoff analysis and is applicable to both compensated and decompensated opamps. The method is validated with Spice simulation and contrasted with published experimental results.

This presentation offers a design procedure when one or more constraints are continuously changing in an analog circuit. The components used for this are Fixator Norator Pairs (FNP). It starts with norators, where their variables (v and i) are linearly dependent on the design constraints, represented by fixators. So, when the constraints are changing the norators variable (as circuit components) can change and adjust themselves. It is shown that the linear dependency is applicable to the voltage and current of the norator, but when it comes to replacing it with a resistor the dependency becomes bilinear. So, for m continuously changing constraints we only need m corresponding resistors (voltage sources or current sources are also candidates) to vary and tune. A simple and efficient computational method is presented for finding these equivalent resistors. One indication of this efficiency is that, no formal matrix inversion is needed in the entire process.

Current cryptographic systems are based on functions that are easy to compute, yet finding the inverse operation is computationally complex. One of these functions is the prime factorization which is utilized in modern communication systems. Memristive circuits are challenging these standards because they enable self-organizing logic gates (SOLGs) which can be operated in reverse mode, where every node can electively be used as an input or output. So far, only investigations with idealized memristor models have been done. That is because manufacturing costs of real memristors are high. Thus, our goal is to create a highly flexible emulator for an universal SOLG to aid future investigations. We therefore exploit the wave digital algorithm to obtain an emulator which preserves stability, allows for exchangeable memristor models, and enables parameter optimization and sensitivity analyses during runtime for future research.

In this contribution a control scheme for a class of fractional-order chaotic systems and its application in the synchronization and secure transmission of data problems is designed. The asymptotic stability of the synchronization error and the ultimate bound of the information recovery error are established employing the fractional Lyapunov direct method. The proposed sigmoid-like controller is used as input to the receiver system whose states are asymptotically synchronized with the transmitter system. The technique has been applied in the synchronization and secure communications of the incommensurate fractional-order Rössler and Chen systems.

Session B2P-K: Digital Signal Processing

Chair: *University of Paris Seine*
Time: Tuesday, August 6, 2019, 11:30 - 12:30
Location: Salon F

To implement the Ising model on hardware and create "things" able to process optimization for the future IoT, a speeding up method is proposed for speeding up an Ising model. By implementing a 6×6 spin Ising model in a 16 nm CMOS FPGA, we found that the traveling salesman problem and SVM can be solved. By implementing parallel updates, higher processing speed is achieved. Furthermore, the Ising model in which the interactions were reduced on the basis of the sparsity as more than nine times faster than the fully connected Ising model.

The filtered-x least mean square (FxLMS) algorithm for active noise control (ANC) systems requires filtering of the reference signal via the cancellation path modeling (CPM) filter. The CPM filter may be available from the offline experiments. However, in many practical situations the online estimation of CPM filter may be needed due to the possible time-varying nature of the cancellation path. This paper investigates estimation of cancellation path during the online operation of the FxLMS-based feedback-type ANC system. The key idea in the proposed approach is to employ a gain-controlled probe noise mixed with the cancelation signal. The gain-factor for the probe noise is adjusted such that a large-level probe signal is used during the transient state of the ANC system. This improves the convergence of the cancellation path estimation process. As the ANC system converges, the level of the probe noise is reduced to achieve a good noise reduction performance. Simulation results demonstrate the effectiveness of the proposed method.

This work proposes an efficient analytic method for designing a class of 2D filters useful in image processing, namely wedge-shaped filters, which can be considered components of a directional filter bank. The design starts from a 1D digital filter prototype transfer function. Using accurate approximations and specific frequency mappings, first an unilateral, half-plane filter with a given orientation is obtained. Using two such unilateral 2D filters with imposed orientation angles, a desired directional wedge filter is derived, with specified orientation and aperture angles. Its transfer function results directly in a factored form, which is an advantage in implementation. The resulted wedge filter is parametric and tunable, since the specified parameters occur in the final matrix form of the filter transfer function.

Time series forecasting has application in many domains. If the state of a system of interest can be modeled as a time series, the prediction of the future state can be viewed as a time series forecasting problem. There are countless examples of such applications ranging from weather forecasting to economic metric prediction or predicting a vehicle’s position. The time scale of these problems may be very different, but they are all essentially time series. While there are many different methods for time series prediction, Time Delay Neural Networks (TDNNs) are one of the main tools for this purpose that have recently received attention. While most TDNNs may be shallow networks, other networks such as LSTM (Long Short-Term Memory) can also be used for this purpose; however, training time of LSTM is considerably more than FFTN. In this paper, we examine how a transform layer (called pre-transform layer) applied to the beginning layer of a TDNN can significantly reduce training time, while also maintaining accuracy or moderately improving it

In image processing, transform coding de-correlate images to pre-condition them for efficient compression. In this work, we propose VLSI architecture design of a hardware-efficient 9/7 Discrete Wavelet Transform (DWT). The architecture takes advantage of Canonical Singed Digit (CSD) and Distributed Architecture (DA) to represent and optimally distribute coefficients to reduce the number of adder and shift registers. In addition, the co-efficient multiplication also exploits the horizontal and vertical redundancy in the architecture to reduce the hardware computational complexity. The result is a filter based designed architecture exploiting data path diagram of a CSD represented coefficients, which selectively finds sum of products to give minimum hardware realization. The proposed architecture is modeled and simulated using HDL (Hardware Description Language). A comparison with filter-based architectures of 9/7 DWT reveals a saving up to 18.75% in hardware. The designed solution is hardware efficient and provides a low-power architecture for high-speed real time applications.

Session B2P-L: System Architectures and Embedded Systems II

Chair: *University of Paris Seine*
Time: Tuesday, August 6, 2019, 11:30 - 12:30
Location: Salon F

HLS based Optimizations of an FPGA Hardware Design for Plenoptic Image Processing Algorithm ..... N/A
Faraz Bhatti, Thomas Greiner
Pforzheim University, Germany

Optical 3D image processing algorithms are used in a wide range of applications, such as research, healthcare, industry automation. Generally, such algorithms consist of computation intensive instructions. The performance of general purpose processor based system is a bottleneck because of its sequential nature. FPGA based hardware solution can be an alternative for such problems. Due to its architecture, FPGA can exploit spatial and temporal parallelization and hence the performance with respect to execution time and area can be improved. However, creating hardware with the help of a hardware description language (HDL), such as VHDL, is a complex and time taking process. High-level synthesis (HLS) tools can be employed to resolve this issue. This paper discusses the approach to optimize the HLS based hardware architecture for plenoptic 3D image processing algorithm. It is an iterative process that requires low-level knowledge of the hardware workflow. The results show that the performance is improved.

10 GHz Standing Wave Oscillator based Clock Distribution Network Considering Distributed Capacitance 694
Gyunam Jeon, Yong-Bin Kim
Northeastern University, United States

The paper presents 10 GHz standing wave oscillator (SWO) minimizing distributed capacitance Cd (distributed capacitance generated from multiple cross-coupled pairs (CCP)) for the clock distribution network. The conventional SWOs have been proposed for a negative resistance gd (an equivalent transconductance per CCP) to get rid of conductance in RLGC extracted from a transmission line. The Cd can not only increase its phase constant but also decrease the unit length of the transmission line. Therefore, the Cd has to be minimized for better performance in the SWO. In the proposed SWO, MOS varactors, Cvar(V)(voltage controlled capacitance), are added to minimize the parasitic capacitance between M1 drain and M2 drain to minimize the capacitance cd(equivalent capacitance per CCP) caused by the parasitic capacitors. The proposed SWO generates the admittance (0.5(-gm1-gm2 -sCvar(V)+gds1,2 +gds3,4 +s(Cgs1,2 +Cgs3,4)). The FOM (ωd) of the proposed approach is about 83*10^9Hz/unit CCP, compared with 71.6*10^9Hz/unit CCP of the conventional design. The design is simulated by a 180nm CMOS technology node with 1.8V power supply, and the total power consumption is 5.4 mW.

Session B2P-M: Communication Systems and Broadband Networks

Chair: *University of Paris Seine*
Time: Tuesday, August 6, 2019, 11:30 - 12:30
Location: Salon F

An Enhanced Error Control Scheme in Real-Time Wireless Sensor Networks ..... N/A
[1]Kamaldeen Ayodele Raji, [2]Kazeem Alagbe Gbolagade, [3]Ayisat Wuraola Yusuf-Asaju
[1]Kwara State Polytechnic, Nigeria; [2]Kwara State University, Nigeria; [3]University of Ilorin, Nigeria

An improved reverse converter with error control scheme conspiring Redundant Residue Number System (RRNS) to boost the correctness of received message is proposed for real-time WSNs. The system utilized moduli set {2n+1-1, 2n, 2n-1} with additional redundant moduli set {2n+1+3, 22n - 3} in order to achieve higher error correction. Maximum likelihood was utilized to identify and correct the corrupted values to the original data. The result obtained shows that the proposed moduli set provides low vitality utilization and c

Efficient Calibration for Robust Indoor Localization based on Low-Cost BLE Sensors 702
Nizam Kuxdorf-Alkirata, Gerrit Maus, Dieter Brückmann
University of Wuppertal, Germany

The fingerprinting method for indoor localization is associated with a high calibration effort. In order to improve the efficiency of this time-consuming method, a new calibration procedure is proposed. It allows to reduce the calibration effort associated with fingerprinting considerably and ensures a sufficient accuracy at the same time. The proposed procedure takes into account the geometry of the environment subject to study, in order to empirically estimate the distribution of the signal strength at predefined positions. Thus, mobile sensor localization can be carried out robustly and the deviation from real position is less than 0.75 m in about 90% of the cases. This is achieved even though the calibration effort is reduced by almost 84% compared to the original one.

Session B2P-N: Power Electronics and Hybrid Systems

Chair: *University of Paris Seine*
Time: Tuesday, August 6, 2019, 11:30 - 12:30
Location: Salon F

Session B3L-A: SAR ADCs

Chair: Qiyuan Liu, *Qualcomm*
Time: Tuesday, August 6, 2019, 13:30 - 15:00
Location: Bent Tree I & II

Session B3L-B: Amplifiers I

Chair: Igor Filanovsky, *University of Alberta*
Time: Tuesday, August 6, 2019, 13:30 - 15:00
Location: Preston Trail I & II

Session B3L-C: Integrated DC/DC Converters

Chair: Jose Silva-Martinez, *Texas A&M University*
Time: Tuesday, August 6, 2019, 13:30 - 15:00
Location: Mesquite I

Session B3L-D: Communication Circuits II

Chair: Steven Bibyc, *Ohio State University*
Time: Tuesday, August 6, 2019, 13:30 - 15:00
Location: Quorum I & II

Session B3L-E: SPECIAL SESSION: Internet of Things: Sensors to Cyber-Security

Chair: Neeraj Magotra, *Western New England University*
Time: Tuesday, August 6, 2019, 13:30 - 15:00
Location: Salon G & H

Session B3L-F: Trusted Electronics and Security II

Chair: Manuel Jimenez, *Univ. of Puerto Rico*
Time: Tuesday, August 6, 2019, 13:30 - 15:00
Location: Addison

Session B3L-G: Recent Advances in Digital Arithmetic Devices and Digital Filter Designs

Chair: William Jenkins, *Pennsylvain State University*
Time: Tuesday, August 6, 2019, 13:30 - 15:00
Location: Salon I & J

Session B4L-A: Design Techniques for TDCs, ADCs and DACs

Chair: Sebastian Hoyos, *Texas A&M University*
Time: Tuesday, August 6, 2019, 15:30 - 17:00
Location: Bent Tree I & II

Session B4L-B: Amplifiers II

Chair: Aydin Karsilayan, *Texas A&M University*
Time: Tuesday, August 6, 2019, 15:30 - 17:00
Location: Preston Trail I & II

Session B4L-C: SPECIAL SESSION: Advanced Power Management ICs: Design, Analysis and Methodology

Chair: Punith Surkanti, *Maxim Integrated*
Co-Chair: Paul Furth, *New Mexico State University*
Time: Tuesday, August 6, 2019, 15:30 - 17:00
Location: Mesquite I

Session B4L-D: Communication Circuits III

Chair: Yushi Zhou, *Lakehead University*
Time: Tuesday, August 6, 2019, 15:30 - 17:00
Location: Quorum I & II

Session B4L-E: SPECIAL SESSION: RFID-Based Sensors for the Internet of Things

Chair: Juan Montiel-Nelson, *University of Las Palmas de Gran Canaria*
Time: Tuesday, August 6, 2019, 15:30 - 17:00
Location: Salon G & H

This paper presents the design of a wireless sensor network for oceanic floating cages in aquaculture. The deployment of the sensor network over current aquaculture installations is discussed. The software and hardware of a sensor node are outlined. A wireless information and power transfer interface, based on the ISO 11784/11785 HDX standard, for underwater sensor nodes are studied. The misalignment problem in the wireless interface antennas is evaluated in depth. In addition, it is determined the maximum allowed misalignment to keep the information and power transfer efficiency over 70%. Moreover, we establish a linear function to model the charging rate with a maximum error of a 2.2%. Finally, all data presented in this paper is based on real measurements over the sensor node prototypes implemented with commercial devices.

Session B4L-F: System Architectures I

Chair: Yong-Bin Kim, *Northeastern University*
Time: Tuesday, August 6, 2019, 15:30 - 17:00
Location: Addison

This paper studies the FPGA implementation of a successive-cancellation (SC) decoder for polar codes which have recently attracted attention as error-correcting codes adopted for 5G wireless systems. We focus on effective ways of partitioning the SC decoding procedure into combinatorial and sequential logic parts. We demonstrate an FPGA implementation of the decoder architecture for a 1024-bit length polar code and show that our FPGA decoder can achieve three times higher throughput than the conventional sequential semi-parallel decoder without significantly increasing the hardware resources.

Sorting is one of the most important computational tasks in data processing applications. Recent studies show that the FPGA-based hardware accelerators are more efficient than the general-purpose processors and GPUs. By increasing the input records in the sorting network, the number of Compare- And-Swap (CAS) units would be increased, which in turn, will lead to increased resource consumption. In some applications, the number of available resources is limited. Thereby, it is necessary to optimize resource requirements while maintaining a sufficient level of performance. This paper presents a new sorting architecture that reduces the number of required resources compared to the state-of-the-art sorting architecture and achieves the desired performance using Unary processing. Results indicate that the proposed architecture increases throughput by 29.1% and reduces the number of LUTs by 42%, for sorting 8-input records, compared to other architecture.

Threshold logic inspires from the principle of the firing of neurons mimicking synaptic connections of a binary neural network to create generalized logical functions for solving complex cognitive tasks such as object detection. We propose an implementation of modular and hierarchical threshold logic network in FPGA that aims to provide a low complexity near sensor co-processing hardware solution for object detection in digital cameras. The proposed network has been designed and implemented on a Xilinx Zynq SoC. The solution is robust in terms of object detection even in the presence of high levels of occlusion, noise and illumination changes. The total power consumption of the design is estimated to be 8.6 W. Performance analysis of the detector IP core is thoroughly simulated on test databases for computer vision with real-world images. The object detection module ensures a high performance rate of about 5000 frames per second at 100 MHz clock frequency while processing 100 × 100 pixel images.

The paper describes the FPGA implementation of a novel TDOA distance evaluation algorithm that combine the characteristics of an OFDM symbol with the properties of the Zadoff-Chu mathematical sequences. The distance evaluation system has been validated in presence of severe multipath interference and allows to achieve an accuracy that is always within 1.2cm of the target position. The algorithm is implemented using the FPGA (Cyclone IV-E EP4CE115F29C8L Cyclone IVE) available on the Altera's DE2-115 development board. The implementation requires about 120k bit of memory and less than 40k logic elements (of which about 30k are registers).

Efficient Hardware Architecture for Overlap-Add Method of Short-Time Fourier Analysis/Synthesis ..... N/A
Mohammed Bahoura
University of Quebec at Rimouski, Canada

This paper presents an efficient hardware architecture of the overlap/windowing and overlap-add techniques for real-time FFT/IFFT-based signal processing algorithms. Short-time overlapped frames are extracted and windowed before applying short-time Fourier analysis/synthesis. The original signal is perfectly reconstructed from the windowed (modified) frames using the overlap-add (AOL) technique. This architecture has been implemented on Field Programmable Gate Array (FPGA) using a high-level programming tool.

Session B4L-G: Control Systems, Mechatronics, and Robotics I

Chair: Ying-Khai Teh, *San Diego State University*
Time: Tuesday, August 6, 2019, 15:30 - 17:00
Location: Salon I & J

Magnetic Angular Position Sensing with High Stray Field Immunity for Mechatronic Applications 1001
Marcus Prochaska, Kris Rohrmann, Marvin Sandner, Phil Meier
Ostfalia University of Applied Sciences, Germany

Magnetic field sensors are of prime importance for robotics, industrial and automotive applications. Due to the digital transformation there is a increasing density of electronic systems in mechatronics. Thus, the number of stray field sources is rising. In this paper a novel approach for the suppression of disturbing magnetic fields is presented. Instead of a single angle sensor the proposed methodology uses an array consisting of 2D magnetometers. An efficient sensor signal processing, which is based on 2D DFT, calculates the angular position and eliminates angle errors. Simulations were conducted in order to validate the presented methodology.

A Numerical Methodology for a 6 DOF Pose Estimation with 3D Magnetic Field Sensors 1005
Phil Meier, Kris Rohrmann, Marvin Sandner, Marcus Prochaska
Ostfalia University of Applied Sciences, Germany

Linear and angular position sensing using magnetic field sensors play a decisive role in automotive, industrial and consumer applications. Recently powerful 3D Hall sensors have become available, which enables simple measurement setups for 3D position sensing. In this paper a numerical concept for the determination of linear and angular position in the three-dimensional space is presented, which bases on an analytic model of an encoder magnet. To prevent numerical instabilities, a modified Newton-Raphson algorithm with adaptive dynamic step size control is used. Simulation results validate the applicability of our approach.

Predictive Control of a Robot Manipulator with Deep Reinforcement Learning ..... N/A
Eduardo Bejar
Pontificia Universidad Catolica del Peru, Peru

This paper tackles the problem of trajectory following of a two-link rigid robot manipulator. The proposed controller bases its operation on the idea behind preview control in which the control law is divided in two parts: a feedback component that depends only on the present state of the system, and a predictive component that only uses future values of the reference trajectory. In this sense, the designed controller uses for training and control both present and future states of the system. Simulation results when following a test trajectory are presented to validate the proposed method and to show that the proposed controller exhibits better performance with respect to a neurocontroller that does not use a predictive component neither for training nor control.

Power Quality Evaluation and Optimization of Sensor-Less Field Oriented Controller on 32-Bit ARM Cortex Microcontroller 1013
Xin Xue, Ying-Khai Teh
San Diego State University, United States

Electronic speed controller (ESC) is an important subsystem in drones, which are used to control and regulate the speed of its electric motor. For the high-end drones which require longer flight times, higher dynamic behavior with smooth and stable performance, Field Oriented Controllers (FOC) which power three-phase sinusoidal back-EMF motors are typically used to provide the required high efficiency, small torque ripple and dynamic performance. This paper proposes an analysis method based on discrete Fourier transform (DFT) over the measured motor current, in order to optimize the system parameters such as modulation period, CPU clock frequency and power supply voltage. As proof of concept, a FOC-based ESC implemented in a generic 32-bit microcontroller is studied. Findings show that the power quality and motor dynamic performance of a FOC ESC depends strongly on modulation period and relatively insensitive with respect to CPU voltage and frequency scaling.

Wednesday, August 7, 2019

Session C1L-A: Circuits for RF Communication

Chair: Sebastian Hoyos, *Texas A&M University*
Time: Wednesday, August 7, 2019, 8:00 - 9:30
Location: Bent Tree I & II

In this paper a low power active-RC filter exhibiting a reconfigurable transfer function, 3rd/5th order Butterworth, integrated in a low IF GPS receiver and fabricated in 0.35um SiGe BiCMOS technology is presented. This 17/26 dB gain filter has a bandwidth of 2.6MHz which is centered at 4.1MHz. It drains 1/1.25mA from a 2.7V supply in 3rd/5th order modes. The average in-band image rejection of this 0.58 mm2 filter is better than 25dB. This trimmed filter employs a quadrature offset cancellation circuit to remove all the available offset coming from the mixer output and its own mismatches.

The paper describes design of solid-state transformers operating at the frequency around 60 GHz. These transformers are approximated as two flat coils located in parallel planes (Bitter coils). A well-known formula for the mutual inductance between two loops located in parallel planes (Maxwell coils) is used to derive the approximate value of mutual inductance of two such coils. The result is improved using three correction factors. The first factor considers the increase of inductance when the round loop is substituted by an octagon. The second factor considers the reduction of inductance when the ideal wire is substituted by a strip. The third factor considers the skin-effect and proposes increasing the effective distance between the coils. The calculation of the primary (or secondary) self-inductance is based on the well known formula of ideal loop inductance, and this result is improved by the first and second correction factors. Two transformers are designed as examples: a planar transformer using the top metal for both primary and secondary, and a stacked transformer with primary in the top metal and secondary in the second from the top metal.

This paper presents a new quenching waveform generation and calibration for sensitivity optimization of super-regenerative (SR) receivers. To achieve high sensitivity, calibration of the slope and step variations of the optimal quenching waveform (OQW) is needed. The proposed sensitivity optimization uses an optimal crossing point waveform calibration technique to achieve maximum sensitivity during the sensitivity accumulation (SA) region. The proposed OQW circuit and its calibration loops are implemented in 180nm CMOS technology and tested within an SR receiver with a center frequency of 2.4GHz.

A high speed and high conversion gain envelope detector (ED) is designed for RF super-regenerative-oscillator (SRO) receivers. To reduce glitches from RC filtering used for common mode signal rejection, the proposed ED is implemented using a band-pass buffer as a first stage. To avoid introducing excessive time delay and maintain good performance under high data rate, the proposed design introduces back-to-back inverters operating in linear mode to enhance the conversion gain while reducing the settling time. Simulation results using 0.18um CMOS technology shows that the proposed ED achieves a high data rate of 6.66Mbps while consuming 8.45uW.

Session C1L-B: Oscillators

Chair: Qiyuan Liu, *Qualcomm*
Time: Wednesday, August 7, 2019, 8:00 - 9:30
Location: Preston Trail I & II

This paper studies the use of the body terminal as control voltage of ring oscillators implemented in Fully Depleted Silicon on Insulator (FD-SOI) CMOS. This technology allows to increase the body factor with respect to conventional (bulk) processes, thus allowing a wider tuning range of the threshold voltage. This effect is exploited in this work to improve the linearity of Voltage-Controlled Ring Oscillators (VCROs) to be used as building blocks of Analog-to-Digital Converters (ADCs). An intuitive analysis of basic VCRO current-starved inverter cells is carried out in order to derive an approximate expression of the voltage-to-frequency characteristic. Electrical simulations in a 28-nm node are shown to get insight about the influence of main design parameters and applied to the design of VCRO-based Sigma-Delta (SD) ADCs up to the layout level, whose performance metrics demonstrate the benefits of the presented approach

In this paper, a super-harmonic injection-locked ring oscillator (ILRO) is proposed. The proposed ILRO has been designed and simulated using a 130-nm CMOS technology. The circuit is injected with a 7.6-GHz clock signal and generates 10 output clocks of 1.52 GHz each. The proposed design occupies an area of approx. 0.001 (mm)^2, has a phase noise of -148.1 dBc/Hz at 1-MHz offset frequency and consumes 9.97 mW from a 1.2-V supply achieving a figure of merit (FoM) of 201.8 dBc/Hz.

Session C1L-C: SPECIAL SESSION: Low-Power Devices, Circuits, Systems, and Algorithms for the Internet of Things I

Chair: Aatmesh Shrivastava, *Northeastern University*
Co-Chair: Vishal Saxena, *University of Idaho*
Time: Wednesday, August 7, 2019, 8:00 - 9:30
Location: Mesquite I

We present two technology portable design techniques to achieve zero steady-state output voltage ripple in digital LDOs. Traditional digital LDOs have an inherent output voltage ripple due to the limit cycle oscillations at a frequency of F_clock/(2*Mode). We use a 4-bit digital LDO as the test vehicle to investigate these two new techniques. The first method uses body biasing of the switches via an auxiliary analog loop to minimize the ripple voltage. Effectively, the analog loop enables the power switches to carry the extra ripple current and has little impact on the efficiency. In the second method, zero steady-state ripple is achieved by modulating the gate-driver voltage-swings at the power-switch gate. In both the techniques, when the digital LDO is in steady state, the analog loop only carries the ripple current magnitude. Control from the analog and digital loops are ping-ponged based on load transients. The LDO design handles inputs from 0.5-1.5V and supports a 0.4-1.2V output voltage for a load range of 0.1-to-20mA (200X). The LDO achieves 99.4% current efficiency and near-zero output voltage ripple.

In this paper, feed-forward and class AB techniques are explored for the design of high-frequency Operational Transconductance Amplifiers (OTA) suitable for ADC architectures. The paper is focused on high gain broadband amplifiers; the first part of the paper revisited the recycling folded-cascode (RFC) architectures. These topologies are power efficient solutions but careful design is needed to avoid the presence of medium-frequency zero-pole pairs that may significantly increase residue amplifier settling time. The two stage class AB amplifier is revisited as well; the popular Monticelli's biasing circuit for class AB amplifiers is power efficient and result in high slew-rate solutions. An alternative class AB solution is proposed in this paper. The biasing of the class AB output stage employs a common-mode feedback, and results in a faster and more power efficient architecture; power consumption is around 75% that of the conventional class AB architecture and shows 3dB lower IM3 for the design of a state-variable 25MHz high-Q biquadratic filter.

We present a novel logic family, titled feedforward leakage self-suppression logic (FLSL), for nanowatt and sub-nanowatt always-on circuits. It addresses the prohibitively long delay of existing ultra-low leakage logic families without requiring sleep or mode control signals to exercise the leakage-suppression mode. Implemented in 180-nm CMOS, the proposed logic family achieves femto-watt per-gate leakage and a fan-out-of-4 (FO4) delay of 10.2 µs, a remarkable speed enhancement of 150X over the prior art in the same process in the same leakage level. We also investigate the impact of technology scaling by designing the FLSL logic family additionally in 65-nm and 28-nm processes. In a 28-nm process, the FLSL can achieve about 70 ns FO4 delay and 10 picowatts per-gate leakage. Finally, we prototype a finite impulse response filter core for physical sensing systems in a 180 nm. The filter can achieve the power consumption of 109 picowatts for sparse, i.e., predominantly constant or slowly changing, input signals at 1 kHz clock frequency.

Session C1L-D: SPECIAL SESSION: Wireline Communications for High-Performance Computing Applications I

Chair: Armin Tajalli, *University of Utah*
Time: Wednesday, August 7, 2019, 8:00 - 9:30
Location: Quorum I & II

Higher data rate requirements in data centers have motivated more spectrum efficient modulation to combat additional ISI at higher frequencies. But this also leads to significant SNR penalty. In addition to that technology scaling is shifting equalization from analog domain to the digital domain. Therefore, recent trend is to explore ADC-DSP based receiver where higher performance equalization such as viterbi decoder can be implemented. But the power consumption and complexity have limited their adoption in conventional SerDes applications. In this work we will introduce several low power implementation techniques such as analog to sequence conversion and direct branch matric estimation to explore possibility of sequence decoding in SerDes domain. Implemented prototype validates that the proposed sequence decoding is capable of compensating 35+ dB loss at 10 Gb/s with better than 10 pJ/bit energy efficiency.

This paper proposes a stochastic wireline communication system. In the proposed stochastic system, the information is encoded in the statistical parameter of noise such as standard deviation, and the noise signal is transmitted on the channel. The receiver estimates the standard deviation of the received noise signal and recovers the information. A stochastic receiver architecture, which can differentiate between the noise signals with two different standard deviations is presented. Using mathematical modeling, this paper demonstrates that the proposed stochastic transceiver has a potential to improve the SNR by more than 3dB over a conventional uncoded deterministic transceiver.

This article analyzes the potentials of different signaling methods to reach very high data communication speeds over copper channels. As the available bandwidth is limited in this type of channels, sensitivity to ISI (inter-symbol interference) turns out to be the key parameter influencing both data rate, and energy consumption. Performance of some of the main common signaling methods, all based on non-return to zero (NRZ), used in wire-line communications, are examined for implementing short-reach links. Moreover, it is shown that proper combination of spatial and amplitude domain coding improves the signal quality (i.e. eye opening), enabling data transfer rates beyond 112 Gb/s.

Session C1L-E: Digital Signal Processing I

Chair: Tarek Elarabi, *Penn State University*
Time: Wednesday, August 7, 2019, 8:00 - 9:30
Location: Salon G & H

Hardware Implementation of a Parallel EVD Processor based on Jacobi Method ..... N/A
Yudong He, Feixiang Huo, Youjiang Liu, Botao Xiong
China Academy of Engineering Physics, China

Computing eigenvalues and eigenvectors of a symmetric matrix is frequently encountered in adaptive array processing. In this paper an efficient parallel architecture of EVD (eigenvalue decomposition) processor based on Jacobi method is proposed. Cordic based fixed-point vector translators and rotators are its basic processors. A scheme of Jacobi ordering is also designed to provide a very high degree of parallelism. With appropriate number of Jacobi sweeps and word-length, convergence time and computation accuracy can be ensured. Implementation results show that it achieves lower resource utilization and higher performance with respect to floating-point operations.

Linear Error Modeling and Noise Smoothing for Improved Low-Cost IMU-Based Indoor Positioning 1069
Nizam Kuxdorf-Alkirata, Fotios Kasolis, Dieter Brückmann, Oliver Koch
University of Wuppertal, Germany

In order to improve the accuracy of indoor positioning systems, an auxiliary signal analysis method is embedded to a path reconstruction algorithm. The proposed method takes into account calibration data that is obtained from an inertial measurement unit while it is at rest, and continues to work on the fly to adjust the output of the path reconstruction algorithm adaptively. A post-processing filter is employed to further reduce fluctuations in the econstructed path.

Design of a 2D Median Filter with a High Throughput FPGA Implementation 1073
Anish Goel, M. Omair Ahmad, M.N.S. Swamy
Concordia University, Canada

In this paper, a hybrid technique for median filtering of images affected by impulse noise is implemented. Our technique combines impulse noise detection, histogram based median calculation and bit-plane processing to obtain approximate median with the aim of optimizing throughput. Implementation of the proposed median filter hardware results in a throughput of 282 Full High Definition (FHD) frames per second on Zynq-7 FPGA; 48% higher than the throughput of low-latency median filter. Compared to FPGA implementation of low complexity noise removal technique, the proposed median filter utilizes 45% of FPGA slices and provides a speed-up of 2.2 on Zynq-7 FPGA.

Session C1L-F: System Architectures II

Chair: Hakduran Koc, *University of Houston-Clear Lake*
Time: Wednesday, August 7, 2019, 8:00 - 9:30
Location: Addison

Impact of Uncertainty and Correlations on Mapping of Embedded Systems 1077
Wenkai Guan, Milad Ghorbani Moghaddam, Cristinel Ababei
Marquette University, United States

The impact of multiple levels of uncertainty in design parameters and uncertainty correlations on the quality of mapping solutions in embedded systems is investigated. The investigation is done with a simulation tool developed to conduct multi-objective design space exploration in order to generate robust Pareto frontiers in the solution space formed by reliability, execution time, and energy as design objectives. The simulation tool integrates proposed models for uncertainty and a hyper volume based technique for quantifying the difference between Pareto frontiers. Simulations results show that by not considering uncertainty and correlations between different sources of uncertainty can lead to overestimation of the performance of the optimal solutions.

Soft Voting-Based Ensemble Approach to Predict Early Stage DRC Violations 1081
Riadul Islam, Md. Asif Shahjalal
University of Michigan-Dearborn, United States

Reducing human effort and design schedule time is facing a tremendous challenge from the cutting-edge technology node, which hinders profitability from IC manufacturing. Initiatives like DARPA IDEA have addressed this challenge by aiming for a 24-hour design turnaround time, maximum resource utilization, and productivity of ICs. In this paper, we proposed a robust ensemble learning model to predict DRC from the placement stage, which precisely predicts design routability and DRC hotspots of a design. The proposed algorithm uses a soft voting classifier to combine random forest and gradient boosting algorithms. Our approach achieved a maximum precision, recall, and F1 score of 97\%, 97\%, and 96\%, respectively, which are significantly better than the state-of-the-art support-vector machine (SVM)-based prediction scheme.

WITHDRAWN

Session C1L-G: Control Systems, Mechatronics, and Robotics II

Chair: Sorore Benabid, *Institut polytechnique des sciences avancées*
Time: Wednesday, August 7, 2019, 8:00 - 9:30
Location: Salon I & J

Bayes' rule can be computed stochastically using a simple Muller C-element, providing an efficient means of implementing Bayesian inference for autonomous robots. This provides such machines with the ability to make decisions when there is uncertainty in the data or models, enabling adaptation to unknown or dynamic environments. Prior studies have not addressed the practical aspects of designing the stochastic number generators (SNGs) required for creating the probabilistically-encoded values at the inputs. In this work, two approaches are evaluated: the use of linear feedback shift registers (LFSRs) and the use of low discrepancy sequence (LDS) generators. In the case of the LFSRs, this paper shows that there is no significant degradation in performance when several SNGs are shared with one LFSR provided a sufficient amount of circular shifting is used between each SNG. Results show an LDS generator is beneficial for lowering the amount of autocorrelation that is input into the C-element, resulting in improved performance.

Session C2L-A: Photonics

Chair: Samuel Palermo, *Texas A&M University*
Time: Wednesday, August 7, 2019, 11:30 - 12:30
Location: Bent Tree I & II

In this paper, we present a new electrical model for perimeter gated single photon avalanche diode (PGSPAD) based silicon photomultiplier (SiPM) detector. PGSPAD is a SPAD with an added polysilicon gate. The extra gate terminal of the PGSPAD device mitigates the perimeter edge breakdown and tunes the operating range, noise performance, efficacy. The proposed PGSPAD SiPM model allows to accurately simulate the static, dynamic and stochastic noise behavior of the SiPM detector considering the built-in randomness of the physical process fundamental to the device operation with the effect of additional gate terminal. Simulation results are validated with experimental measurements of the PGSPAD SiPM fabricated in 0.5 μm CMOS process. Simulation results show very good matching with experimental measurements. The proposed model is a helpful simulation tool for the CMOS PGSPAD SiPM designer to evaluate the effect of parameters with additional gate terminal to optimize the performance and the PGSPAD SiPM user to design the optimum readout electronics.

A scheme to realize Optical PAM-4 transmitter by driving a three-segment microring modulator with tunable voltage-mode drivers is presented. This proposed scheme provides linearly spaced PAM-4 levels and is further categorized into two schemes, namely higher "0" and lower "1" tuning. The two schemes are verified using co-simulation of voltage-mode drivers implemented in 65nm CMOS and Verilog-A compact models for photonic components based on a silicon photonic process from IMEC. Also, the robustness of our proposed scheme can be proved by achieving high linearity when phase-shifter length variation is present.

A digital silicon photomultiplier (SiPM) using segmentation technique is designed, simulated and fabricated in the AMS 0.35 um SiGe BiCMOS process. The digital SiPM is intended for photon counting applications. The digital SiPM consists of 16 avalanche photodiodes (APD) each with active area of 24 um x 24 um arranged in a 4x4 array with series 236 k ohm quench resistors. The SiPM has a peak responsivity at 490 nm wavelength and a fill factor of 12.6%. The digital SiPM generates an output 5-bit digital word. The digital SiPM occupies an area of 0.38 mm2.

Session C2L-B: Nanoelectronics and Nanotechnology

Chair: Mohamed Shaban, *Southern Arkansas University*
Time: Wednesday, August 7, 2019, 11:30 - 12:30
Location: Preston Trail I & II

As a result of a decrease in cross-section, increases have been noted in several thermal and electric properties of copper interconnects. To mitigate such concerns, new approaches are being considered for new wiring solutions for VLSI technologies. The incorporation of carbon nanotubes (CNTs) in VLSI design to replace existing interconnection material, may be an efficient and cost-effective evolution from current materials. Carbon nanotubes, more specifically multi-walled carbon nanotubes (MWCNT), have been identified as potential alternatives to diminish such concerns. This paper will delineate the shared and differing aspects of each of the CNT structures.

Nano M-S contacts show a non-conventional I-V behavior compared to the planar–Schottky contacts. The enhanced tunneling current due to the narrowing barrier width results from the enhanced electric field at the nano M-S interface. Nano Schottky junctions are sensitive to different doping concentrations of n-type semiconductor substrates. The low dope concentration substrate increases the probability of free electrons in the metal to tunneling through the thin junction barrier to the conduction band of the semiconductor. The model was examined using conductive Atomic Force Microscope with a gold coated nano tips and compared with the simulation model.

This work presents an Insulator Metal Transition (IMT) based Integrate-And-Fire (IAF) neuron. The proposed neuron leverages the switching mechanism of the IMT device to deliver the neuron functionality without the need for complex CMOS circuitry. The IMT neuron parameters such as the threshold voltage and the refractory period, however, are dependent on the device parameters. Design expressions for the IMT neuron are derived. These expressions can aid designers choosing the proper circuit variables given a specific IMT device with a particular set of device parameters.

Session C2L-C: SPECIAL SESSION: Low-Power Devices, Circuits, Systems, and Algorithms for the Internet of Things II

Chair: Aatmesh Shrivastava, *Northeastern University*
Co-Chair: Vishal Saxena, *University of Idaho*
Time: Wednesday, August 7, 2019, 11:30 - 12:30
Location: Mesquite I

Asynchronous circuits have many advantages over their synchronous counterparts in terms of robustness to parameter variations, wide supply voltage ranges, and potentially low power by not needing a clock, yet their promise has not been translated yet into commercial success due to several issues related to design methodologies and the need for handshake signals. Stochastic computing is another processing paradigm that has shown promises of low power and extremely compact circuits but has yet to become a commercial success mainly because of the need for a fast clock to generate the random streams. The Asynchronous Stream Processing circuits described in this paper combine the best features of asynchronous circuits (lack of clock, robustness) with the best features of stochastic computing (processing on streams) to enable extremely compact and low power IoT sensing nodes that can finally fulfill the promise of smart dust, another concept that was ahead of its time and yet to achieve commercial success.

Session C2L-D: SPECIAL SESSION: Wireline Communications for High-Performance Computing Applications II

Chair: Armin Tajalli, *University of Utah*
Time: Wednesday, August 7, 2019, 11:30 - 12:30
Location: Quorum I & II

Session C2L-E: Digital Signal Processing II

Chair: M. Omair Ahmad, *Concordia University*
Time: Wednesday, August 7, 2019, 11:30 - 12:30
Location: Salon G & H

This paper presents a modified two-stage corrector comb-based decimation structure with an improved magnitude characteristic in all folding bands. This is achieved by inserting a simple multiplierless filter into the first stage of the two-stage corrector-comb-based structure. Additionally, the maximum absolute value of the passband deviation is decreased and it is equal to 0.1 dB, for the cascade of three and four combs, while for the cascade of two and five combs it is equal to 0.2 dB. The method is illustrated with one example. The comparisons with the methods in literature are also included.

To avoid the occurrence of non-computable, delay-free loops, classic Wave Digital Filters (WDFs) usually exhibit a tree-like topology. However, recent advances led to a strictly modular realization of the former structures by identification of contractivity properties of WDFs, allowing an assured con- verging iterative procedure, which depends on the presence of artificial port resistances. In this paper, an improved semi-modular approach based on Multi-dimensional Wave Digital Filters (MDWDFs) is presented for the mentioned topologies. Therefore, a new method of Automatic Differentiating Wave Digital Filters (ADWDFs) is proposed to overcome convergence speed limitations induced by artificial port resistances, making the improved approach independent of the same.

Session C3L-B: Analog Design Applications

Chair: Jose Silva-Martinez, *Texas A&M University*
Time: Wednesday, August 7, 2019, 13:30 - 15:00
Location: Preston Trail I & II

Inrush-current limiting voltage regulators are considered important components in many voltage and current drivers applications, to reduce the startup surge of current from the voltage supply to the supplied loads. Moreover, driving stable current to multiple filament light sources is necessary to improve their life-time and reduce light fluctuations. In this paper, a fully-integrated soft-start linear voltage regulator is proposed, for driving high current to filament light sources. In addition to the soft startup feature, this proposed technique is used to allow introducing new loads during operation without disturbing the regulated output. The design has been implemented in 130nm technology. The maximum driving current is 1.5A from 5V supply. Minimum drop-out voltage of 250mV is used to supply different filament light sources.

An energy-efficient analog front-end circuit for ultrasound imaging applications in X-FAB's 0.18-micron Modular high-voltage (HV) SOI CMOS technology is presented. The front-end circuit is composed of a supply-doubled three-level HV pulser and a low power complementary noise-canceling (NC) low noise amplifier (LNA). The proposed HV pulser can generate a three-level 53 Vpp pulse from 30 V supply at 10MHz frequency, which improves transmitter (Tx) efficiency when compared with conventional methods. The low power LNA can achieve a 2.5 dB noise figure (NF), 15.2 dB voltage gain while only consuming 0.27 mW at 1.8 V supply voltage.

A new approach for circuits devoted to speech recognition and voice activity detection is proposed. This new approach is based on using VCO-based ADC filters, which enable us to implement an architecture with very small area and low power consumption. The architecture is validated by behavioral simulation and designed in a 130-nm CMOS process to estimate the occupied area and the power consumption. The simulated results show that the solution is the best in terms of area with a competitive power consumption, very suitable for portable devices and Internet-of-things (IoT) applications.

Session C3L-C: MEMS, NEMS and Emerging Technologies

Chair: Mohamed Shaban, *Southern Arkansas University*
Time: Wednesday, August 7, 2019, 13:30 - 15:00
Location: Mesquite I

Session C3L-D: Wireless and Wearable Systems

Chair: Vishal Saxena, *University of Idaho*
Time: Wednesday, August 7, 2019, 13:30 - 15:00
Location: Quorum I & II

Session C3L-E: Embedded Electronics

Chair: Juan Montiel-Nelson, *University of Las Palmas de Gran Canaria*
Time: Wednesday, August 7, 2019, 13:30 - 15:00
Location: Salon G & H

This paper presents an improved Othello game solver using the Hardware/Software Co-Design approach. Enhancements in Data Communication, Searching Algorithm, and Evaluation function have been made to beat the prevalent implementations. A novel 64-bit Communication model is proposed which transfers the current board position from the Processing System to the Programmable Logic through a 64-bit change board, instead of the complete 128-bit board. The proposal uses NegaScout searching algorithm along with Transposition Table and Node Ordering; and features like Opening Book, Killer Heuristics, and Bitboards. An Adaptive Evaluation function assigns variable weights to Mobility, Stability, Corner Occupancy, and Disc Differential depending upon the game stage. At a search depth of eight, the proposed communication model improves the communication overhead by 19.5%. Overall, the proposed design demonstrates 75.06% improved performance as compared to the prevalent implementation, and 6.53 times faster than its software implementation on the same platform.