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**Time:** Monday, August 5, 2019, 8:00 - 9:30

**Location:** Preston Trail I & II

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<sup>1</sup>José C. García, <sup>1</sup>Juan A. Montiel-Nelson, <sup>2</sup>Saeid Nooshabadi

<sup>1</sup>University of Las Palmas de Gran Canaria, Spain; <sup>2</sup>Michigan Technological University, United States

A current mirror based low voltage single supply CMOS level up-shifter (fcm-ls) for upconverting signals from 0.4 to 0.8V power supply domain is presented in this work. Based on the post-layout simulation, fcm-ls provides 48.5% lower energy consumption and 29.7% better speed than a similar circuit topology (vl-ls). Both circuits are evaluated on UMC 65nm CMOS process and low threshold voltage transistors. Using a power supply of 0.8V, and an input voltage range of 0.4V, we obtain up to 63.4% energy-delay-product (EDP) improvement at 500MHz frequency, at 590fF output loading, over reference circuit. Active area is optimized to achieve low static and dynamic energy consumption at the maximum load capacitance. The limits of proposed circuit are verified using the post-layout simulation results.

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Mario Auer, Maximilian Scherzer

Graz University of Technology, Austria

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**Chair:** Ayman Fayed, *Ohio State University*

**Time:** Monday, August 5, 2019, 8:00 - 9:30

**Location:** Mesquite I

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Mahmoud Elhebeary, Chih-Kong Ken Yang

University of California, Los Angeles, United States

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*Nan Chen, Tingcun Wei, Jianfu Liu*

Northwestern Polytechnical University, China

A new pulse width modulation (PWM)-based digital control for single-inductor multi-output (SIMO) DC-DC converters operating in continuous current mode (CCM) is proposed in this paper. To reduce the complexity of the control system and the hardware cost, only one digital-proportion-integration-differentiation (D-PID) compensator is used for the SIMO converters, and an idle period is introduced between each phase of the converters to reduce cross-regulation. Then, a SIMO buck DC-DC switching converter using the proposed control with two outputs is designed and implemented on a field-programmable gate array (FPGA) platform. The test results indicated that this SIMO converter can convert an input of 5V to 1.8 V and 2 V. Load transient measurements demonstrate that the cross-regulation is 0.13 mV/mA with a 300-mA load current change at output 1, and 0.04 mV/mA with a 500-mA load current change at output 2.

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<sup>1</sup>Paul M. Furth, <sup>1</sup>Anurag Veerabathini, <sup>1</sup>Z.M. Saifullah, <sup>1</sup>Derrick T. Rivera, <sup>1</sup>Abdelrahman Elkanishy,

<sup>1</sup>Abdel-Hameed A. Badawy, <sup>2</sup>Christopher P. Michael

<sup>1</sup>New Mexico State University, United States; <sup>2</sup>Sandia National Laboratories, United States

Towards the goal of enhanced hardware security, this work proposes compact supervisory circuits to perform low-frequency monitoring of a communication SoC. The communication RF output is monitored through an integrated RF envelope detector. The input supply to the transceiver block of the SoC is delivered by an integrated linear voltage regulator with output current monitoring. These two supervisory circuits are inexpensively fabricated in 0.6- $\mu$ m technology. The useful bandwidth of the envelope detector is measured as 1-6 GHz at a supply of 3.3 VDC and quiescent current of 2.65 mA. The linear regulator generates 3.3 VDC using an input of 5 VDC, quiescent current of 1.83 mA, and load current from 1-120 mA. Static and transient load current tests demonstrate linear output current monitoring.

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<sup>1</sup>Mohamed Shehata, <sup>1</sup>Eslam A. Aly, <sup>1</sup>Mostafa B. Alabd, <sup>1,2</sup>Hassan Mostafa

<sup>1</sup>Cairo University, Egypt; <sup>2</sup>Zewail City of Science and Technology, Egypt

Different energy harvesting techniques have gathered the attention of many, due to the huge potential they hold in future technologies. Among these newly emerging techniques are the triboelectric nanogenerators (TENGs). Since 2012, a lot of studies have been pushed towards characterizing and modelling TENGs for the potential they hold in many future applications. TENGs prove very promising as reliable power sources for small, mobile electronic devices, and mobile sensor networks. TENGs are mainly classified in four different fundamental modes, based on their mechanism of operation. In this paper, the attached-electrode contact-mode TENGs are broken down and analytically modelled, providing a systematic framework for the design and analysis of more complicated modes of TENGs in the context of complete systems.

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*William Morell, Ashok Srivastava*

Louisiana State University, United States

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**Chair:** Jose Silva-Martinez, *Texas A&M University*

**Time:** Monday, August 5, 2019, 8:00 - 9:30

**Location:** Quorum I & II

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<sup>1</sup>Chung-Yu Wu, <sup>1</sup>Chi-Kuan Tzeng, <sup>1</sup>Shih-Yun Huang, <sup>2</sup>Fang-Liang Chu, <sup>2</sup>Chuan-Chin Chiao, <sup>3</sup>Yueh-Chun Tsai,

<sup>4</sup>Jun Ohta, <sup>5</sup>Toshiniko Noda

<sup>1</sup>National Chiao Tung University, Taiwan; <sup>2</sup>National Tsing Hua University, Taiwan; <sup>3</sup>A-Neuron Electronic Corp., Taiwan;

<sup>4</sup>Nara Institute of Science Technology, Japan; <sup>5</sup>Toyohashi University of Technology, Japan

A self-photovoltaics-powered CMOS 256-pixel implantable chip with wide image dynamic range and shared electrodes is proposed and fabricated for subretinal prostheses. The infra-red (IR) light is incident only on photovoltaic cells of the chip for power whereas the visible light is mainly incident on pixels for image. The functions of the chip have been successfully validated with both electrical measurement and ex vivo patch clamp experiments with the retinas of Rd1 mice.

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*Masoud Nazari, Kye-Shin Lee*

University of Akron, United States

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*Akanksha Rohit, Yunus Kelestemur, Julian C. Runyon, Savas Kaya*

Ohio University, United States

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*Cory Davis, Alekhya Muthineni, Eugene John*

University of Texas San Antonio, United States

AES is one of the most popular and widely adopted encryption algorithms. The increasing use of AES in severely power constrained devices such as the implantable cardiac devices makes the low power implementation of AES critical. Traditionally, one of the AES core functions, ShiftRows, is accomplished by implementing a series of shift registers. In this paper we propose a new power efficient implementation of AES by introducing a new realization of the ShiftRows operation using muxes. Simulations of these implementations, using 45nm and 90nm technology nodes, yielded respective averages of 13.5% and 10.6% reduction in overall power consumption of AES.

**Session A1L-E: Neural Networks and Neuromorphic Engineering**

**Chair:** Jennifer Blain Christen, *Arizona State University*

**Co-Chair:** Fathi Salem, *Michigan State University*

**Time:** Monday, August 5, 2019, 8:00 - 9:30

**Location:** Salon G & H

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<sup>1</sup>Narumi Yasuhara, <sup>1</sup>Takahiro Natori, <sup>2</sup>Mitsuo Hayashi, <sup>1</sup>Naoyuki Aikawa

<sup>1</sup>Tokyo University of Science, Japan; <sup>2</sup>Hiroshima University, Japan

Drowsiness can reduce working efficiency and result in dozing while driving. It is known that short naps in sleep stage 2 is effective for eliminating drowsiness, so further analysis of sleep stage 2 are required to clarify the relationship between nap length and quality. EEG in sleep stage 2 is characterized by the appearance of a sleep spindle and detection of this sleep spindle is thus required for analysis of this sleep stage. In this paper, we propose a method to detect a sleep spindle in the time domain using a Long Short-Term Memory (LSTM) network.

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*Shadi Sheikhaal, Steven D. Pyle, Soheil Salehi, Ronald F. DeMara*

University of Central Florida, United States

This work aims to improve current neural network models by leveraging the principle that the cortex consists of noisy and imprecise components in order to realize an ultra-low-power stochastic spiking neural circuit that resembles biological neuronal behavior. By utilizing probabilistic spintronics to provide true stochasticity in a compact CMOS-compatible device, an Adaptive Ring Oscillator for as-needed discrete sampling, and a homeostasis mechanism to reduce power consumption, provide biological characteristics, and improve process variation resilience, this subthreshold circuit is able to generate sub-nanosecond spiking behavior with biological characteristics at 200mV, using less than 80nW, along with behavioral robustness to process variation.

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*Sumedha Gandharava Dahl, Robert C. Ivans, Kurtis D. Cantley*

Boise State University, United States

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*Je-Joong Woo, Jong-Moon Choi, Kee-Won Kwon*

Sungkyunkwan University, Korea

We study the kinetics of charging by hot carrier injection (HCI) in CMOS-Compatible floating gate(FG) cell under variety of pulse conditions. The adapted pulse which makes weight update linearly and symmetrically, is generated by adding amount of threshold voltage shifted. To implement the adapted pulse, we propose a 3T1C Metal-Insulator-Metal(MIM) FG with simple yet effective charge sharing scheme. With this scheme we can sample the present threshold voltage and store it in a capacitor. Stored voltage in a capacitor is then coupled to required voltage. Write operation sequence in both cell and arrays is successively simulated in a 180nm CMOS technology. To improve accuracy, we added pre-charging phase which reduced charge sharing error up to by 87.7%.

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*<sup>1</sup>Shang-Kai Wei, <sup>1</sup>Steven D. Gardner, <sup>1</sup>Mohammad R. Haider, <sup>1</sup>J. Iwan D. Alexander, <sup>2</sup>Yehia Massoud*

<sup>1</sup>University of Alabama at Birmingham, United States; <sup>2</sup>Stevens Institute of Technology, United States

With the increase of the number of sensors in an Internet-of-Things (IoT) environment, there is a critical need of in-situ signal processing for local intelligence. This work presents a ring-oscillator based neural network (ONN) for sensor signal processing. A series of 36 ring oscillators are coupled serially and the network performs computations by synchronization. The coupling weights are modulated by sensor inputs which in turn affect the stored memory by indication of synchronization time and frequency of the network. This work studies the effects of synchronization time and frequency of the ONN for different supply voltages, coupling weights and number of oscillating nodes. The 36 oscillator ring neural network scheme has been designed and simulated using 130 nm SiGe Bi-CMOS process. Simulation results show power consumption to be less than 5.6 mW for the entire ONN and pattern recognition based on synchronization frequency and time differences between the training and input patterns.

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**Chair:** Nader Rafla, *Boise State University*

**Time:** Monday, August 5, 2019, 8:00 - 9:30

**Location:** Addison

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*Mahdi Hasanzadeh, Ebadollah Taheri, Mansour Shafaei, Ahmad Patooghy*

University of Central Arkansas, United States

In this paper, we propose an in-field test strategy to make sure that the most important hardware components of a 3D NoC i.e., FIFO buffers and crossbar switches, are up and functioning as expected. Unlike previous schemes, our proposed test strategy runs as a background process and does not interfere with the normal operation of the chip i.e., it uses two always-ON test architectures to minimize the failure detection latency. The testing architectures keep giving feedback to the routing unit of NoC to avoid using failed components for future packets. Our network level evaluations show that the proposed test strategy reduces the number of packets that were previously dropped due to in-field failures of NoC components by 93%. This is achieved with a negligible network delay increase when there are failed components, and zero-increase in the network delay when there is no failed component in the chip. The synthesis results of our Verilog implementation show that the hardware and power consumption overheads of the proposed test architecture are limited to 3.2% and 2.1% respectively.

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*Luka Daoud, Nader Rafla*

Boise State University, United States

Network-on-Chip (NoC) is the communication platform of the data among the processing cores in Multiprocessors System-on-Chip (MPSoC). NoC has become a target to security attacks and by outsourcing design, it can be infected with a malicious Hardware Trojan (HT) to degrades the system performance or leaves a back door for sensitive information leaking. In this paper, we proposed a HT model that applies a denial of service attack by deliberately discarding the data packets that are passing through the infected node creating a black hole in the NoC. It is known as Black Hole Router (BHR) attack. We studied the effect of the BHR attack on the NoC. The power and area overhead of the BHR are analyzed. We studied the effect of the locations of BHRs and their distribution in the network as well. The malicious nodes has very small area and power overhead, 1.98% and 0.74% respectively, with a very strong violent attack.

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*Kaitlin N. Smith, Mitchell A. Thornton*

Southern Methodist University, United States

Quantum computers capable of practical information processing are emerging rapidly. As these devices become more advanced, tools will be needed for converting generalized quantum algorithms into formally-verified forms that are executable on real quantum machines. In this work, a prototype tool is presented that transforms quantum algorithms into executable specifications. Additionally, the tool incorporates formal verification internally with Quantum Multiple-valued Decision Diagrams to confirm that the generated technology-dependent executable is functionally equivalent to the original, technology-independent algorithm. Experimental results are provided that target the Rigetti family of quantum processing units although the tool may also target other architectures such as the IBM machines.

**Session A1L-G: Linear and Nonlinear Circuits and Systems I**

**Chair:** Esteban Tlelo-Cuautle, *INAOE*

**Time:** Monday, August 5, 2019, 8:00 - 9:30

**Location:** Salon I & J

**Analysis of Nonlinear Passive Pinched Hysteresis Generator Circuits** ..... 77

*Rodolfo Kiyama-Armendariz, Isaac Abraham*

Intel Corporation, United States

Hysteresis is a cornerstone of threshold based switching circuits. The idea of pinched hysteresis has taken on a new relevance with the advent of the memory resistor. There are models in literature that employ nonlinear elements paired with passive phase shift to demonstrate pinched hysteresis. This work analyzes the suitability of passive models for demonstrating hysteresis with a representative passive circuit candidate. The computational model employed in this study analyzes lobe symmetry, lobe area, response at zero stimulus, linearity etc. to arrive at its conclusions. The computed results are validated against SPICE simulations with good agreement. This study shows that pinched hysteresis emulators implemented with passive, nonlinear element based phase shift may seem superficially satisfactory but fail analytical inspection.

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*Shervin Erfani*

University of Windsor, Canada

This paper focuses on the analysis of linear time-varying systems by the iterated Laplace transform (ILT). The development of the bi-variate and bifrequency theory for linear circuits and systems are outlined. Both the two-dimensional Laplace transform (2DLT) as well as the ILT are used to characterize linear time-varying causal systems.

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<sup>1,3</sup>Sharath Patil, <sup>1,2</sup>Volodymyr Seliuchenko, <sup>1</sup>Darrell Livezey, <sup>1</sup>Saad Ahmad, <sup>1</sup>Bhanu Singh, *Martin Margala*

<sup>1</sup>Melexis Inc., United States; <sup>2</sup>The Vrije Universiteit Brussel, Belgium; <sup>3</sup>University of Massachusetts Lowell, United States

Lidars are gaining popularity in the automotive domain especially in the field of autonomous driving systems. Development of multi-channel monolithic Lidars could reduce the system cost and size for better integration into automobile components. Since Lidars work on the principle of time of flight, an important function of the Lidar system is to precisely detect the time of arrival of the received light pulse. A method is being proposed in this paper to detect the peak location in the received Lidar signal using differentiation. With a single chip solution, the proposed method can improve the footprint of the analog signal chain by 30% thereby saving the overall chip area.

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<sup>1</sup>Aslihan Kartci, <sup>1</sup>Norbert Herencsar, <sup>2</sup>Oguzhan Cicekoglu, <sup>2</sup>Bilgin Metin

<sup>1</sup>Brno University of Technology, Czech Rep.; <sup>2</sup>Bogazici University, Turkey

The design trend in the analog CMOS signal processing technology is towards the MOS-only approach. Using this technique, this work presents three new core topologies realizing floating positive or negative inductance simulators. The positive inductance simulator (PIS) is investigated as both integer- and fractional-order element. For illustration purpose, the behavior of the fractional-order PIS was tested via implementation in RLC ladder prototype of voltage-mode (VM) high-pass filter with various orders; particularly of orders 2, 2.5, and 3. The performance of the integer-order PIS was tested in third-order VM elliptic low-pass filter at very high frequencies. Theoretical results are verified by LTSPICE simulations using BSIM3 1  $\mu\text{m}$  technology transistor parameters.

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Salih Ergün

ERGTECH Research Center, Switzerland

A novel cross-coupled bipolar transistor-based non-autonomous chaotic oscillator is proposed. The derivation methodology of this novel chaotic oscillator is based on integrating two of existing chaotic oscillators symmetrically and employing a differential-pair stage. Simulation and experimental results, verifying the feasibility and the correct operation of the circuit are also given.

**Session A2P-H: Data Converters**

**Chair:** Qiyuan Liu, *Qualcomm*

**Time:** Monday, August 5, 2019, 11:30 - 12:30

**Location:** Salon F

**Energy-Efficient and Area-Efficient Switching Schemes for SAR ADCs** ..... 97

<sup>1</sup>Meysam Akbari, <sup>2</sup>Masoud Nazari, <sup>1</sup>Omid Hashemipour, <sup>2</sup>Kye-Shin Lee

<sup>1</sup>Shahid Beheshti University, Iran; <sup>2</sup>University of Akron, United States

In this paper, Two energy-efficient switching schemes based on close-loop charge recycling method are presented. In each transition, required capacitors with an initial charge will be connected to the capacitor arrays, while the bottom plates of all capacitors are connected to the same reference voltage. This method does not let capacitors to drain any DC current from the reference voltage, and existing charge on the capacitors will be shared on their top plates to provide the required threshold voltage. Two proposed schemes are simulated in MATLAB and the results show a 100% transitional energy saving during bits generation for both proposed techniques, without considering reset phase. In addition, the first and the second schemes show 25% and 50% capacitor area reductions in comparison with the conventional scheme, respectively.

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Yuan Mei, Shaorui Li

Brookhaven National Lab, United States

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Sanjeev Tannirkulam Chandrasekaran, Arindam Sanyal

University at Buffalo, United States

This paper presents an asynchronous current controlled oscillator (VCO) based analog-to-time converter (ATC). The proposed ATC uses a ring oscillator as phase-domain integrator and quantizer. A negative feedback loop using a current steering digital-to-analog converter (DAC) relaxes linearity requirement of the CCO. The ATC output is a multi-phase pulse-width modulated (PWM) signal which can be used with continuous-time digital signal processing systems. The proposed ATC is simulated in a 65nm CMOS process and has a 59.2dB SNDR with an input-referred noise of 42.6nV/Hz over 500kHz bandwidth while consuming 11uW from a 0.5V power supply.

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Shuai Li, Jianguo Diao, Yimin Wu, Fan Ye, Junyan Ren

Fudan University, China

This paper proposes a 20MHz bandwidth time-interleaved based band-pass noise shaping SAR, which is especially suitable for high frequency ultrasound imaging systems. A high power efficiency op amp sharing switched-capacitor filter is employed and the total amount of capacitance is thus reduced by about 4 times compared with fully-passive noise shaping SAR ADCs.



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*Hossein Ghafarian, Helia Ordouei, Friedel Gerfers*

Technische Universität Berlin, Germany

This paper studies various impedance calibration techniques applied on a 10-bit source series terminated digital-to-analog converter (DAC) implemented in a 22 nm FDSOI process. The body biasing and parallel branching technique, both take advantages of the FDSOI technology by using the large backgate voltage tuning. To verify the proposed technique, an analytical model of the SST driver is developed and the impedance tuning range of each technique is proven to cover over the full 3 sigma process and -40 °C to 80°C temperature range. It turns out, that the body biasing technique just covers one third of the process and temperature variations, whereas parallel branching calibrates for all corners at cost of increased power consumption. The obtained simulation results of the complete SST driver using the proposed impedance calibration meet the stringent return loss specifications of the automotive 10GBase-T1 Ethernet standard across 3 sigma process corner and -40°C to 80°C temperature range.

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*Alok Keshattiwar, Bibhu Datta Sahoo*

Indian Institute of Technology Kharagpur, India

This paper proposes a systematic way of sizing capacitors in a split-Successive Approximation Register (SAR) analog-to-digital converter (ADC) so as to achieve optimum redundancy that can take care of comparator noise, comparator offset, and digital-to-analog converter (DAC) finite settling. The capacitor sizing technique to optimally distribute redundancy across all bit-cycling phases, has been demonstrated with system-level simulation using MATLAB for split-SAR with one, two, and three bridge-capacitors. The proposed technique of sizing capacitors to achieve optimum redundancy at every bit-cycling step can be easily extended for split-SAR with arbitrary number of bridge-capacitors.

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*Xiaochen Tang, Qisong Hu, Wei Tang*

New Mexico State University, United States

We present an Analog to Digital Feature Converter system based on oversampling modulators. The system consists of a Delta Sigma Modulator, two Delta Modulator, and one Second order Delta Modulator in parallel. The goal of Analog to Digital Feature Converter is to extract the waveform features from the analog signal during analog to digital conversion to save system power. We demonstrated this system in an example application of electrocardiogram (ECG) delineation with a counting based feature extraction algorithm. Compared the conventional ECG delineation methods using wavelet transform, the proposed method has much lower power consumption for data conversion and computation.

**Session A2P-J: Amplifiers and Filters**

**Chair:** Paul Furth, *New Mexico State University*

**Time:** Monday, August 5, 2019, 11:30 - 12:30

**Location:** Salon F

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*James K. Mellott, Eric Monahan, Vikas Vinayaka, Sachin P. Namboodiri, Angsuman Roy, R. Jacob Baker*

University of Nevada, Las Vegas, United States

A low cost, low power substitute for expensive, high power high-speed analog-to-digital converters (ADCs) in some situations is presented. This circuit is called a variable fast transient digitizer (VFTD). This paper provides an overview of the design and measured test results. The VFTD is designed to sample a high-speed analog input signal and later reconstruct the captured signal at a much slower rate, for example, around three orders of magnitude. This approach eliminates quantization error in the captured signal. Further, this approach enables the use of slow, low cost, analog-to-digital converters such as those found in microcontrollers.

**Multi-Stage Current-Steering Amplifier Design based on Extended  $g_m/I_D$  Methodology** ..... 129

*Jacob Atkinson, Amin Aghighi, Stuart Anderson, Anthony Bailey, Mitchel Crane, Armin Tajalli*

University of Utah, United States

A methodology to optimally design multi-stage current-steering CMOS amplifiers is described. The optimal device operating conditions and sizes are directly calculated from design constraints, such as desired voltage gain, and frequency bandwidth. The proposed design algorithm is based on an analytical approach, which extends the conventional  $g_m/I_D$  methodology. Examples are provided to show effectiveness of the proposed approach.

**A 0.65 V, 65-nm CMOS Technology 4th-Order Tunable Bandpass Filter for Acoustic Applications** ..... N/A

*Ningcheng Gaoding, Jean-François Bousquet*  
Dalhousie University, Canada

This paper presents a nano-power 4th order active biquad bandpass filter (BPF) in CMOS 65-nm technology. The proposed second-order BPF is based on a Gm-C topology and utilizes a PMOS differential pair. Through cascading two of these elements, a fourth-order BPF can be obtained. The center frequency of the proposed BPF can be tunable from 77Hz to 26kHz by using a current source to control it, with a quality factor approximately equals to 5. For the nominal center frequency of 1.3kHz and a quality factor of 5, the dynamic range of this design is 42.3dB for 0.62% total harmonic distortion (THD). The proposed filter shows great potential for use in acoustic and biomedical applications with a very low power equal to 7.47nW. At these nominal settings, the proposed biquad BPF achieves an excellent figure of merit (FOM) at  $0.22 \times 10^{-13}$ , as compared to existing state-of-the-art.

**A Tunable Bandstop Filter based on Source Follower** ..... 137

*Fatima T. Almutairi, Aydin I. Karsilayan*  
Texas A&M University, United States

A tunable bandstop filter based on source follower is presented. The filter is designed using a source follower architecture with partial positive feedback and feed-forward paths using a 180 nm CMOS technology. The filter consumes about 1 mW from a 1.8V power supply, and it is designed to have 1.5GHz center frequency with 500 MHz bandwidth and 92 dB attenuation. The filter achieves 10 dBm IIP3 for two tones at 1.495GHz and 1.505 GHz.

**A Ring Amplifier based Current Feedback Continuous Time PGA for High Frequency Ultrasound Applications** ..... 141

*Yimin Wu, Jingchao Lan, Shuai Li, Fan Ye, Junyan Ren*  
Fudan University, China

This paper presents a ring amplifier based wideband continuous time (CT) programmable gain amplifier (PGA) with high power and area efficiency, which is essential for high frequency ultrasound applications. A new amplifying strategy for driving time-interleaved SAR ADC (TI-SAR) is also proposed to address the stability problem of a ring amplifier. The prototype is designed in 0.18um BCD high-voltage process as part of a pitch-size-matched ultrasound transceiver. The simulation result shows that the PGA achieves 10-40dB gain range and 40MHz bandwidth. The high linearity and low noise performance is also guaranteed with only 4.2mW power consumption.

**Session A2P-K: Sensors and References**

**Chair:** *New Mexico State University*

**Time:** Monday, August 5, 2019, 11:30 - 12:30

**Location:** Salon F

**A Voltage Stabilization Method of Charge Pump based on 4-Phase Clock Generator** ..... 145

*Botao Xiong, Yudong He, Tao Cao, Feixiang Huo, Xinbing Ma, Youjiang Liu*  
China Academy of Engineering Physics, China

A four-phase clock generator based on hybrid digital pulse width modulator (DPWM) is proposed, which provides adaptive 4-phase clock for charge pump converting low input voltage (3.3V) to the high output voltage (110V). The proposed adaptive 4-phase clock algorithm not only stabilizes the output voltage of charge pump but also render the charge pump immune to PVT variations and dynamic loads. On the other hand, the dead time scheme cuts off the reverse current so that the power efficiency is improved by 5%. The layout simulations demonstrate that the 4-phase clock generator improves the power efficiency and robustness of charge pump (17.6mm<sup>2</sup>, 150mW) with negligible cost (0.45 mm<sup>2</sup>, 35mW).

**A New Voltage Reference based on Threshold Voltages Summation of CMOS Transistors** ..... 149

*W.A. Amaral*  
University of Brasilia, Brazil

The necessity of voltage references with low temperature dependence is notable in analog and mixed signal circuit design. These circuits are normally designed using the base-to-emitter voltage (VBE) of bipolar junction transistors (BJT). Although this is the most widespread technique, different solutions can be found in literature. In this paper a new topology of voltage reference with low temperature dependence is shown. The design is based on the summation of two voltages; one with positive temperature dependence and another with negative temperature dependence, both obtained using the threshold voltage (Vth) of MOS transistors. The circuit was designed using TSMC 0.13um and achieved 16ppm/C in a range of 0C to 100C.

**A Temperature Sensing System with Encrypted Readout using Analog Circuits** ..... 152

<sup>1</sup>Ava Hedayatipour, <sup>1</sup>Kendra Anderson, <sup>1</sup>Shaghayegh Aslanzadeh, <sup>1</sup>Daniel Brown,

<sup>2</sup>Donatello Materassi, <sup>1</sup>Nicole McFarlane

<sup>1</sup>University of Tennessee, United States; <sup>2</sup>University of Minnesota, United States

Low power integrated compact sensors for applications such as IoT and arrayed bio-medical sensors are essential for today's technology. However, security is not incorporated in these sensors and are typically added after the implementation using digital hardware or software. In this paper, we demonstrate a temperature to time sensing system with an encryption process in real-time analog circuitry and minimal processing power. The encryption takes advantage of the chaotic Lorenz attractor system. The temperature sensor, implemented in 130 nm technology, consumes 195 nW with 0.5 V power supply. The encryption module is simulated in Simulink and implemented at the board level using discrete components on a printed circuit board. Experimental results show that the envisioned chaotic system is capable of encrypting and decrypting the digital temperature signal.

**An Oscillator based Energy Efficient Computing Architecture for Smart Sensors** ..... 156

<sup>1</sup>Ting Zhang, <sup>1</sup>Ruikuan Lu, <sup>1</sup>Mohammad Haider, <sup>1</sup>J. Iwan D. Alexander, <sup>2</sup>Yehia Massoud

<sup>1</sup>University of Alabama at Birmingham, United States; <sup>2</sup>Stevens Institute of Technology, United States

With the advent of Internet-of-Things (IoT), there is a growing need of large array sensors with higher temporal and spatial resolutions. However, the immense volume of sensor data creates a huge burden on the data center for real-time signal processing and data mining. To alleviate this problem, an oscillatory neural network (ONN) based energy-efficient local computing scheme is proposed in this work. This paper shows a hierarchical associative memory (AM) architecture using oscillator synchronization and stable cluster state for pattern recognition and how such architecture can be efficiently used in local processing units. The ONN based AM architecture can be easily achieved using CMOS technology on local hardware units. Unlike cloud computing system, this architecture provides an offline approach and performs sensing and data processing efficiently on the local device without connecting to the Internet.

**Session A2P-L: Modeling, Optimization, and Analysis**

**Chair:** Qiyuan Liu, *Qualcomm*

**Time:** Monday, August 5, 2019, 11:30 - 12:30

**Location:** Salon F

**Comparative Analysis of Circuit Performance for Photocurrent Estimation** ..... 160

Paul E. Stevenson, Jennifer M. Blain Christen

Arizona State University, United States

In this work, we compare the benefits of two different circuit methods of estimating slowly changing photocurrent. Simulation and silicon results are presented.

**Impact and Modeling of Möbius Connection in the Rotary Traveling Wave Oscillator Performance** ..... N/A

<sup>1</sup>Carlos Alberto Sanabria Díaz, <sup>1</sup>Mónico Linares Aranda, <sup>2</sup>Rogelio M. Higuera González,

<sup>1</sup>F. Javier De la Hidalga Wade

<sup>1</sup>INAOE, Mexico; <sup>2</sup>Tecnológico de Estudios Superiores de Ixtapaluca, Mexico

The new interest in high frequency applications such as 5G and mmWaves have increased the design requirement for the integrated circuits, specifically for the signal generation and base-band processing stages. The Rotary Traveling Wave Oscillator (RTWO) has been proposed not only as clock distribution network when is used in arrays (ROAs), but also for high data rate applications and communication systems. The most complex discontinuity of the RTWO resonator is the Möbius connection; this discontinuity is generally manufactured using angles of 90° or 45°, different metal levels and stacks of intermetallic connections (vias). In this work we analyze and model the 45° Möbius connection for different geometrical configurations and technologies.

**On Sensitivity of Bias Operation Point in Transistors with Moderate Inversion** ..... 168

<sup>1</sup>I.M. Filanovsky, <sup>2</sup>L.B. Oliveira

<sup>1</sup>University of Alberta, Canada; <sup>2</sup>Universidade Nova de Lisboa, Portugal

The paper analyses sensitivity, with respect to threshold voltage, of bias operation point in the analog circuits using moderate inversion. It is shown that this regime is highly sensitive with respect to the threshold voltage variation. Such high sensitivity imposes unrealistic requirements on the threshold voltage tolerances, so that it is practically impossible to design an amplifier with moderate inversion in the stages without adaptable or tunable threshold voltage. It is also shown that, as a result of this mode of inversion, some important design metrics (cancelling of the third order distortion) are unrealizable.

**A Low-Power Single Comparator Solution for Window Crossing Detection in Signal Activity Monitoring for Sensor Interface Systems** ..... N/A

*Priya V, Murali K. Rajendran, Gajendranath Chowdary*  
Indian Institute of Technology Hyderabad, India

A novel Window Crossing Detector Circuit (WCDC) which can sense when the absolute difference between two signals exceeds a predefined threshold is presented. The circuit finds its applications as activity detector in a wide range of state-of-the-art systems like sensor interface circuitry and control systems. The circuit is capable of detecting excursions of the difference between the input signals in both the positive and negative directions. WCDC consists of a single differential amplifier and a pair of common source amplifier stages. The proposed design saves power and area as compared to the conventional architectures. The WCDC is designed in 180 nm CMOS technology and occupies an on-chip area of 0.008 mm<sup>2</sup>.

**Study of Strategies for Circuit Optimization** ..... N/A

*Alexander Zemliak*  
Autonomous University of Puebla, Mexico

The process of analog circuit optimization is mathematically defined as a controllable dynamic system. In this context the minimization of the processor time of designing can be formulated as a problem of time minimization for transitional process of dynamic system. In order to analyze the properties of such a system, it is proposed to use the concept of Lyapunov function of dynamic system. Using this function and its time derivative, the special functions have been built that allow us to predict the total processor time for circuit optimization by analyzing the initial interval of the optimization process. Numerical results indicate the possibility of predicting the processor time of different strategies for circuit optimization.

**A Review on Negative Capacitance based Transistors** ..... 180

*Johnathan Bacharach, Muhammad S. Ullah, Emadelden Fouad*  
Florida Polytechnic University, United States

Continuous scaling of transistor dimensions to satisfy the increasing demands for higher performance and energy efficiency over the last 50 years is leading the conventional field effect transistors (FETs) to their fundamental material and physical limits. Further improvement of transistor operation and reliability will require new technology and device structure like negative capacitance based transistor. Besides, the roadmap for silicon device technology is approaching the point, where radical material alternatives must be introduced. Negative capacitance based conventional transistor that is often viewed as an adverse effect of short channel lengths in the conventional metal oxide field effect transistors (MOSFETs) has emerged as a promising current injection mechanism to allow the reduction of operating voltage beyond the capabilities of the MOSFET technology. In this paper includes a review summarizing the progresses in the development of the negative capacitance technology, and the experimentally observed performances of different transistors.

**Remote FPGA Lab for ZYNQ and Virtex-7 Kits** ..... 185

<sup>1</sup>Abd El-Rahman Mohsen, <sup>2</sup>Mohamed Youssef GadAlrab, <sup>2</sup>Zeina elhaya Mahmoud, <sup>1</sup>Gameel Alshaer,  
<sup>1</sup>Mahmoud Asy, <sup>1,2</sup>Hassan Mostafa  
<sup>1</sup>Cairo University, Egypt; <sup>2</sup>Zewail City of Science and Technology, Egypt; <sup>3</sup>Alexandria University, Egypt

This paper proposes a remotely programmable and interactive ZYNQ and Virtex-7 FPGA (Field Programmable Gate Array) Lab for testing and implementing arbitrary hardware circuit designs on real hardware. The online virtual lab facilitates the use of FPGA Boards in simple steps and provides graphical and command line interface to control and monitor FPGA signals in real time. The remote lab provides a scheduling system and allows multiple concurrent remote users. The remote interaction method doesn't depend on the type of the device; so it can be scaled to include different devices. The required hardware and software of the remote laboratory is developed, implemented and tested by the undergraduate and graduate students at Cairo University in Egypt.

**Session A2P-M: Image/Video Processing**

**Chair:** *Qualcomm*

**Time:** Monday, August 5, 2019, 11:30 - 12:30

**Location:** Salon F

**Improvement of Low-Light Image by Convolutional Neural Network** ..... 189

*Manbae Kim*  
Kangwon National University, Korea

Many researches have been carried out for enhancing low-light images over the past decades. One of the methods is Retinex theory, where reflectance component is recovered and illumination component is attenuated. Recently, hand-crafted approaches for low-light enhancement have been replaced by artificial neural networks. This paper presents a convolutional neural network that can replace the Retinex-based low-light enhancement method. Experiments carried out on 120 low-light images validated the feasibility of the replacement by producing satisfactory reflectance images.

**Linear Filters for Image Energy** ..... 193

*Jian-ao Lian*

Prairie View A&M University, United States

Four families of new matrix linear filters are established and being used for the approximation to directional derivatives. These filters are also used for representations of image energy, which, in turn, are used for representing image edges. The first three families are for approximations of first order digital directional derivatives, while the fourth family is for the approximations to the second order digital directional derivatives. Examples are demonstrated.

**A Photo-Based Mobile Crowdsourcing Framework for Event Reporting** ..... 198

<sup>1,2</sup>*Aymen Hamrouni, <sup>2</sup>Hakim Ghazzai, <sup>1</sup>Mounir Frikha, <sup>2</sup>Yehia Massoud*

<sup>1</sup>University of Carthage, Tunisia; <sup>2</sup>Stevens Institute of Technology, United States

Mobile Crowdsourcing (MCS) photo-based is an arising field of interest and a trending topic in the domain of ubiquitous computing. It has recently drawn substantial attention of the smart cities and urban computing communities. In fact, the built-in cameras of mobile devices are becoming the most common way for visual logging techniques in our daily lives. MCS photo-based frameworks collect photos in a distributed way in which a large number of contributors upload photos whenever and wherever it is suitable. This inevitably leads to evolving picture streams which possibly contain misleading and redundant information that affects the task result. In order to overcome these issues, we develop, in this paper, a solution for selecting highly relevant data from an evolving picture stream and ensuring correct submission. Simulation results indicate that the implemented framework can effectively reduce false submissions and select a subset with high utility coverage with low redundancy ratio from the streaming data.

**Data Augmentation for Face Recognition System Implemented in Multiple Transform Domains** ..... 203

*Ramy C.G. Chehata, Wasfy B. Mikhael*

University of Central Florida, United States

A face recognition system which represents each of the augmented facial images as a superposition of the dominant components in two transform domains is proposed. Each face in the spatial domain is divided into horizontal, vertical halves and diagonal format. These partitions are concatenated to generate four more faces per subject in any database used. All images are first preprocessed then compressed using two different domains. The Discrete Wavelet Transform (DWT) and the Discrete Cosine Transform (DCT). Accordingly, each face will have two feature matrices. A voting scheme is used to define ground truth identity. The performance of the proposed system is evaluated using k-fold cross validation of ORL, Yale and FERET databases. Sample results are presented. The proposed technique achieves higher recognition rates while retaining 44% savings in storage recently reported.

**Session A2P-N: Digital Electronics and Trust**

**Chair:** *Qualcomm*

**Time:** Monday, August 5, 2019, 11:30 - 12:30

**Location:** Salon F

**Implementation of LMS Adaptive Filter Algorithm based on FPGA** ..... 207

*Andrew Gohn, Joonwan Kim*

LeTourneau University, United States

A LMS (Least Mean Square) algorithm used as an adaptive noise canceller has been implemented on an Artix 7 FPGA (Field Programmable Gate Array) board. The FPGA is used for this research due to its advantages of real-time processing and pipelining which are not possible with other implementation boards. The purpose of implementing the LMS algorithm is to create a noise canceling device that removes noise from the input to achieve the appropriate output. Noise cancellation devices are needed for many environments and can be used to reduce the noise added to speech in airplanes, helicopters, and cars.

**A Novel Design Gate based Low-Cost Configurable RO PUF using Reversible Logic** ..... 211

<sup>1,2</sup>*Bappaditya Dey, Kasem Khalil, Ashok Kumar, Magdy Bayoumi*

<sup>1</sup>imec, Belgium; <sup>2</sup>University of Louisiana at Lafayette, United States

A Physical Unclonable Function (PUF) is often used to uniquely identify an integrated circuit by extracting its internal random differences using so-called Challenge Response Pairs (CRPs). On the other side, It has been realized that quantum computing is one of the latest technologies using reversible logic. It is observed that increasing growth of transistor density, power consumption will reach their limits in conventional technologies. In conventional Circuits, during the logic operations, bits of information is erased resulting dissipation of energy insignificant amount. Thus, if Circuits are designed so that information bits can be preserved, the power use can be reduced. We can use reversible logic technology for minimizing the power consumption, heat dissipation, increasing speed etc. In this paper, we propose the reversible logic design for an existing XOR Gate based Low- Cost Configurable RO PUF structure based on Feynman gate as a reversible logic block. A comparative analysis between classical and quantum logic function is also given on various parameters along with limitations of conventional computing. The proposed approach is implemented using VHDL on Xilinx-7 FPGA.

**Pulse Broadening in Combinational Circuits with Standard Logic Cell Synthesis** ..... 215

<sup>1</sup>Semiu A. Olowogemo, <sup>1</sup>William H. Robinson, <sup>2</sup>Ahmed Yiwere, <sup>2</sup>Ebenezer Tachie-Menson,

<sup>2</sup>Daniel B. Limbrick, <sup>1</sup>Bor-Tyng Lin

<sup>1</sup>Vanderbilt University, United States; <sup>2</sup>North Carolina A&T State University, United States

Technology scaling improves the power, area, and speed of an electronic design, but the reliability of newer technologies is impacted by the presence of radiation-induced transients; these transients are more pronounced in newer technologies. In the presence of variations due to process corners (P), operating voltage (V), and temperature (T), a transient pulse with no serious threat, which would be masked electrically, traverses more gates towards a storage element due to pulse broadening. In this paper, the transient pulses that initially pose no significant threat are simulated with PVT variations in arithmetic circuits from the EPFL benchmark suite to investigate the effect of variations on vulnerable gates. The results show that the variation enhances the transient pulses with no serious threat and causes pulse broadening from the locations of vulnerable gates. A mitigation approach is applied on the vulnerable gates of the sine circuit, and the masking capability during worst-case analysis improves on average by 76.5% for process corner variation, 85.5% for operating voltage variation, and 84.4% for temperature variation.

**Secure Interface Architecture for Charge Trap Transistor (CTT) based EEPROM** ..... 219

Vishal Reddy Banala, Cheng Hao, Chris Hutchens

Oklahoma State University, United States

Cryptographic attacks and memory observability among DRAM or PROM have drawn researcher's attention. C. Kothandaraman et al. [1] have proposed a secure memory element using charge-trap based transistor for a potential memory application. Our work presents an on-chip interface architecture between CPU and secure EEPROM for control and data communication. This architecture allows the secure EEPROM to be embedded with the processing unit preventing interface eavesdropping so that encryption keys can be accessed locally and securely. It is also designed to overcome the cold-boot attacks and side channel attacks employing on-chip implementation and parallel data communication. The design is implemented in VHDL and validated with secure EEPROM model. The synthesis and simulation results of the design are presented.

**Using Carry Increment Adders to Enhance Energy Savings with Spanning-Tree Adder Structures** ..... 223

Kyle Price, James E. Stine

Oklahoma State University, United States

Hybrid adders have provided innovation in the field of digital arithmetic. These designs take the best parts of multiple implementations and improve results in terms of area, delay, or power. This work implements a 64-bit hybrid adder using a spanning tree structure with the carry-increment algorithm. Synthesis results are obtained for 45nm technology and show promising data when compared with an existing hybrid design.

**Novel 3D Monotonic Characterization of Standard Cell Liberty File Attributes w.r.t ASIC Tool Flow** ..... 227

<sup>1</sup>Lalitha Mohana Kalyani Garimella, <sup>2</sup>Sri Raga Sudha Garimella

<sup>1</sup>Intel Corporation, United States; <sup>2</sup>New Mexico State University, United States

Shrinking of process nodes is declining and demand is increasing for design perfection to progress power, performance, area (PPA) enhancement. Standard library cells are basic building blocks for ASIC design PPA. This paper presents first of its kind research to bridge the gap between conventional STD cell monotonic characterization and resulted STD cell liberty file (.lib file) attributes usage with respect to ASIC tool cost function in a ASIC design and proposes a novel 3 dimensional (3D) monotonic characterization method for PPA boosting. An algorithm for identifying non-3D-monotonic cells in a given library is described. Post-route, post-extracted, primetime results prove that eliminating those cells give excellent PPA gain. Summary of results by replacing non-3d-monotonic cells with cells fitting 3D-monotonic characterization for further PPA improvement are provided with no disadvantages.

**Memristor-Based AES Key Generation for Low Power IoT Hardware Security Modules** ..... 231

<sup>1</sup>Hanan Rady, <sup>2</sup>Hagar Hossam, <sup>1</sup>M. Sameh Saied, <sup>3</sup>Hassan Mostafa

<sup>1</sup>Cairo University, Egypt; <sup>2</sup>Ains-Shams University, Egypt; <sup>3</sup>Zewail City of Science and Technology, Egypt

Security of Internet of Things (IoT) needs devices and algorithms that offer ultra-low power consumption and a long lifespan, alongside strong immunity against attacks, lower chip area, and acceptable throughput. Hardware security using nanoelectronic technologies shows promise for the area and energy-efficient implementations in IoT. Owing to the recent advances in Memristor as a potential building block for future hardware, it becomes a vital issue to study the role that Memristor will play in hardware security. This work presents a hardware security module for low power IoT security implementations. The proposed module depends on Memristor-based AES key generation relying mainly on the uniqueness of Memristor devices due to fabrication process variations. In addition to taking into consideration the strength properties and great features of Time-based ADC and AES cryptographic algorithm, the proposed hardware security module could meet the needs of modern technology such as secure communication between IoT embedded devices.

## Session A2P-P: System Architectures and Embedded Systems I

**Chair:** Fakhreddine Ghaffari, *University of Paris Seine*

**Time:** Monday, August 5, 2019, 11:30 - 12:30

**Location:** Salon F

### **System Design Methodologies for Safety and Security of Future Wireless Technologies in Aviation** ..... 235

*Pranay Bhardwaj, Carla Purdy*

University of Cincinnati, United States

Automatic Dependent Surveillance-Broadcast (ADS-B) and the Global Navigation Satellite System (GNSS) are already transforming communication for airplanes and ground-based stations. This unsecured aviation communication system raises many safety and security concerns. Kocher and others have shown that security is best built into system design itself, not added later. We reconsider ADS-B security issues from scratch. We use the Universal Modeling Language (UML) to specify security and safety weaknesses and possible solutions. Our eventual goal is to develop a formal specification for ADS-B model-checking. Our strategy can also be extended to other applications, such as the CANBUS.

### **Variable Record Table: A Run-Time Solution for Mitigating Buffer Overflow Attack** ..... 239

*Love Kumar Sah, Sheikh Ariful Islam, Srinivas Katkooi*

University of South Florida, United States

In this paper, we present a novel approach to extract base and bound information of variable during run-time. We instrument frame pointer and functions registers to decode the layout of stack and heap. We store this information in a table called Variable Record Table (VRT). Then, we utilize VRT information to detect any out-of-bound access in the program. We modified SimpleScalar/PISA simulator to extract variables space using 6 benchmark suites of MiBench to maintain VRT. We tested 290 small C programs (MIT corpus suite) having 22 different buffer overflow vulnerabilities in stack and heap. Experimental results show that our approach can detect attack with zero instruction overhead, and the memory space requirement up to 13KB to maintain VRT.

### **Empirical Analysis of Fixed Point Precision Quantization of CNNs** ..... 243

*Anaam Ansari, Tokunbo Ogunfunmi*

Santa Clara University, United States

Image classification, speech processing, autonomous driving, and medical diagnosis have made Convolutional Neural Networks (CNN) mainstream. Implementing these deep and complex networks in hardware is challenging. In this paper, we use quantization on the output of each layer for AlexNet and VGGNET16 to analyze its effect on accuracy. We use Signal to Noise Quantization Ratio (SQNR) to empirically determine the integer length (IL) as well as the fractional length (FL) for the fixed-point precision. We can report that in addition to the small word length, the accuracy is highly dependent on the integer length as well as the fractional length.

### **Self-Decompressing FPGA Bitstreams** ..... 247

*Shenghou Ma, Paul Ampadu*

Virginia Polytechnic Institute and State University, United States

SRAM based FPGAs (field programmable gate arrays) are volatile devices, and need to reload its configuration (bitstream) every time after power up. Bitstream compression is one of the major method to reduce the cost of storing the configuration storage and speed up configuration. This paper drew inspiration from self-extracting archive, and utilizes the self partial reconfiguration capabilities of modern FPGAs to create a self-decompressing FPGA bitstreams so that the decompression engine is located inside the compressed bitstream itself.

## Session A3L-B: Wireline Communication Circuits

**Chair:** Samuel Palermo, *Texas A&M University*

**Time:** Monday, August 5, 2019, 13:30 - 15:00

**Location:** Preston Trail I & II

### **A 4-40 Gb/s PAM-4 Transmitter with a Hybrid Driver in 65 nm CMOS Technology** ..... N/A

<sup>1</sup>Dengjie Wang, <sup>1</sup>Hong Chen, <sup>1</sup>Wenhuan Luan, <sup>1</sup>Xin Lin, <sup>2</sup>Fangxu Lv, <sup>1</sup>Ziqiang Wang, <sup>1</sup>Hanjun Jiang,

<sup>1</sup>Chun Zhang, <sup>1</sup>Zhihua Wang

<sup>1</sup>Tsinghua University, China; <sup>2</sup>Air Force Engineering University, China

This paper presents a 4-40 Gb/s PAM-4 transmitter using a novel hybrid driver. Different from conventional current-mode (CM) drivers with poor linearity and source-series terminated (SST) drivers with limited differential output swing, the proposed hybrid driver delivers a differential output swing exceeding the supply voltage with high linearity using a combination structure of the CM and SST driver. In addition, a 4-40 Gb/s quarter-rate transmitter with one-tap feedforward equalization is designed in 65nm CMOS technology using the hybrid driver, yielding a 1.8V differential peak-to-peak output swing at 1.2 V supply voltage with a 96.4% ratio of level mismatch.

**A 5.4 Gbps Protocol based CMOS Limiting ReDriver for Type-C Applications** ..... 255

*Siamak Delshadpour, Cor Speelman*  
NXP Semiconductors, United States

PCB traces have high-frequency losses due to skin effect and dielectric losses which result in inter symbol interference (ISI), as the signal passes through cable and PCB traces. A limiting ReDriver, which acts as a repeater and includes a continuous time equalizer, removes the ISI which results in a longer signal reach. A CMOS limiting ReDriver channel operating up to 5.4Gbps and programmable pre-emphasis and de-emphasis to be compliant with some of the standards like display port (DP) and USB, is presented. It has programmable peaking gain up to 12dB at 2.7GHz with 1.5dB steps to compensate for the channel loss and a programmable output swing control of 400mVpp up to 1100mVppd. It has been implemented in 0.14 um CMOS technology and consumes 37.5mA to 55.5mA per channel from a 1.8V supply, depending on selected output swing and emphasis level. It uses common mode keeper, far-end termination detector and incoming squelch detector to work inside a protocol based ReDriver chip.

**Digital RF-Over-Fiber Links based on Continuous-Time Delta-Sigma Modulation** ..... 259

*Xi Gao, Jifu Liang, Soumyajit Mandal*  
Case Western Reserve University, United States

Transmission of digitized radio frequency (RF) signals over optical fiber links is attractive because of low loss, extremely broad bandwidth, and robustness to external RF interference (RFI). However, realizing these advantages requires highspeed digitizers with high resolution and low power consumption. In this paper, a fourth-order continuous-time delta-sigma modulator (CT-DSM) with one-bit digital-to-analog converter (DAC) is proposed for this purpose. An assistant circuit is implemented to steer currents from the feedback DAC and input resistor to idealize the performance of the operational amplifier (op-amp) in the first integrator stage. The first op-amp also uses chopping to reduce flicker noise and offset. The proposed modulator is designed in the TSMC 180 nm CMOS process. Simulation results show a maximum signal-to-noise-and-distortion ratio (SNDR) of 89.3 dB for a sample frequency of 100 MHz, a chopping frequency of 50 MHz, and an oversampling ratio (OSR) of 100, resulting in a Walden figure of merit (FoM) of 360 fJ/bit.

**A Pre-Skewed Bi-Directional Gated Delay Line Bang-Bang Frequency Detector with Applications in 10 Gbps Serial Link Frequency-Locking** ..... 263

*Yue Li, Fei Yuan*  
Ryerson University, Canada

This paper proposes a pre-skewed bi-directional gated delay line (BDGDL) bang-bang frequency detector (BBFD) with applications in frequency-locking of 10 Gbps (giga-bits-per-second) serial links. Bang-bang frequency detection is performed using a pair of BDGDLs that digitize the logic-1 pulse of receiver oscillator and a reference clock. A redundant successive approximation register (SAR) driven by the output of the BBFD is used to generate the frequency control word (FCW) of the digitally controlled oscillator (DCO) of the receiver. A frequency detection decision can be made in only 4 cycles of the reference clock. The frequency error of the ADFLL utilizing the proposed BBFD is analyzed. The ADFLL is designed in a TSMC 65 nm 1.2 V CMOS and tested with a 5 GHz reference clock. Simulation results show the ADFLL achieves frequency lock in less than 10 ns with the maximum frequency error in the lock state is within the frequency error boundaries of the BBFD.

**Session A3L-C: Energy Harvesting**

**Chair:** Paul Furth, *New Mexico State University*

**Time:** Monday, August 5, 2019, 13:30 - 15:00

**Location:** Mesquite I

**A 2-Stage, 50Ω RF-DC Charge-Pump with Load Lines for High RF-DC Voltage Conversion** ..... 267

*Sichong Li, Fadhel Ghannouchi, Rushi Vyas*  
University of Calgary, Canada

A novel 2-stage RF-DC charge-pump circuit (RFCP) with a 50 ohm input impedance and higher RF-DC voltage conversion without an external input-matching network or output DC-filter for ambient wireless energy-harvesting (WEH) in the 2.4 GHz band is presented. The novelty of this RFCP is the use of near quarter-wavelength transmission lines on the load-side of each half-wave rectifying stage in the RFCP to induce a standing wave maxima at each of the diode inputs at 2.4 GHz. Doing so minimizes diode losses and maximize RF-DC voltage conversion of the charge-pump while still achieving a near 50 ohm input impedance. Simulations and measurements show the proposed design generating a higher DC output of 2.12V and energy efficiency of 18% with just -6dBm of RF input; an RF sensitivity of -7.2dBm for 1.8V output; and a 50Ω input impedance (reflection co-efficient = -11dB) in the 2.4 GHz band.



**Simultaneous Multi-Source Integrated Energy Harvesting System for IoE Applications** ..... 271

*Mohamed Badr, Mohamed M. Aboudina, Faisal A. Hussien, Ahmed N. Mohieldin*

Cairo University, Egypt

This paper presents an integrated modular multi-source energy harvesting system based on the Dickson charge pump and hill-climbing algorithm. The proposed maximum output power extraction is optimizing the system's end-to-end efficiency. It collects the power simultaneously from multiple energy sources and boosts their DC voltages to a regulated output voltage that can be used for Internet of Everything (IoE) applications. The proposed implementation utilizes the whole capacitance on-chip regardless of the number of stages in use. A demonstration system using the proposed techniques is implemented for two sources in 0.18  $\mu\text{m}$  CMOS technology and utilizes a total of 900 pF MIM capacitance. The simulation results shows that the proposed system achieves a peak MPPT efficiency of 90%, charge pump efficiency of 70% and end-to-end efficiency of 55% at a regulated output voltage of 1.5 V.

**Least Lossy Piezoelectric Energy-Harvesting Charger** ..... 275

*Siyu Yang, Gabriel A. Rincón-Mora*

Georgia Institute of Technology, United States

Wireless microsensors can operate indefinitely when they use ambient kinetic energy in motion to replenish the battery. Of available technologies, a switched inductor can draw the most power from a piezoelectric transducer. Power consumption, however, limits how much of that power the battery receives. This paper theorizes and shows that drawing and delivering power with an inductor from the transducer into the battery directly reduces the energy the inductor carries. With less energy, inductor current is lower, and ohmic losses can be up to 74% lower. This is why switched-inductor bridge is the least lossy piezoelectric charger in the state-of-the-art.

**An Improved OCV-Based MPPT Method Targeting Higher Average Efficiency in Thermal/Solar Energy Harvesters** ..... 279

*Zemin Liu, Yu-Pin Hsu, Mona M. Hella*

Rensselaer Polytechnic Institute, United States

This paper presents an improved open-circuit voltage (OCV)-based maximum power point tracking (MPPT) method which is able to achieve MPPT within a shorter sampling time compared to traditional architectures, and thus provides a higher average conversion efficiency from thermal/solar energy harvesters. The proposed OCV-based MPPT method employs separate control signals for the converter and MPPT blocks. A short time delay between disabling the converter and enabling the MPPT blocks eliminates the long charging time required to compensate for the voltage drop in the sampled signal, and thus reduces the sampling time. The prototype chip fabricated in 0.18- $\mu\text{m}$  has a 0.58 mm x 0.33 mm total area, delivers a 1.8 V DC voltage at an input voltage of 0.28 V. Measurement results confirm a sampling time of 26ms every 16s with an improved average efficiency of 82.2%.

**A Sub- $\mu\text{A}$  Quiescent Current Power Management System with SAR-Based Adaptive MPPT for Piezoelectric Energy Harvesting** ..... 283

*Ran Wei, Xinyao Tang, Soumyajit Mandal, Philip X.-L. Feng*

Case Western Reserve University, United States

We report on the design of a low quiescent current, high-efficiency power management circuit for piezoelectric (PZE) energy harvesting using a 180 nm CMOS process. The system includes: 1) active bias-flip rectifier to convert the AC output of the PZE energy harvester to DC; 2) inductor-based DC-DC boost converter with maximum power point tracking (MPPT) to boost the rectified voltage to a higher pre-defined value; 3) constant current battery charging module for charging a small Li-ion rechargeable battery, which is used as the energy storage element. The MPPT is implemented by a successive approximation (SAR)-controlled digital to analog converter (DAC), which is used as the current reference for the constant current battery charging module. This proposed MPPT method can adaptively adjust to different PZE harvesters (size, output voltage). The active bias-flip rectifier has 99.2% power conversion efficiency (PCE) and can boost the total amount of energy harvested from conventional rectifiers by more than 4 times. The step-up converter has 90.6% PCE, and the charging module can output 0-12.8  $\mu\text{A}$  under control of the 5-bit current DAC.

## Session A3L-D: RFIC, Microwave, and Optical Systems I

**Chair:** Taiyun Chi, *Rice University*

**Time:** Monday, August 5, 2019, 13:30 - 15:00

**Location:** Quorum I & II

### **A Power Mixer based Dual-Band Transmitter for NB-IoT Applications** ..... 287

*Xiaodong You, Haigang Feng, Xinpeng Xing, Zhihua Wang*

Tsinghua University, China

In this paper, a power mixer based dual-band transmitter for NB-IoT applications implemented in 65 nm RF CMOS process is described. The novel power mixer works at class-AB region to reduce power consumption and introduce gain-boosting structure to improve the CIM3. Based on the power mixer and tunable transformer-capacitor tank, the transmitter only has one path for dual-band. The number of on-chip transformers is only one achieving low chip area. The optimization on the power mixer can make the overall transmitter having relatively low power and high linearity.

### **Statistical Methodology to Relocate Resonance Frequencies of Software Defined Radio Antennas** ..... 291

*R.J. García-Dzul, C.H. Rodriguez, J.M. Trejo-Arellano, R. Parra-Michel*

Cinvestav, Mexico

Software Defined Radio (SDR) allows integrating different wireless communication standards using the same hardware. In this scenario the antenna should be able to operate at different frequency bands to maintain the SDR advantages. This difficult task can be tackled through matching networks (MN) circuits without requiring significant redesign of the SDR platform. However, is particularly difficult to find a set of MN components values when it is required to operate at multiple frequency bands. This paper proposes, a statistical methodology based on a Design of Experiments to model the SDR system response that effectively relocate the antenna frequency resonances.

### **A K-Band Differential SiGe Stacked Power Amplifier based on Capacitive Compensation**

#### **Techniques for Gain Enhancements** ..... 295

*<sup>1,2</sup>Xi Sung Loo, <sup>2</sup>Kiat Seng Yeo, <sup>1</sup>Moe Z. Win, <sup>2</sup>Zhichao Li, <sup>3</sup>Xiaopeng Yu, <sup>2</sup>Jer-Ming Chen*

<sup>1</sup>Massachusetts Institute of Technology, United States; <sup>2</sup>Singapore University of Technology and Design, Singapore;

<sup>3</sup>Zhejiang University, China

A 20GHz differential 4-stacked power amplifier fabricated on 0.18 $\mu$ m SiGe technology is presented. Uniquely, 2 capacitive compensation techniques are introduced at common base stages and successfully boosting power gain by 2.56dB/stage. Inter-stage matching inductors are adopted and input biasing is achieved by emitter follower for reliability concern. It demonstrates favorable gain performance of >20dB against other stacking schemes while showing competitive saturated power of  $\approx$ 22dBm with peak PAE of 26%.

### **A 140 GHz, 4 dB Noise-Figure Low-Noise Amplifier Design with the Compensation of**

#### **Parasitic Capacitance $C_{GS}$** ..... 299

*<sup>1</sup>Dong Wei, <sup>2</sup>Xuan Ding, <sup>2</sup>Hai Yu, <sup>2</sup>Bo Yu, <sup>1</sup>Shunli Ma, <sup>2</sup>Q. Jane Gu, <sup>1</sup>Junyan Ren*

<sup>1</sup>Fudan University, China; <sup>2</sup>University of California, Davis, United States

This paper presents the design of a 140 GHz, low-noise and low-power consumption LNA. A new input matching method and implementation based on the 3-coil transformer is proposed to further improve the noise figure performance. Combining the cap neutralization and current reuse techniques, the LNA achieves the 4 dB minimum NF and 21 dB maximum gain while takes 10 mW power consumption based on the TSMC 28nm CMOS process.

### **A New and Reliable Decision Tree based Small-Signal Behavioral Modeling of GaN HEMT** ..... 303

*<sup>1</sup>Ahmad Khusro, <sup>2</sup>Mohammad S. Hashmi, <sup>1</sup>Abdul Quaiyum Ansari, <sup>2</sup>Medet Auyenur*

<sup>1</sup>Jamia Millia Islamia University, India; <sup>2</sup>Nazarbayev University, Kazakhstan

The paper, for the first time, explores multivariable small signal modeling technique of GaN HEMT based on Decision tree. The proposed model presents a novel binary decision tree to model the GaN HEMT device for multi-biasing and broad frequency range. Bayesian algorithm has been used to find the optimal hyperparameters for better generalization capability and higher accuracy. An excellent agreement is found between the measured S-parameters and the proposed model for complete frequency range of 1GHz-18GHz.

## Session A3L-E: Neural Networks I

**Chair:** Fathi Salem, *Michigan State University*

**Time:** Monday, August 5, 2019, 13:30 - 15:00

**Location:** Salon G & H

### **Performance of Three Slim Variants of the Long Short-Term Memory (LSTM) Layer** ..... 307

*Daniel Kent, Fathi Salem*

Michigan State University, United States

LSTM-based neural networks have been successfully employed in various applications such as speech processing and language translation. The LSTM layer can be simplified by removing certain components, potentially speeding up training and runtime with limited change in performance. In particular, several recently introduced variants, called Slim LSTMs, have shown success in initial experiments. We performed computational analysis of the validation accuracy of a neural network architecture using the standard LSTM and three Slim LSTM layers. We found that some realizations of Slim LSTM layers can potentially perform as well as the standard LSTM layer for our considered architecture.

### **Neuromorphic In-Memory Computing Framework using Memtransistor Cross-Bar based Support Vector Machines** ..... 311

<sup>1</sup>*P. Kumar, <sup>1</sup>A.R. Nair, <sup>2</sup>O. Chatterjee, <sup>1</sup>T. Paul, <sup>1</sup>A. Ghosh, <sup>2</sup>S. Chakrabarty, <sup>1</sup>C.S. Thakur*

<sup>1</sup>Indian Institute of Science, India; <sup>2</sup>Washington University in St. Louis, United States

This paper presents a novel framework for designing support vector machines, which does not impose any restriction on the SVM kernel to be positive-definite and allows the user to define memory constraint in terms of fixed template vectors. A hardware implementation utilizing novel low power memtransistor device characteristic is shown for SVM implementation. The framework is shown to achieve state-of-the-art classification accuracy and is also scalable. This framework would be beneficial for the design of SVM based wake-up systems for Internet of Things devices where memtransistors can be used to optimize system's energy-efficiency and perform in memory matrix-vector multiplication.

### **Second Order Memristor Models for Neuromorphic Computing** ..... 315

*Francesco Marrone, Gianluca Zoppo, Fernando Corinto, Marco Gilli*

Politecnico di Torino, Italy

Second order memristors have shown to be able to mimic some specific features of neuron synapses, specifically Spike-Timing-Dependent-Plasticity (STDP), and consequently to be good candidates for neuromorphic computing. On the other hand neuromorphic studies and experiments have revealed different kinds of plasticity and have shown the effect of calcium concentration on synaptic changes. In this paper we derive a simplified model of a biologically inspired second order memristor and show that, through our approach, the most significant synaptic properties of second order memristors can be easily studied and predicted.

### **Adder-Only Convolutional Neural Network with Binary Input Image** ..... 319

<sup>1</sup>*Mayank Palaria, <sup>1</sup>Sai Sanjeet, <sup>1</sup>Bibhu Datta Sahoo, <sup>2</sup>Masahiro Fujita*

<sup>1</sup>Indian Institute of Technology Kharagpur, India; <sup>2</sup>University of Tokyo, Japan

Convolutional neural networks (CNNs) have performed exceptionally well on a variety of image classification tasks but need significant amount of memory and computational resources. In this paper, we propose an adder-only CNN (AO-CNN) inference engine, that has its weights and/or outputs at each layer reduced to either powers of two or zero, thus replacing the multiplication operations with a simple right or left shift and hence reducing the computation significantly. The proposed AO-CNN architecture, demonstrated using three sets of data-sets, viz., MNIST, EMNIST, and SVHN, performs with  $\approx 80\%$  accuracy or more, while using minimal hardware and taking only binary input images, i.e., 1 and 0. This could pave the way for realization of image-sensors with 1-bit resolution images and the corresponding CNN based classification engine being integrated into low-power internet-of-things (IoT) devices.

### **A Multiplication by a Neural Network (NN) with Power Activations and a Polynomial Enclosure for a NN with PReLU** ..... 323

*Kazuya Ozawa, Kaito Isogai, Toshihiro Tachibana, Hideo Nakano, Hideaki Okazaki*

Shonan Institute of Technology, Japan

Since a series of successes of deep neural networks (DNNs) with rectified linear units (ReLU), many approximations by NNs with ReLUs, parametric rectified linear units (PReLU), or rectified power units (RePUs) have been focused on. However how to obtain the parameters of NNs with PReLU, approximating polynomials, have not been fully discussed. In this paper for finding such parameters, a multiplication of NNs with  $n$ -th power (P) activation and a polynomial enclosure of NN with PReLU are discussed. Theorem of Multiplication of  $n$  variables by a NN with  $n$ -th P, and  $m$ -th P enclosure of PReLU are provided. PReLU NN is compared with the polynomial implying the enclosure. Learnings of the approximation by the shallow, or the deep PReLU NNs are also discussed.

## Session A3L-F: Digital and Arithmetic Circuits

**Chair:** Chunhong Chen, *University of Windsor*

**Time:** Monday, August 5, 2019, 13:30 - 15:00

**Location:** Addison

### **Allocating Gate Reliability for Circuit Reliability Optimization** ..... 327

*Suoyue Zhan, Khawja Sikander, Chunhong Chen*

University of Windsor, Canada

Reliable operation is increasingly critical for today's digital integrated circuits with nanoscale devices. High reliability requires various considerations and efforts throughout the design flow. However, at gate-level, it could be very time-consuming to conduct circuit reliability analysis and optimization in a global fashion. Currently, a general and computationally practical solution is to do local restructuring and optimization with certain cost constraints, which is less effective. This paper presents a global gate reliability allocation approach to optimize circuit reliability subject to specific cost constraints. With fast reliability estimation based on an asymmetrical reliability model, the proposed method is both effective and efficient with linear-time complexity.

### **HEVC Interpolation Filter Architecture using Hybrid Encoding Arithmetic Operators** ..... 331

<sup>1</sup>Rafael S. Ferreira, <sup>2</sup>Guilherme Paim, <sup>2</sup>Brunno A. Abreu, <sup>1</sup>Cláudio M. Diniz, <sup>1</sup>Eduardo Costa, <sup>2</sup>Sergio Bampi

<sup>1</sup>Catholic University of Pelotas, Brazil; <sup>2</sup>Federal University of Rio Grande do Sul, Brazil

The High-Efficiency Video Coding (HEVC) standard introduces a new and complex luminance interpolation filter for fractional-pixel motion estimation. This work investigates the use of a different encoding for the pixels and filter coefficients to reduce power dissipation of a sequential interpolation filter architecture based on the multiply-and-accumulate operation. The encoding, called Hybrid, groups  $m$  bits and uses Gray encoding to potentially reduce the switching activity both internally and at the inputs of the arithmetic operators. The high swings of the interpolation filter coefficients benefit the hybrid representation when compared with the binary. The architectures, using hybrid and binary arithmetic operators, were synthesized to 45 nm standard cells technology and analyzed in terms of power dissipation using real video sequences. Results show that by using the Hybrid arithmetic operators, the interpolation filter architecture reduces power in 14.26% on average when compared with the use of binary operators.

### **Optimal SAT-based Minimum Adder Synthesis of Linear Transformations** ..... 335

*Shenghou Ma, Paul Ampadu*

Virginia Polytechnic Institute and State University, United States

In this paper, we extend an existing boolean satisfiability (SAT) based formalization of the problem of synthesizing minimum adder circuit for linear transforms from GF(2) to generic case, and propose a successive approximate framework to make the formulation feasible with current SAT solvers. This approach could not only find optimal solutions but could also formally prove the optimality of the result. When applying this to synthesis of lightweight linear transformations (e.g., approximate DCT), it could find optimal multi-layer implementations that save up to 3.4% area and 3% power comparing to state-of-the-art ASIC synthesizers and up to 22% area saving and 6% delay improvements compared to FPGA synthesizers.

### **Design and Analysis of Energy Efficient Reversible Logic based Full Adder** ..... N/A

*Jagadeesh Pujar, Sithara Raveendran, Trilochan Panigrahi, Vasantha M.H, Nithin Kumar Y.B.*

National Institute of Technology Goa, India

Conventional digital systems incur information loss due to erasure of bits during logic operations resulting in remarkable amount of energy/power loss. Reversible computations nullify the information loss by retaining bits at the output. In arithmetic and logic computational structures, adders are the fundamental and performance determining component. In this paper an energy efficient low power reversible full adder is proposed, which is a combination of Feynman gates and a Fredkin gate. This paper proposes a comprehensive analysis and estimation of energy dissipation in reversible circuits. Cadence Virtuoso schematic editor is used to experimentally validate the models. The proposed adder effectively reduces ancilla inputs by 50%, garbage outputs by 50%, quantum cost by 33.33% and transistor count by 16.67% in comparison with full adder architectures present in literature.

## Session A3L-G: Linear and Nonlinear Circuits and Systems II

**Chair:** Federico Bizzarri, *Politecnico di Milano*

**Time:** Monday, August 5, 2019, 13:30 - 15:00

**Location:** Salon I & J

### **An Integrated Chaotic Transceiver for Spread-Spectrum Radar and Communications** ..... 343

*Xinyao Tang, Soumyajit Mandal*

Case Western Reserve University, United States

This paper introduces an integrated chaotic transceiver for spread spectrum communication and radar systems. The design uses a broadband transmitter based on a chaotic oscillator that combines a continuous differential equation with a discrete switching condition. This hybrid oscillator admits an analytic solution that is a linear convolution of symbol sequences and basis functions. A tunable analog matched filter circuit is designed for this basis function and used to implement an optimal coherent receiver to extract symbolic sequences from the chaotic waveform. The proposed chaotic transmitter and coherent receiver are then used to implement a simple on-off-keying (OOK) communication scheme. The proposed analog matched filter continuously outperforms a conventional Butterworth low-pass filter in an additive white Gaussian noise (AWGN) channel. Specifically, simulation results in a 180 nm CMOS process show an average improvement of ~3.0dB in signal-to-noise ratio (SNR) per bit when receiving noisy waveforms with SNR varying from -5 dB to 10 dB, thus significantly improving the bit-error-rate (BER).

### **Driving Point Loop Gain and Return Ratio** ..... 347

<sup>1</sup>Agustin Ochoa, <sup>2</sup>Don Patterson, <sup>3</sup>Megan McGuckin

<sup>1</sup>Xtreme Analog Circuit Technology, United States; <sup>2</sup>Ario Labs LLC, United States; <sup>3</sup>Texas Instruments Inc., United States

Stability in feedback analog circuits is measured as phase margin obtained from the system loop gain function. Different functions have been used to represent loop gain. Generally these functions yield similar phase margins so that the designer is usually not concerned with which may be correct. A development and comparison of results of two main approaches to finding loop gain, one focusing on a controlled source, Bode's Return Ratio, the other keeping circuit variables foremost, the driving point impedance approach, is presented showing the source of this difference concluding that the approach using a circuit focus analysis produces consistent results for phase margin while the Return Ratio may not making the former the preferred method.

### **Wave Digital Emulation of a Memristive Circuit to find the Minimum Spanning Tree** ..... 351

*Karlheinz Ochs, Dennis Michaelis, Enver Solan*

Ruhr-University Bochum, Germany

Self-organizing circuits are subject to current research because they are known to solve computationally complex tasks fast, energy efficient and can be implemented in integrated circuits with minimum space requirements. This is especially desired in contexts where the problem involves many components, such as neural networks, and the solution demands exhaustive computational effort. Networks which are centered around memristors have shown to be good candidates for such self-organizing, circuit-inspired solutions. One of many interesting problems include finding the minimum spanning tree in a graph, as it has applications in human learning in the context of the self-organizing discovery of information transport and hence topology formation. This work presents a memristive circuit to solve the minimum spanning tree in a directed, weighted graph of arbitrary size. Since the manufacturing process of memristors is generally complicated and costly, an emulator based on wave digital principles is derived which provides a powerful tool for investigations with different memristor models to aid development processes.

### **Solving the Longest Path Problem using a HfO<sub>2</sub>-Based Wave Digital Memristor Model** ..... 355

*Karlheinz Ochs, Dennis Michaelis, Enver Solan*

Ruhr-University Bochum, Germany

Circuit-inspired approaches are potential candidates to solve computationally complex problems. One of these problems is discovering the longest path, which is known to be a np-complete problem. The key are self-organizing memristive circuits which have shown to outperform existing graph-theoretical algorithms and while theoretical models of memristors have been used to tackle the problem before, models of real, manufacturable memristors have not been deployed yet. This paper intends to utilize physical models of real RRAM memristive devices. We exploit the wave digital concept as an emulation technique and our results show that the size of the maze has a neglectable influence on the time the solution is found.

### **Nonlinear Device Conversion** ..... 359

*Tyler Archer, Pallavi Ebenezer, Chin-Wen Chen, Randall Geiger*

Iowa State University, United States

A Nonlinear Device Converter is introduced that can be used to create useful new nonlinear devices whose characteristics differ significantly from those of the small number of basic devices that are currently available. The Nonlinear Device Converter is similar in concept to the generalized impedance converter but operates on nonlinear rather than linear devices. One example, supported by both analytical formulation and computer simulations in a 130nm CMOS process, converts a diode to a different one-port device that has a reduced voltage dependence and a reduced temperature dependence. A second example implemented in a 65nm CMOS process converts a MOS transistor to a different three-terminal device with different I-V characteristics.

## Session A4L-A: Analog Filters

**Chair:** Igor Filanovsky, *University of Alberta*

**Time:** Monday, August 5, 2019, 15:30 - 17:00

**Location:** Bent Tree I & II

### Low Sensitivity Coupled CMOS CCII Biquads ..... 365

<sup>1</sup>Edi Emanovic, <sup>1</sup>Drazen Jurisic, <sup>2</sup>George S. Moschytz

<sup>1</sup>University of Zagreb, Croatia; <sup>2</sup>Bar-Ilan University, Israel

In this paper we examine the influence of coupling to reduce the sensitivity to component tolerances in a CMOS-CCII realization of a fourth-order band-pass filter using two two-integrator biquads: cascaded and coupled. It is shown how the CCII non-idealities, causing lossy integrators, influence the coupled biquad design. With the example of a fourth-order 1MHz/100kHz band-pass filter, the design is tested with post-layout simulations with AMS 0.35-micron technology using Cadence. The analysis of the performance of both filters is done with Cadence. It is demonstrated that the coupled biquads, although having one more CCII and a resistor, have significantly lower sensitivity to component tolerances than the equivalent biquad cascade.

### Single-Transistor Second-Order Allpass Filters ..... 369

<sup>1</sup>M.B. Elamien, <sup>1</sup>B.J. Maundy, <sup>1</sup>L. Belostotski, <sup>1,2,3</sup>A.S. Elwakil

<sup>1</sup>University of Calgary, Canada; <sup>2</sup>University of Sharjah, U.A.E.; <sup>3</sup>Nile University, Egypt

This paper presents two CMOS designs of a second-order voltage-mode allpass filters (APFs) for high-frequency applications. Each of the proposed filters is based only on a single transistor and four surrounding impedances. The first proposed allpass filter is an RL filter while the second proposed one is an RLC filter. A detailed analysis along with the parasitic effects is provided for each of the proposed filters. As a proof of concept, one design was constructed and verified experimentally using discrete MOS transistors at a 2.3MHz pole frequency. The experimental results showed a group delay of approximately 165ns with a quality factor of 1. The second design was simulated in 65-nm CMOS process and demonstrated a group delay of 22ps within a bandwidth of 18GHz with total power consumption of 9mW.

### An Ultra-Low Power Wide-Band Single-Transistor Second-Order Allpass Filter in 65nm CMOS ..... 373

<sup>1</sup>M.B. Elamien, <sup>1</sup>B.J. Maundy, <sup>1</sup>L. Belostotski, <sup>1,2,3</sup>A.S. Elwakil

<sup>1</sup>University of Calgary, Canada; <sup>2</sup>University of Sharjah, U.A.E.; <sup>3</sup>Nile University, Egypt

In this paper, we propose a MOS design of a second-order voltage-mode allpass filter to be used as a time delay cell. The proposed filter is based on a single transistor, three resistors and two energy storage elements and was designed in a 65nm CMOS technology. Post-layout simulations demonstrate a group delay of approximately 13ps across a 30GHz bandwidth, while only consuming 809.7μW from a 1-V supply. As a proof of concept, the proposed filter was constructed and verified experimentally using discrete MOS transistors. The experimental results show a group delay of approximately 370ns across a 1.22MHz bandwidth.

## Session A4L-B: Energy Harvesters and Sensors

**Chair:** Anurag Veerabathini, *Maxim Integrated*

**Time:** Monday, August 5, 2019, 15:30 - 17:00

**Location:** Preston Trail I & II

### An SSHC Circuit Integrated with an Active Rectifier for Piezoelectric Energy Harvesting ..... 377

<sup>1</sup>Liao Wu, <sup>1</sup>Chenrui Guo, <sup>2</sup>Zhongsheng Chen, <sup>3</sup>Dong Sam Ha

<sup>1</sup>Changsha University, China; <sup>2</sup>Hunan University of Technology, China;

<sup>3</sup>Virginia Polytechnic Institute and State University, United States

This paper presents a piezoelectric energy harvesting circuit, which integrates a Synchronized Switch Harvesting on Capacitors (SSHC) and an active rectifier. An SSHC circuit does not require an inductor for voltage flipping, and hence is suitable for an on-chip implementation of the circuit. Existing SSHC circuits require dedicated switch drivers, which increases the circuit complexity to result in high power dissipation. The proposed circuit addresses this problem through integration of SSHC and a rectifier. The proposed circuit is designed in 0.35 μm CMOS technology. The simulation results indicate conversion efficiency of 92%, which is far higher than state-of-art SSHC circuits.

**Auto-Tuned Transition Scheme in Bias-Flip Rectifier for Piezoelectric Energy Harvesting** ..... 382

*Rohit Chaudhari, Ashis Maity*

Indian Institute of Technology Kharagpur, India

The self-sustainable, ultra-low powered devices and sensor nodes are becoming quite popular just because of the availability of the micro-power generators. One of such micropower generator is a piezoelectric energy harvester which converts the ambient mechanical vibration energy into the electrical energy. The piezoelectric energy harvester is capable of extracting 100's of  $\mu\text{W}$  of power available. The most widely used interfacing circuit for the piezoelectric energy harvester is a bias-flip rectifier. In the conventional bias-flip rectifier, there is an inherent trade-off between the power extraction and the size of the external inductor. Based on the system demand, the designers often face challenges to generate a precise transition time for a particular value of the inductor. In this paper, an auto-tuned transition scheme for the bias-flip rectifier is presented. It is capable of generating and adjusting the transition time suitably based on the value of the inductor chosen. The proposed auto-tuned transition scheme is designed in 180 nm CMOS technology with a total power consumption of 14.6  $\mu\text{W}$ .

**Frontend Electronic System for Triboelectric Harvester in a Smart Knee Implant** ..... 386

<sup>1</sup>Manav Jain, <sup>2</sup>Alwathiqbellah Ibrahim, <sup>1</sup>Emre Salman, <sup>1</sup>Milutin Stanacevic, <sup>3</sup>Ryan Willing, <sup>2</sup>Shahrzad Towfighian

<sup>1</sup>Stony Brook University, United States; <sup>2</sup>Binghamton University, United States; <sup>3</sup>University of Western Ontario, Canada

Total knee replacement (TKR) is an increasingly common surgery, particularly among active young and elderly people who suffer from knee pain. Continuous monitoring of the load on the knee after the surgery is highly desirable for designing an efficient and more functional smart knee implant. This study involves designing a triboelectric harvester to produce a signal, which is used by the proposed frontend electronic system to monitor the load. At a knee cyclic load of 2.3 kN, the harvester produces 6  $\mu\text{W}$  power and 18 V RMS signal at a frequency of 1 Hz. This paper proposes a novel self-powered frontend electronic system to process this harvested signal and monitor the load on the knee. First, an electrical model is generated for the fabricated harvester. In the next step, the output signal is processed using a filter, rectifier and regulator, and finally converted into digital bits using an analog-to-digital converter. The power consumption of the proposed design is 5.25  $\mu\text{W}$ .

**A Sensor Interface for Neurochemical Signal Acquisition** ..... 390

*Olaitan Olabode, Marko Kosunen, Vishnu Unnikrishnan, Tommi Palomäki, Tomi Laurila,*

*Kari Halonen, Jussi Ryyänen*

Aalto University, Finland

This paper describes the design of an integrated sensor interface for neurochemical signal acquisition. Neurochemicals undergo oxidation and reduction reactions in the presence of an action potential. Thus, knowledge of the oxidation and reduction potentials of neurochemicals is important in the neurostimulation treatment of neurological and neurodegenerative diseases. The sensor interface circuit utilizes a mixed-signal design to detect the induced current from the neurochemical, in response to an applied voltage. The circuit is fabricated in 65nm CMOS technology and supports a wide input current range of  $\pm 1.2\mu\text{A}$  with a current resolution of 85.4pA, enabling detection of neurochemicals within the supported current range. Measured results with dopamine concentration of 500nMol demonstrate the ability of the sensor interface circuit to detect oxidation and reduction current peaks, indicating the release times and the required oxidation and reduction potentials for neurostimulation of the neurochemical.

**Low Noise Combined Optical-Chemical CMOS Sensor for Biomedical Application** ..... 394

*Mozhdeh Nematzadeh, Philipp Dominik Häfliger, Behnam Samadpoor Rikan, Steffen Nøvik, Joar Martin Østby*

University of Oslo, Norway

In this paper, a combined optical-chemical biosensor is realized by integrating photodiodes (PDs) and ion sensitive field effect transistors (ISFETs) in a dense 2D pixel array. It is intended for rapid screening of specific biomolecular membranes with-photo sensitive ion-pumps. A correlated double sampling (CDS) readout is applied to suppress the pixel-to-pixel non- uniformity such as the threshold voltage mismatch for ISFET pixel, and the reset KTC noise for PD pixel. An 8 (PD pixel) and 9 (ISFET pixel) transistor configuration with two in-pixel capacitors realize CDS and global shutter functionality. The sensor consists of a  $46 \times 46$  pixel array with the 31.5 $\mu\text{m}$  pixel pitch. The pixel array and peripheral circuitry are designed using a standard 0.35 $\mu\text{m}$  CMOS technology and occupy an area of 4.73mm<sup>2</sup>. A switched capacitor amplification gain of 2 in the readout chain realizes a light sensitivity of 400  $\mu\text{V}/\text{lux}$  for optical pixels and a pH sensitivity of 150mV /pH for chemical pixels.

## Session A4L-C: Power Converters

**Chair:** Narayan Kar, *University of Windsor*

**Time:** Monday, August 5, 2019, 15:30 - 17:00

**Location:** Mesquite I

### **Total Harmonic Distortion and Power Factor Improvement Technique for CRM Flyback PFC Converters ..... 399**

<sup>1,2</sup>*Mustafa Kavci, <sup>2</sup>Ahmet Tekin, <sup>1</sup>Cengiz Tarhan*

<sup>1</sup>Vestel Electronics Power R&D Lab, Turkey; <sup>2</sup>Özyeğin University, Turkey

In many of today's solid-state lighting applications, Critical Conduction Mode (CCM) Flyback PFC converter is a popular solution due to its limited component count and simple structure with respect to other SMPS topologies. As described in international standards documents (IEC/EN 61000-3-2), drivers are required to demonstrate a power factor results greater than 0.9 and lower THD for power levels above 25W. Due to non-sinusoidal input current waveform of the traditional constant-on-time control method, achieving improved PF and THD is quite difficult. In this paper, a new control method is introduced in an effort to improve power factor and total harmonic distortion of Voltage Mode CRM Flyback PFC Converter. The work proposes injection of a compensating  $\sin(\omega t)$  signal component in the feedback path utilizing an additional primary transformer winding to linearize the current from the source. The detailed theoretical analysis is presented along with measurement results of a 30W high-power system prototype.

### **Bidirectional Interleaved Buck/Boost DC-DC Converter Design to Improve Power Density in High-Current Applications ..... 403**

*Joseph Edler, Nisha Kondrath*

Villanova University, United States

Interleaved topologies are popular in high-power high-current applications due to the reduction in device current stresses and filter sizes. Despite its popularity, a proper design procedure for bidirectional interleaved dc-dc converter operating in CCM including the selection of appropriate number of phases and passive component design to optimize converter efficiency is missing in the literature. This paper presents a comprehensive design procedure for a bidirectional interleaved buck/boost dc-dc converters for high-current applications. Use of silicon carbide devices in the converter will further improve its efficiency and power density.

### **Tapped-Inductor Buck DC-DC Converter with Complex Load ..... 407**

*Ankit Chadha, Marian K. Kazimierzczuk*

Wright State University, United States

This paper provides small-signal analysis of a pulse width modulated (PWM) tapped-inductor buck dc-dc converter with complex load running in continuous conduction mode (CCM). Circuit averaging technique is used to obtain its small-signal model. The obtained model is then used to obtain duty cycle-to-output voltage and input-to-output voltage transfer functions. The equations representing the exact effect of the complex load these transfer functions have been derived. The obtained theoretical results are validated through circuit simulations.

### **Custom Built 400kW 1kV 2-Channel Water-Cooled Power Electronics Building Block ..... 411**

<sup>1</sup>*Robert W. Ashton, <sup>2</sup>Sherif Michael*

<sup>1</sup>Ashton Consulting LLC, United States; <sup>2</sup>Naval Postgraduate School, United States

This paper documents the requirements, modeling, design and testing of a 400kW 1kV full-bridge water-cooled power electronics building block for use as a low frequency current injector for an industrial load. The evolution of the buss bar, buss capacitance and gate driver mother-board are discussed. Both modeling and hardware test results are presented.

## Session A4L-D: RFIC, Microwave, and Optical Systems II

**Chair:** Vishal Saxena, *University of Idaho*

**Time:** Monday, August 5, 2019, 15:30 - 17:00

**Location:** Quorum I & II

### **Microwave Photonic Notch Filter based on the use of the Chromatic Dispersion Parameter and the Length of an Optical Link ..... 416**

<sup>1</sup>*J.R. Warnes-Lora, <sup>1</sup>L.J. Quintero-Rodríguez, <sup>1</sup>L.A. González-Mondragón, <sup>1</sup>I.E. Zaldivar-Huerta,*

<sup>2</sup>*J. Rodríguez-Asomoza, <sup>3</sup>R. Rojas-Laguna*

<sup>1</sup>INAOE, Mexico; <sup>2</sup>Universidad de las Américas Puebla, Mexico; <sup>3</sup>Universidad de Guanajuato, Mexico

In this paper, an approach to achieving a microwave photonic notch filter based on the use of the chromatic dispersion parameter and the length of an optical link is presented. The proposed photonic notch filter has the ability to adjust its bandwidth by varying the length of the optical link. A set of simulations are carried out for lengths of 25 km, 38 km, 50 km and 63 km. Theoretical, simulated and experimental results are in good agreement for every location of the notches obtained. The filter has potential application in the field of optical communications systems.



**High Gain High Efficiency Doherty Amplifiers with Optimized Driver Stages** ..... 420

<sup>1</sup>Duy P. Nguyen, <sup>2</sup>Xuan-Tu Tran, <sup>1</sup>Phat T. Nguyen, <sup>1</sup>Nguyen L.K. Nguyen, <sup>1</sup>Anh-Vu Pham

<sup>1</sup>University of California, Davis, United States; <sup>2</sup>VNU University of Engineering and Technology, Vietnam

In this paper, we present two different approaches to design a driver for high gain Doherty power amplifiers (DPAs): single driver and dual driver topologies. Detailed analysis and quantitative comparison between the two approaches are proposed. In particular, the single driver topology is preferred when the output Doherty stage has a reasonable gain. On the other hand, when the output stage has low gain, the dual driver approach is required to prevent significant efficiency reduction. Two DPA circuits at two different frequency ranges have been fabricated in a 0.15- $\mu\text{m}$  Gallium Arsenide (GaAs) process to verify the concept. The single driver DPA at 10 GHz achieves a measured gain of 19.2 dB and the maximum power of 27 dBm. The peak power added efficiency (PAE) and PAE at 6-dB power back-off (PBO) are 43% and 32%, respectively. On the other hand, the dual driver DPA at 28 GHz exhibits 15 dB of gain, 28.2 dBm of output power level with an associated peak PAE of 37%. To the best of the authors' knowledge, our DPA prototypes achieve the highest gain of all reported DPA at similar frequency ranges.

**Rapid Simulation of Photonic Integrated Circuits using Verilog-A Compact Models** ..... 424

*Md Jubayer Shawon, Vishal Saxena*

University of Idaho, United States

With the advent of silicon-based integration of photonics, there is a growing interest in the electronic circuits community to develop hybrid electronic-photonic integrated systems. However, photonic integrated circuits (PICs) design tools have focused on the solutions of Maxwell's equations using numerical methods. Recently developed PIC system-level design tools employ s-parameter modeling of optical components. However, in such platforms, accurate modeling of electronic driver and interface circuits is not supported. To allow electronic integrated circuit (IC)-centric design, there is a trend of compact modeling of photonic components using Verilog-A so that they can be co-simulated with CMOS electronics. In this work, we present our modeling approach and a novel method for rapid frequency-domain simulation of PICs.

**A Signal Source Chip at 140 GHz and 160 GHz for Radar Applications in a SiGe Bipolar Technology** ..... 428

<sup>1</sup>Matthias Völkel, <sup>2</sup>Mohamed Thoubtia, <sup>1</sup>Sascha Breun, <sup>3</sup>Klaus Aufinger, <sup>1</sup>Robert Weigel, <sup>1</sup>Amelie Hagelauer

<sup>1</sup>Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany; <sup>2</sup>eesy-ic GmbH, Germany;

<sup>3</sup>Infineon Technologies AG, Germany

In this paper, a monolithic signal source chip at 140 GHz and 160 GHz including two VCOs, a dynamic divider and a static divider chain is presented. Two signal sources with these high fundamental frequencies are realized. All components have been designed using a 0.13 $\mu\text{m}$  250 GHz fT SiGe BiCMOS technology. The whole integrated circuit has a size of 930 $\mu\text{m}$  x 600 $\mu\text{m}$  including bondpads and consumes 210mA from a 3.3V and 130mA from a 1.8V supply. The oscillators cover a frequency range from 119.3–147.7 GHz and 154.2–164 GHz, which results in a tuning range of 28.4 GHz and 9.8 GHz. A output power of -0.9/3.6dBm with a best case phase noise of -111.2/-108 dBc/Hz at 1MHz offset, measured at the divider output for PLL stabilization is achieved.

**An Inductorless Noise Cancelling Wideband Balun LNA with Dual Shunt Feedback and Current Reuse** ..... 432

*Shashank Tiwari, Jayanta Mukherjee*

Indian Institute of Technology Bombay, India

An inductorless wideband low noise amplifier (LNA) with single to differential conversion is proposed for low power multiband and multi-standard radios. Conventionally common source (CS) and common gate (CG) based balun LNA suffers from high power dissipation. The proposed LNA uses dual shunt feedback to reduce the bias current of CG stage while this current is reused by CS stage. Complimentary CS stage is used to get maximum transconductance. The design is implemented in 180nm CMOS technology and occupies an active chip area of 0.24mm<sup>2</sup>. It achieves a maximum voltage gain of 18.5 dB, minimum NF of 2.8 dB, bandwidth ranging from 210 MHz to 1.1 GHz and an IIP3 of -13.4 dBm. The proposed design excluding the buffer draws a current of 3.1 mA from 1.8 V power supply.

**Session A4L-E: Neural Network II**

**Chair:** Fathi Salem, *Michigan State University*

**Time:** Monday, August 5, 2019, 15:30 - 17:00

**Location:** Salon G & H

**39fJ Analog Artificial Neural Network for Breast Cancer Classification in 65nm CMOS** ..... 436

*Ruobing Hua, Arindam Sanyal*

University at Buffalo, United States

An analog artificial neural network (ANN) classifier using a common-source amplifier based nonlinear activation function is presented in this work. A shallow ANN is designed in 65nm CMOS to perform binary classification on breast cancer dataset and identify each patient data as either benign or malignant.

**Traffic Sign Recognition based on Multilayer Perceptron using DWT and DCT** ..... 440

*Genevieve Sapijaszko, Taif Alobaidi, Wasfy B. Mikhael*

University of Central Florida, United States

The purpose of this study is to improve the speed of traffic sign recognition while maintaining accuracy through a neural network. The proposed system will reduce the size of the image without losing any vital information as well as extract features of the images through a combination of the discrete wavelet transform and the discrete cosine transform. A multilayer perceptron will complete the analysis and classification. The execution speed is significantly improved while maintaining a recognition accuracy of 96% using three traffic signs dataset: BelgiumTSC, GTSRB, and TSRD datasets.

**A Spatiotemporal Pattern Detector** ..... 444

*Robert Ivans, Kurtis D. Cantley*

Boise State University, United States

A spatiotemporal pattern detector design is presented which can identify three fundamental spatiotemporal patterns consisting of two spikes (from different neurons or from the same neuron). These fundamental cases provide the building blocks for construction of more complicated arbitrary spatiotemporal patterns. The overall design consists of three primary subcircuits, and the operation of each is described. The detection of the three cases of spatiotemporal patterns, and the detection of a more complicated pattern by a network of Spatiotemporal Pattern Detectors, is then demonstrated through simulation using the Cadence Virtuoso platform.

**Slim LSTMs: Parameter-Reductions within Gating Signals** ..... N/A

*Fathi M. Salem*

Michigan State University, United States

Long Short-Term Memory (LSTM) Recurrent Neural networks (RNNs) rely on gating signals, each driven by a function of a weighted sum of at least 3 components: (i) one of an adaptive weight matrix multiplied by the incoming external input vector sequence, (ii) one adaptive weight matrix multiplied by the previous memory/state vector, and (iii) one adaptive bias vector. In effect, they augment the simple Recurrent Neural Networks (sRNNs) structure with the addition of a "memory cell" and the incorporation of at most 3 gating signals. The standard LSTM structure and components encompass redundancy and overly increased parameterization. In this paper, we systemically introduce variants of the LSTM RNNs, referred to as Slim LSTMs. These variants express aggressively reduced parameterizations in the gates to achieve computational saving and/or speedup in (training) performance--while necessarily retaining (validation accuracy) performance comparable to the standard LSTM RNN.

**Session A4L-F: SPECIAL SESSION: Emerging Topics in Hardware Security and Trust**

**Chair:** Rashmi Jha, *University of Cincinnati*

**Co-Chair:** Marty Emmert, *University of Cincinnati*

**Time:** Monday, August 5, 2019, 15:30 - 17:00

**Location:** Addison

**Non-Invasive Reverse Engineering of Finite State Machines using Power Analysis and Boolean Satisfiability** ... 452

*Harsh Vamja, Richa Agrawal, Ranga Vemuri*

University of Cincinnati, United States

In this paper, we present a non-invasive reverse engineering attack based on a novel approach that combines functional and power analysis to recover finite state machines from their synchronous sequential circuit implementations. The proposed technique formulates the machine exploration and state identification problem as a Boolean constraint satisfaction problem and solves it using a SMT (Satisfiability Modulo Theories) solver. It uses power measurements to achieve fast convergence. Experimental results using the LGSynth'91 benchmark suite show that the satisfiability-based approach is several times faster compared to existing techniques and can successfully recover 90%-100% of the transitions of a target machine.

**Process Specific Functions for Assurance of Analog/Mixed-Signal Integrated Circuits** ..... 456

<sup>1</sup>*Matthew Casto, <sup>1</sup>Brian Dupaix, <sup>1</sup>Pompei Orlando, <sup>2</sup>Waleed Khalil*

<sup>1</sup>Air Force Research Laboratories, United States; <sup>2</sup>Ohio State University, United States

This paper investigates the process-induced variation response of analog and mixed-signal ICs to yield anti-counterfeiting and anti-cloning design techniques. It defines unique behaviors called Process Specific Functions (PSFs) that identify circuits of the same pedigree and provide traits for authentication and individual chip identification. To demonstrate PSF utility, expansion of quantization sampling theory is used to produce a statistically bounded digital to analog converter uniqueness model. A parameter space of normalized, challenge driven, non-linear harmonic amplitude responses are then correlated to random and systematic process variations to produce distributions for probability of detection and probability of false alarm statistics. These authenticity characteristics are related to process models to provide a novel analog IC supply chain risk management technology.

**Logic Obfuscation using Metasurface Holography** ..... 460

*Mahabubul Alam, Yimin Ding, Xingjie Ni, Swaroop Ghosh*

Pennsylvania State University, United States

In this paper, we have presented a novel obfuscation technique based on the concepts of cloaked nets and fake holographic gates using metasurface holography. The proposed approach can address optical and X-ray imaging based RE.

**Operating Temperature based Vulnerabilities in ReRAM** ..... 464

*Thomas Schultz, Rashmi Jha*

University of Cincinnati, United States

Resistive Random-Access Memory (ReRAM) devices have caught significant research attention as scalable non-volatile memory (NVM) technology for high-density data storage in 3-D crossbar architectures. Memory storage read/write schemes rely on specific timing, voltage, and sensing thresholds to change and determine the states of the devices. While several in-memory computing architectures with ReRAM have been proposed, the impact of chip operating temperatures on write and read operations of ReRAM and the impact on resistive states is not well studied. This paper reports the impact of the temperature on the ReRAM devices during the write and read operations

**Session A4L-G: Machine Learning to Enhance the Internet of Things and Environmental Monitoring**

**Chair:** Mohsin Jamali, *University of Texas Permian Basin*

**Time:** Monday, August 5, 2019, 15:30 - 17:00

**Location:** Salon I & J

**Parallel Bayesian Belief Network in Building Energy Conservation** ..... 468

<sup>1</sup>*Golrokh Mirzaei, <sup>1</sup>Nima Mansouri, <sup>2</sup>Mohsin M. Jamali*

<sup>1</sup>Ohio State University, United States; <sup>2</sup>University of Texas Permian Basin, United States

It is important to control processes efficiently in commercial buildings for Energy conservation. The key element for saving energy is to obtain accurate information about the occupancy, and if there is no one in the building then services such as Heating, Ventilation, and Air-conditioning (HVAC), lighting, etc. can be turned off. Also, it is very critical that the building services respond in real-time, as it may affect the functionality of employees/equipment in the building. This paper presents a fast occupancy detection technique using parallel Bayesian Belief Network. This technique can be used as a fast, reliable, and automated occupancy detection technique in commercial buildings.

**Lab in a Box : A Rapidly Deployable Environmental Monitoring IoT System** ..... 472

*Sudip Maitra, Ahmed Abdelgawad, Kumar Yelamarthi*

Central Michigan University, United States

The advent of the Internet of Things (IoT) has brought about a new horizon in the field of pervasive computing and network-oriented systems. IoT has enabled everyday "things" to communicate with each other, exchange information and perform tasks more efficiently in terms of power and resources while requiring minimum human intervention. As the application scope of IoT is tremendously vast, the integration of heterogeneous objects or "things" in an IoT system is a challenging task. In this paper, multiple embedded systems have been implemented in battery powered, small portable packages to acquire environmental data from various sensors and publish the information to several IoT cloud platforms for analysis and visualization, using different wireless transceiver technologies to demonstrate the portability, modularity, and interoperability of lab in a box.

**Distributed Estimation via Opinion Dynamics** ..... 476

*Noyan C. Seviüktekin, Alexander G. Schwing, Andrew C. Singer*

University of Illinois at Urbana-Champaign, United States

Distributed networks comprising decision-making units of variable competence are used to perform a sequence of tasks. Estimation of the local competences based solely on comparisons of local decisions on dynamically changing tasks is necessary for improving decision aggregation performance. This paper addresses distributed estimation of local competences on networks of heterogeneous decision-making units. We propose an order-preserving metric that depends on the local network structure to measure the competence of each node in the network instantaneously. We investigate two regimes of operation: First, the tasks are received at low frequency, or sequentially, hence the network can reach a consensus in-between tasks. Second, tasks are received at high frequency, or in batches, in which case, the network reaches to a consensus after tasks are processes locally.

**Classification of Alzheimer's Disease from MRI Data using an Ensemble of Hybrid Deep Convolutional Neural Networks** ..... 481

*Emimal Jabason, M. Omair Ahmad, M.N.S. Swamy*  
Concordia University, Canada

Although there is no cure for Alzheimer’s disease (AD), an accurate early diagnosis is extremely important for both the patient and social care, and it will become even more significant once disease-modifying agents are available to prevent, cure, or even slow down the progression of the disease. In recent years, classification of AD through deep learning techniques has been one of the most active research areas in the medical field. However, most of the existing techniques cannot leverage the entire spatial information; hence, they lose the inter-slice correlation. In this paper, we propose a novel classification algorithm to discriminate patients having AD, mild cognitive impairment (MCI), and cognitively normal (CN) using an ensemble of hybrid deep learning architectures to leverage a more complete spatial information from the MRI data. The experimental results obtained by applying the proposed algorithm on the OASIS dataset show that the performance of the proposed classification framework to be superior to that of the conventional methods.

**Tuesday, August 6, 2019**

**Session B1L-A: Sigma-Delta Modulators**

**Chair:** Jose M. de la Rosa, *Instituto de Microelectrónica de Sevilla*

**Time:** Tuesday, August 6, 2019, 8:00 - 9:30

**Location:** Bent Tree I & II

**Single-Ended-to-Differential Sampling Technique for Sigma Delta ADCs in X-Ray Detectors** ..... 485

*Hussein Ali, Pietro Caragiulo, Camillo Tamma, Xiaobin Xu, Bojan Markovic, Faisal Abu-Nimeh, Dionisio Doering, Angelo Dragone, Gunther Haller*  
SLAC National Accelerator Laboratory, United States

A sampling technique for X-ray detectors is presented, which performs a two channel single-ended-to-differential sampling, and buffers the sampled signals serially to the incremental Sigma Delta ADC. This sampling technique maximizes the readout speed of the X-ray detectors, while allowing the ADC to sample the input signal multiple times for reduced thermal noise and higher resolution. The sampler is implemented in 0.25 um CMOS technology, as a part of a mixed signal processing backend for the pixel signal, consists of buffering, ADC conversion and readout circuits. Measured performance shows a high linearity of >77 dB SNDR at 3.5 Kfps, which emphasizes the speed advantage and high linearity of the proposed approach.

**Time-Mode All-Digital Delta-Sigma Time-to-Digital Converter with Process Uncertainty Calibration** ..... 489

*Fei Yuan, Parth Parekh*  
Ryerson University, Canada

This paper studies the impact of process uncertainty on a time-based all-digital  $\Delta\Sigma$  time-to-digital converter (TDC) with a differential pre-skewed bi-directional gated delay line (BDGDL) time integrator. The principle and design of the TDC are presented first. It is followed with an in-depth investigation of the impact of process uncertainty on the building blocks of the TDC. An effective calibration technique capable of minimizing the impact of process uncertainty on the performance of the TSC is proposed. The TDC is designed in a 130 nm 1.2 V CMOS technology and analyzed using Spectre with BSIM4 device models. Simulation results demonstrate that process spread has a significant impact of the delay of the building blocks of the TDC subsequently the performance of the TDC. The detrimental impact of process uncertainty can be minimized by optimizing the TDC at SS (slow NMOS/slow PMOS) corner and adjusting the delay of the key delay blocks and that of the gated delay stages of the TDC in TT (typical NMOS/typical PMOS) and at FF (fast NMOS/fast PMOS) corner to their respective SS-corner value.

**All-Digital  $\Delta\Sigma$  TDC with Current-Starved Bi-Directional Gated Delay Line Time Integrator** ..... 493

*Fei Yuan, Parth Parekh*  
Ryerson University, Canada

This paper presents an all-digital 1st-order 1-bit  $\Delta\Sigma$  time-to-digital converter (TDC) with a differential current-starved bi-directional gated delay line (CS-BDGDL) time integrator with built-in quantization. Current-starved gated delay cells are used to improve the linearity of the time integrator subsequently the SNDR of the TDC. Differential time integration is performed by simultaneously issuing right-shift and left-shift commands to the CS-BDGDL so as to minimize integration time. The error caused by current mismatch between NMOS and PMOS transistors of gated delay cells is eliminated using a digital comparator. Design methodologies for process uncertainty are explored. The TDC is designed in an IBM 130 nm 1.2 V CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM4 device models. Simulation results show that the figure-of-merit (FOM) of the proposed all-digital TDC outperforms that of all reported TDCs alike.

**A 0.2 pJ/Step Open Loop VCO-Based ADC with inverse R-2R Prewighted Linearization** ..... 497

*Karama M. Al-Tamimi, Kamal El-Sankary*

Dalhousie University, Canada

An open loop analog-to-digital converter based on ring voltage-controlled oscillator (VCO-based ADC) is presented. By introducing the inverse R-2R pre-weighted front-end technique, the nonlinearities of the voltage to frequency conversion of the proposed VCO is kept less than 1% over rail-to-rail input swing. Unlike prior approaches, this proposed method does not suffer from any stability issues or feedback imperfections. A prototype was fabricated using TSMC 65nm process. It occupies an active area of 0.03 mm<sup>2</sup> and consumes as little as 3.1 mA from 1 V power supply. Measurement results of linearity indicate SFDR and SNDR of 77 and 66.7 dB, respectively, over 5 MHz passband bandwidth. This reveals energy less than 0.2 pJ/step.

**Fully Digital 1-1 MASH VCO-Based ADC Architecture** ..... 501

*Mohammadhadi Danesh, Arindam Sanyal*

University at Buffalo, United States

This paper proposes a novel architecture for purely voltage controlled oscillator (VCO) based 1-1 MASH second-order analog-to-digital converter (ADC). Each stage of the MASH uses an open loop inverter based ring VCO. The proposed ADC uses phase information from all inverters in the VCO in both the MASH stages to perform efficient multi-bit quantization. A novel VCO quantization error extraction circuit is proposed to easily extract quantization noise of the first VCO stage. A gain calibration for the second stage of the ADC has been analyzed. Behavioral simulations have been performed to validate the proposed architecture.

## **Session B1L-B: Voltage References and Bandgaps**

**Chair:** Anuraj Veerabathini, *Maxim Integrated*

**Time:** Tuesday, August 6, 2019, 8:00 - 9:30

**Location:** Preston Trail I & II

**A Precision Bandgap Voltage Reference using Curvature Elimination Technique** ..... 505

*Pallavi Ebenezer, Tyler Archer, Degang Chen, Randall Geiger*

Iowa State University, United States

A bandgap voltage reference circuit using a curvature elimination approach is proposed. Curvature elimination is achieved by a weighted subtraction of the outputs of two basic bandgap circuits that have the same functional form of the curvature. The reference is implemented in a 130nm CMOS process and generates a nominal output voltage of approximately 700mV. Simulation results predict the proposed circuit can achieve a temperature coefficient of 0.3ppm/°C over the temperature range from 0°C to 100°C

**A Curvature Compensated Bandgap Circuit Exploiting Temperature Dependence of  $\beta$**  ..... 509

*Radha Krishna Mothukuru, Manish Kumar, Bibhu Datta Sahoo*

Indian Institute of Technology Kharagpur, India

This paper proposes a technique for the curvature compensation in Bandgap references to obtain a better Temperature Coefficient (TC). The proposed method is based on the fact that the Bipolar junction transistors used in Bandgap references have finite Beta which is temperature dependent. As  $\beta$  of NPN transistors in CMOS process is very low, Darlington configuration is used to achieve larger  $\beta$  to achieve the desired curvature compensation. Designed and simulated in TSMC 180-nm CMOS process the proposed bandgap circuit achieves a temperature coefficient of 9.9 ppm/°C across a temperature range of -40°C to 125°C and a line regulation from 1.6 V to 4.0 V.

**A Low-Latency 16-Phase Pulse Width Modulator with Phase Angle Control for 140MHz Fully Integrated Voltage Regulators on 22nm Tri-Gate CMOS** ..... 513

*Gerhard Schrom, Sarath Makala, Ravi Sankar Vunnam, Raghuraman Narayanan, Fabrice Paillet*

Intel Corporation, United States

A 16-phase Pulse Width Modulator (PWM) for Fully Integrated Voltage Regulators manufactured on a 22nm tri-gate CMOS process is presented. The PWM supports a wide operating frequency range of 20MHz-320MHz, individually programmable phase angles from 0° to 360° with 11.25° resolution, a low latency of 150ps, and synchronized enabling/disabling of phases. The PWM can be phase-locked to a spread-spectrum reference clock for EMI/RFI control. The design does not require low-leakage analog components.

## Session B1L-C: Power Systems

**Chair:** Ali Mehrizi-Sani, *Washington State University*

**Time:** Tuesday, August 6, 2019, 8:00 - 9:30

**Location:** Mesquite I

### **Substation Earth Grid Modeling and Simulation for Transient Performance Analysis** ..... 517

*Bongeka Z. Nongena, Agha Francis Nnachi, Philip Tshubwana, Coneth G. Richards*

Tshwane University of Technology, South Africa

This paper presents model of a substation earth grid with analytical method of determining the resistances of the meshes and electrodes for proper model representation in Matlab/Simulink. The model is then used for earthing system simulation of 88/22 kV substation to assess its transient performance.

### **Analysis and Application of Seasonal ARIMA Model in Energy Demand Forecasting:**

#### **A Case Study of Small Scale Agricultural Load** ..... 521

*Subrina Noureen, Sharif Atique, Vishawjit Roy, Stephen Bayne*

Texas Tech University, United States

This paper has presented the use of Auto Regressive Integrated Moving Average (ARIMA) method for forecasting of seasonal time series data. An agricultural dataset has been used for modeling and forecasting. ARIMA method can be applied only when the time series data is stationary. As seasonal variations make a time series non-stationary, this paper also presents analyses on testing stationarity and transforming non-stationarity into stationarity. Lastly, the model has been developed with a specific selection of orders for autoregressive terms, moving average terms, differencing and seasonality and the forecasting performance has been tested and compared with the actual value.

### **Mitigation of Distribution Voltage Violations using Single-Phase Residential Static VAR Compensators** ..... 525

*Andres Valdepeña Delgado, Muhammad Kamran Latif, Said Ahmed-Zaid*

Boise State University, United States

An alternative method to support the voltage at the end of a distribution feeder using residential static VAR compensators (RSVCs) is presented. The distribution feeder and the RSVCs were modeled using OpenDSS and validated by comparing the results of measured data with the output of the model. Results show that the use of RSVCs on the low side of the service transformers is an efficient way to mitigate low- and high-voltage violations in the distribution feeder. During a one-month evaluation of the system, the results show that the use of RSVCs was able to eliminate all voltage violations below 113 V and it reduced the number of voltage violations under 114 V by 88%

### **Design of Load-Independent Class-E Inverter with MOSFET Parasitic Capacitances** ..... 529

*<sup>1</sup>Weisen Luo, <sup>1</sup>Xiuqin Wei, <sup>2</sup>Hiroo Sekiya, <sup>3</sup>Tadashi Suetsugu*

<sup>1</sup>Chiba Institute of Technology, Japan; <sup>2</sup>Chiba University, Japan; <sup>3</sup>Fukuoka University, Japan

This paper presents a numerical design method of the load-independent class-E inverter with MOSFET parasitic capacitances. A design example is shown along with its LTspice simulation and laboratory experiment. There are no changes in the output-voltage waveforms and all the switch-voltage waveforms satisfy the zero-voltage-switching (ZVS) condition even the load-resistance value varies from the desired one. Additionally, the results obtained from the LTspice simulation and laboratory experiment show quantitative agreement with the numerical predictions, which shows the effectiveness of the proposed design method of the load-independent class-E inverter with MOSFET parasitic capacitances given in this paper.

### **Fractional-Order LC<sup>α</sup> L Filter-Based Grid Connected PV Systems** ..... 533

*Reyad El-Khazali*

Khalifa University, U.A.E.

this paper introduces a new class of fractional-order LCL (FoLCL) low-pass filters to mitigate current harmonics caused by inverters in grid connected photovoltaic (PV) systems. Usually LCL filters interconnect inverters to utility grids to filter out harmonics produced by inverters. This produces resonance that causes instability to the overall system. A fractional-order capacitor of impedance  $1/S^\alpha C_\alpha$  is proposed to replace its integer-order counterpart to yield a LC<sup>α</sup> L filter instead of the classical LCL filters. Unlike what is normally used in passive damping, the dynamics of the fractional-order capacitors exhibit intrinsic passive damping effect of order  $\alpha$ , which can be controlled to minimize heat dissipation that is accustomed in passive damping. Besides introducing a single control element, i.e.,  $\alpha$ , the (LC)<sup>α</sup> L filter provides wider bandwidth to mitigate higher order resonant frequencies than its integer-order counterpart. The performance analysis of the proposed filters is verified via numerical simulations.

## Session B1L-D: Communication Circuits I

**Chair:** Rushi Vyas, *University of Calgary*

**Time:** Tuesday, August 6, 2019, 8:00 - 9:30

**Location:** Quorum I & II

### **Signal Point Target Code** ..... 537

<sup>1</sup>Janak Sodha, <sup>2</sup>Todd Moon

<sup>1</sup>University of the West Indies, Barbados; <sup>2</sup>Utah State University, United States

The signal points transmitted from a given modulation scheme are rotated to follow a pre-defined path through the signal constellation diagram to create a novel rate 1/2 systematic block code that allows for trellis based decoding. By setting a predefined target signal point, the input signal points are rotated to overlay the target signal point to create a code trellis of (M-1) initial and final rotation states. Simulation results are presented for rate 1/2 systematic target codes created using the M-ary QAM signal constellations for M = 4 and 16.

### **A Test Comparison of Full/Half Duplex and Sequential RFID Systems for Communication with Magnetic Carbon Steel Pipes** ..... 540

Bailey Tye, Rushi Vyas

University of Calgary, Canada

The ever-growing oil and gas industry has led to the high demand for technologies which accurately sense defects in underground pipelines. Creating a cost efficient, real time monitoring system is very challenging and a rapidly evolving research topic. Radio frequency identification (RFID) based sensors are a hot topic for use with buried pipelines because they do not require batteries and are very affordable. The issue is most RFID systems do not function optimally in the presence of magnetic materials especially magnetic carbon steel pipes that are prevalent in the Oil and Gas industry. There is also the issue of electromagnetic (EM) fields attenuating rapidly through different soil compositions (water, sand, clay). Using magnetic induction-based communication, a comparison between conventional full/half duplex (FDX/HDX) schemes and a sequential (SEQ) based scheme is detailed. Measurements comparison between the two communication systems in the presence of ASTM A-53 carbon steel pipe show a SEQ RFID system offering 8.3 dBm (6.76 times) improvement over the conventional FDX/HDX system.

### **Simple and Low-Cost Measurement Test Setup to Determine the RF, LO and IF Impedances for Designing GaN FET Resistive Mixer** ..... 544

C. Pérez-Wences, J.R. Loo-Yau, P. Moreno

Cinvestav, Mexico

This paper deals with a simple and low-cost test setup capable to measure the impedances needed for designing a FET resistive mixer. The proposed method uses an external signal generator along with one port S-parameters measurement and signal flow theory to determine the impedances at the RF, LO and IF frequencies. A packaged GaN FET is used to design a high linearity FET resistive mixer suitable to down-convert a 2.4 GHz LTE signal to a 0.1 GHz IF signal and the experimental results show a conversion loss of 6.9 dB and ACLR better than 45 dBc.

### **Blocker-Tolerant RF-to-Digital Linearization with a Very Nonlinear Auxiliary Path** ..... 548

Julian Camilo Gomez Diaz, Amir Tofighi Zavareh, Lester Boampong, Sebastian Hoyos

Texas A&M University, United States

This paper introduces a new linearization technique based on signal-component cancellation to remove the third order lumped nonlinearities from the entire receiver chain using a nonlinear auxiliary path. The paper shows that the solution performance improves when the auxiliary path becomes more nonlinear, a rather counter-intuitive property of the proposed technique with several practical implications. The signal component cancellation uses two coefficients that are found adaptively with a novel two-step LMS algorithm in the digital domain. In contrast with previous prominent approaches based on an auxiliary path, the proposed linearization has two significant advantages: 1) it does not estimate the signal nonlinearities used in other techniques for cancellation, and 2) upon convergence of the adaptive algorithm, the digital solution is input-signal independent and therefore is static in steady-state.

## Session B1L-E: Internet of Vehicles (IoV) and Internet of Things (IoT)

**Chair:** Steven Bibyc, *Ohio State University*

**Time:** Tuesday, August 6, 2019, 8:00 - 9:30

**Location:** Salon G & H

### **Collision-Free Navigation and Efficient Scheduling for Fleet of Multi-Rotor Drones in Smart City** ..... 552

*Ahmed Bahabry, Xiangpeng Wan, Hakim Ghazzai, Gregg Vesonder, Yehia Massoud*

Stevens Institute of Technology, United States

Recently, multi-rotor drones, commonly seen as flying Internet-of-things (IoT) devices, have witnessed a drastic usage in many smart city applications due to their three dimensional (3D) mobility and flexibility. Collectively, drones can be used to accomplish different short-term and long-term missions requiring low altitude motion. In such a scenario, an effective routing and scheduling of the drone swarms is required to ensure efficient energy management, collision-free navigation, and accurate mission accomplishment. In this paper, we propose a low complexity framework to determine shortest trajectories and time plans for each member of the fleet while taking into account the different constraints. Collision is avoided by forcing some of the drones to statically hover to allow their peers to safely pass the path segment. Selected scenarios are investigated to show the efficiency of the routing and scheduling framework. Selected scenarios are investigated to show the efficiency of the routing and scheduling framework. The impact of some of the system parameters on the fleet behavior is also investigated.

### **Real-Time Infrastructure-to-Vehicle Communication using RF-Triggered Wireless Sensors** ..... 556

*Owen Pochettino, Sri Harsha Kondapalli, Kenji Aono, Shantanu Chakrabartty*

Washington University in St. Louis, United States

A method for implementing low-latency, long-distance wireless communication between sensors embedded in infrastructure, and fast moving vehicles. This is achieved by using an RF-trigger to selectively enable an active wireless link.

### **Security Taxonomy in IoT – A Survey** ..... 560

*Phillip Williams, Pablo Rojas, Magdy Bayoumi*

University of Louisiana at Lafayette, United States

This paper takes a look at security implementation in some of the major IoT sectors today. With the different case studies on security vulnerabilities in these devices, it is reasonable to say that these sectors viewed security as an afterthought. This is shown by identifying case studies of devices lacking security features/taxonomies. This paper looks at some of the common threats faced by devices in these IoT sectors. This is also a guideline on what security features needs to be integrated in an IoT device to truly say it secure and immune to its common security threats.

### **A CMOS Current Mirroring Integration based Visible Light Receiver for Intelligent Transport Systems** ..... 566

*Moaaz Ahmed, Amine Bermak*

Hamad Bin Khalifa University, Qatar

We present a current mirroring integration (CMI) based VLC receiver for intelligent transport systems. Polarization property of light is used to reject ambient light interference by sending and receiving differential data over adjacent channels. Each channel transmits and receives complimentary data through a set of linear polarizers. The receiver front-end is based on differential CMI topology which integrates the photocurrent over a pair of capacitors followed by a differential charge transfer amplifier (CTA) which performs amplification of differential optical signal and cancellation of background (DC) light up to 100uA. This is followed by a differential comparator with D-flip flop to make decision and latch the resultant data in digital format. Designed and simulated in 0:18um CMOS process, the proposed receiver front-end consumes 42uA current and achieve a data rate of 5MHz with energy consumption of 15pJ/bit.

### **A Low Complexity Space-Time Algorithm for Green ITS-Roadside Unit Planning** ..... 570

*Michael C. Lucic, Hakim Ghazzai, Yehia Massoud*

Stevens Institute of Technology, United States

Roadside Unit (RSU) planning and management is not a straightforward task. Usually, the problem is modeled as an NP-hard mixed-integer combinatorial optimization problem especially when the planner ought to incorporate various problem characteristics. For large-scale problems, heuristic approaches, that achieve a trade-off between execution time and planning performance, can be good enough for making planning decisions. In this paper, we design an iterative reduction heuristic algorithm to maximize the coverage efficiency of a network of RSUs in an urban setting, given a daily amortized budget and other planning constraints. The framework also incorporates capture-and-use solar panels to offset operational electricity costs. We perform a sensitivity analysis, to study the model response to variations. The heuristic shows that variations in both financial as well as communication-related parameters have expected model solution response. We find that in 10% to 50% of the convergence time of the optimal solution, the heuristic found solutions that that had a coverage efficiency around 10% of the optimal solution.



## Session B1L-F: Trusted Electronics and Security I

**Chair:** Srinivas Katkoori, *University of South Florida*

**Time:** Tuesday, August 6, 2019, 8:00 - 9:30

**Location:** Addison

### **An SR Flip-Flop based Physical Unclonable Functions for Hardware Security** ..... 574

*Rohith Prasad Challa, Sheikh Ariful Islam, Srinivas Katkoori*

University of South Florida, United States

Physical Unclonable Functions (PUFs) have emerged as a promising solution to identify and authenticate Integrated Circuits (ICs). In this paper, we propose a novel NAND-based Set-Reset (SR) Flip-flop (FF) PUF design for security enclosures of the area constrained Internet-of-Things (IoT). Such SR-FF based PUF is constructed during a unique race condition that is (normally) avoided due to inconsistency. We incorporate the process variations to leverage the capability of SR-FF to generate the unique identifier of an IC. The SPICE-level simulations presented for 90nm, 45nm, and 32nm technologies in both intra- and inter-chip variations show the robustness of SR-FF PUF in terms of uniqueness, randomness, uniformity, and bit(s) biases. Furthermore, we perform physical synthesis to evaluate the applicability of SR FF PUF on five designs from OpenCores. The estimated overhead for power, timing, and area in three design corners are negligible.

### **A 0.36pJ/bit Analog PUF based on Current Steering DAC and VCO** ..... 578

<sup>1</sup>Mohammadhadi Danesh, <sup>2</sup>Aishwarya Bahudhanam Venkatasubramaniyan, <sup>1</sup>Gaurav Kapoor, <sup>1</sup>Arindam Sanyal

<sup>1</sup>University at Buffalo, United States; <sup>2</sup>Intel Corporation, United States

This paper proposes an analog weak physical unclonable function (PUF). The proposed PUF derives its unique key from random mismatch in a cascode current steering thermometer digital-to-analog converter (DAC). The DAC drives a voltage-controlled 7-stage ring oscillator (RO). MSB of the difference in phase outputs of two ROs generate the PUF response. An N-bit PUF key can be produced from a single proposed PUF cell by running the VCOs for N sampling periods which results in the proposed PUF having the lowest area/bit among weak PUFs. A prototype fabricated in 65nm has an intra-HD of 0.0906 and inter-HD of 0.4859 for 2048-bit PUF key.

### **Supervising Communication SoC for Secure Operation using Machine Learning** ..... 582

<sup>1</sup>Abdelrahman Elkanishy, <sup>1,3</sup>Abdel-Hameed A. Badawy, <sup>1</sup>Paul M. Furth, <sup>1</sup>Laura E. Boucheron,

<sup>2</sup>Christopher P. Michael

<sup>1</sup>New Mexico State University, United States; <sup>2</sup>Sandia National Laboratories, United States;

<sup>3</sup>Los Alamos National Laboratory, United States

Manufacturers normally buy and/or fabricate communication chips using third-party suppliers, which are then integrated into a complex hardware-software stack with a variety of potential vulnerabilities. This work proposes a compact supervisory circuit to classify the operation of a Bluetooth (BT) SoC at low frequencies by monitoring the input power and radio frequency (RF) output of the BT chip passed through an envelope detector. The idea is to inexpensively fabricate an envelope detector, power supply current monitor, and classification algorithm on a custom low-frequency integrated circuit in a trusted legacy technology. When the supervisory circuit detects unexpected behavior, it can shut off power to the BT SoC. In this preliminary work, we proto-type the supervisory circuit using off-the-shelf components. We extract simple yet descriptive features from the envelope of the RF output signal. Then, we train machine learning (ML) models to classify different BT operation modes, such as BT advertising and transmit modes. Our results show ~100% classification accuracy.

### **Design of a Lightweight Reconfigurable PRNG using Three Transistor Chaotic Map** ..... 586

*Aysha S. Shanta, Md Sakib Hasan, Md Badruddoja Majumder, Garrett S. Rose*

University of Tennessee, United States

In this paper, we implemented a lightweight reconfigurable pseudo-random number generator (PRNG). The map generates discrete-time chaotic signals. The chaotic oscillator requires two map circuits to generate chaotic signals. The design is reconfigurable because two map circuits have two bifurcation parameters which can be leveraged to generate multiple random sequences. The design of the PRNG utilizes two chaotic oscillators, analog mux, 10 bit ADC, 2 bit shift register and an XOR gate. The circuit has been implemented in 65 nm CMOS technology with a supply voltage of 1.2 V. The estimated power consumption of the circuit is 2.12 mW and the area overhead is 0.132 mm<sup>2</sup>. The throughput of the proposed PRNG is 100 MS/s. The proposed PRNG can be used for security applications in IoT devices which requires circuits to consume less area and power overhead. The PRNG design passes all the tests in NIST SP 800-22 test suite.

**Analysis and Machine Learning Vulnerability Assessment of XOR-Inverter based Ring Oscillator PUF Design** ..... 590

Noor Ahmad Hazari, Ahmed Oun, Mohammed Niamat

University of Toledo, United States

This paper evaluates an XOR inverter based ROPUF compared to different designs of ROPUF. For vulnerability analysis, it is assumed that an attacker somehow manages to acquire a few CRPs of the total number of CRPs and tries to predict the remaining CRPs from the designed model. A design modification has been made to the ROPUF structure to prevent modeling attacks.

**Session B1L-G: Image/Video Processing and Multimedia Systems**

**Chair:** Hongbin Sun, Xi'an Jiaotong University

**Time:** Tuesday, August 6, 2019, 8:00 - 9:30

**Location:** Salon I & J

**Pulmonary Nodule and Malignancy Classification Employing Triplanar Views and Convolutional Neural Network** ..... 594

Shimaa A. Abdelrahman, Moataz M. Abdelwahab, Mohammed S. Sayed

Egypt-Japan University of Science and Technology, Egypt

Appearance of pulmonary lesions in a Computed Tomography (CT) scan of lung has the potential to become cancerous. Therefore, classification of lesion at early stage is a powerful tool to increase the chance of survival of a patient. In this paper a novel system for lesion classification as either nodule or non-nodule followed by malignancy classification (benign or malignant) is presented. Three dimensional (3D) lung tissue is constructed from the two dimensional (2D) slices of the patient CT scan. Lung is segmented by a thresholding based method, and lesions are extracted with triplanar views, axial, coronal, and sagittal. For classification, two Convolutional Neural Networks (CNNs) are cascaded, where the first network for lesion classification and the second for malignancy classification with concatenated triplaner views as an input in both stages. Experimental results performed on 1010 patients from Lung Image Database Consortium (LIDC) reveal that, the proposed approach achieved the best performance in lesion and malignancy classification with an accuracy of 82.58% and 82.62% respectively compared with existing methods.

**Applying Multiresolution Analysis to Vector Quantization Features for Face Recognition** ..... 598

<sup>1</sup>Ahmed Aldhahab, <sup>2</sup>Taif Alobaidi, <sup>1</sup>Awwab Q. Althahab, <sup>2</sup>Wasfy B. Mikhael

<sup>1</sup>University of Babylon, Iraq; <sup>2</sup>University of Central Florida, United States

Face recognition (FR) based on Facial Parts Detection (FPD) followed by Discrete Wavelet Transform (DWT) / Vector Quantization (VQ) is proposed. The FPD detects nose, eyes, and mouth for each pose. Then, DWT is applied to each detected part for dimensionality reduction / feature selection. Thereafter, VQ is applied to form the final model with four feature groups/person. The Euclidean distance is used to measure the accuracy. Georgia Tech, YALE, FEL, and FERET databases are used to evaluate the FR performance. Recognition accuracies improved while the storage requirements reduced significantly compared to the state-of-the-art approaches.

**Affine Approximation Approach to Matrix Factorization Problem for DOSY** ..... 602

<sup>1</sup>Yuho Tanaka, <sup>2</sup>Kazunori Uruma, <sup>3</sup>Tomoki Nakao, <sup>1</sup>Toshihiro Furukawa

<sup>1</sup>Tokyo University of Science, Japan; <sup>2</sup>Kogakuin University, Japan; <sup>3</sup>JEOL RESONANCE Inc., Japan

Diffusion ordered 2D nuclear magnetic resonance spectroscopy (DOSY) is a molecular structure analysis method, and it is formulated as the non-negative matrix factorization (NMF) problem. This paper proposes a novel algorithm to solve NMF for DOSY based on the affine approximation approach. Simulation results show that the proposed algorithm achieves a high factorization performance and low calculation cost.

**Fast Algorithm with Palette Mode Skipping and Splitting Early Termination for HEVC Screen Content Coding** ... 606

<sup>1</sup>Emad Badry, <sup>2</sup>Ahmed Shalaby, <sup>1</sup>Mohammed S. Sayed

<sup>1</sup>Egypt-Japan University of Science and Technology, Egypt; <sup>2</sup>Benha University, Egypt

Screen content videos have special features such as frequently repeated patterns, limited number of colors and non-noisy regions. It differs from the natural scene sequences which require more proper coding tools. New modes were incorporated into the High Efficiency Video Coding (HEVC) standard such as Palette mode (PLT) and Intra Block Copy (IBC) to target the special nature of these videos. The new tools achieve higher coding performance, however, they bring remarkable computational complexity. In this paper, a new fast scheme is proposed to reduce the HEVC encoding time for the screen content videos. It depends on the number of distinct colors inside the current block. The new approach is implemented and simulated using HEVC screen content extension software HM 16.7+SCM 6. The results show that our scheme reduces the encoding time by 24.46% with small increment of 2.1% in the bitrate.

**Extended Neighbourhood Filter for LDR Displays** ..... 610

<sup>1</sup>*Sijin Felix P*, <sup>1</sup>*Joshin John Mathew*, <sup>2</sup>*Akshay Maan*, <sup>2</sup>*Alex Pappachen James*

<sup>1</sup>ARS Traffic & Transport Technology, India; <sup>2</sup>, <sup>3</sup>Nazarbayev University, Kazakhstan

Visual preservation and reproduction of subtle and feeble scene details is challenging during conversion from Hyper-spectral Image (HSI) to Low Dynamic Range (LDR) color images due to poor scene area to pixel density ratio, where a large geographical plane is mapped to a single pixel. This results in an averaging effect or a partial volume effect that affects the visual distinction of fine subtle details. Secondly, HSI data reduction to LDR color image involves sub-band averaging which again affects details distinction, especially structures of feeble strength. The proposed approach addresses this issue and improves the details in the scene for preservation and enhancement by modifying an existing HSI to LDR color image conversion method. An interim, detail enhancement stage is introduced. The results show a clear improvement in visual content reproduction and the numerical quantification also agrees to the same. The results are compared using three data sets and two other methods including the original method being modified.

**Session B2P-H: Neural Systems and Deep Learning**

**Chair:** Fakhreddine Ghaffari, *University of Paris Seine*

**Time:** Tuesday, August 6, 2019, 11:30 - 12:30

**Location:** Salon F

**Improving the Performance of Serial Arc Detection using VMD and Deep Neural Network** ..... 614

<sup>1</sup>*Sangik Lee*, <sup>1</sup>*Seokwoo Kang*, <sup>1</sup>*Taewon Kim*, <sup>2</sup>*Seungsoo Lee*, <sup>2</sup>*Manbae Kim*

<sup>1</sup>KESCO, Korea; <sup>2</sup>Kangwon National University, Korea

Serial arc is one of factors causing electrical fires. Over past decades, a variety of researches have been carried out to detect arc signals using frequency characteristics, wavelet analysis and statistical features. However, the usage of those features has shown low arc-detection performance. To solve this, we employ variational mode decomposition (VMD) to generate more time-domain signals, from which statistical features are computed from VMD mode signals, providing more informative features. Using a deep neural network (DNN) as an arc classifier, experiments validate that the VMD could improve the arc-detection performance by 4 percent.

**A Novel Reconfigurable Hardware Architecture of Neural Network** ..... 618

<sup>1</sup>*Kasem Khalil*, *Omar Eldash*, <sup>1,2</sup>*Bappaditya Dey*, <sup>1</sup>*Ashok Kumar*, <sup>1</sup>*Magdy Bayoumi*

<sup>1</sup>University of Louisiana at Lafayette, United States; <sup>2</sup>imec, Belgium

Neural networks are commonly used in learning applications. The hardware implementation of a neural network is one challenge of a neural network. It is required to design a network to be general for any application. This paper presents a reconfigurable feed-forward neural network which can be used for any application. The proposed method has the flexibility to change the node organization to be suitable for an application. The network is divided into two parts: one part has a fixed node in each layer and the second part includes the reconfigurable nodes. The reconfigurable nodes have the ability to switch from one layer to another until reaching the optimum result. The proposed method is compared with the traditional network, and the result shows the proposed method improves the performance of the network. The hardware implementation of the proposed method is presented using VHDL and Altera 10 GX FPGA.

**Self-Healing Approach for Hardware Neural Network Architecture** ..... 622

*Kasem Khalil*, *Omar Eldash*, *Ashok Kumar*, *Magdy Bayoumi*

University of Louisiana at Lafayette, United States

Neural Network can be used for many applications and it is important to keep it works without fault. Self-healing neural network became important towards reliable Neural Network (NN). Self-healing is the ability to detect and fix a fault in the system. Most of the current self-healing NN are based on replication of hardware nodes which spend higher area overhead. The proposed self-healing approach is used to reduce the area overhead and it is suitable for complex NN. The proposed method a shared operation and spare node in each layer which compensates any faulty node in the layer. Each faulty node will be recovered by its neighbor node, and the neighbor node performs the faulty node and its operations sequentially. In the case of the neighbor is faulty, the spare node will compensate them. The proposed method is implemented using VHDL and the simulation results are obtained using Altira 10 GX FPGA for a different number of nodes. The area overhead is very small for a complex network. The reliability of the proposed method is studied and compared to the traditional NN.

**Accelerating Deterministic and Stochastic Binarized Neural Networks on FPGAs using OpenCL** ..... 626

*Corey Lammie*, *Wei Xiang*, *Mostafa Rahimi Azghadi*

James Cook University, Australia

In this paper, we introduce, to the best of our knowledge, the first FPGA-accelerated stochastically binarized DNN implementations, and compare them to implementations accelerated on both GPUs and FPGAs. All our developed networks are trained and benchmarked using the popular MNIST and CIFAR-10 datasets. For our binarized and conventional FPGA-based networks, we achieve a >16-fold improvement in power consumption, compared to their GPU-accelerated counterparts. Also, our binarized FPGA-based networks require >25% shorter inference times, compared to their GPU-based counterparts.

**Slim LSTM NETWORKS: LSTM\_6 and LSTM\_C6** ..... N/A

*Atra Akandeh, Fathi M. Salem*

Michigan State University, United States

We show that parameter-reduced slim variants of Long Short-Term Memory (LSTM) Recurrent Neural Networks (RNN) are comparable in performance to the standard LSTM RNN on two diverse benchmark datasets, namely, the review sentiment IMBD and the 20 News-group datasets. We focus on two of the simplest slim variants, namely LSTM\_6 (i.e., standard LSTM with three fixed constant gates) and LSTM\_C6 (i.e., LSTM\_6 with further reduced memory-cell input block). We demonstrate that these two aggressively reduced-parameter variants are competitive with the standard LSTM when hyper-parameters, e.g., the learning rate, number of hidden units and/or gate constants are set properly. These slim architectures enable training speedup and hence these networks would be more suitable for online training and inference onto portable devices with relatively limited computational resources.

**Q-Learning based Routing Scheduling for a Multi-Task Autonomous Agent** ..... 634

<sup>1,2</sup>*Omar Bouhamed, <sup>2</sup>Hakim Ghazzai, <sup>1</sup>Hichem Besbes, <sup>2</sup>Yehia Massoud*

<sup>1</sup>University of Carthage, Tunisia; <sup>2</sup>Stevens Institute of Technology, United States

Reinforcement Learning. The objective is to employ an autonomous agent to cover the maximum of pre-scheduled tasks spatially and temporally distributed in a given geographical area over a pre-determined period of time. In this approach, we train the agent using Q-learning, an off-policy temporal difference learning algorithm, that finds effective optimized solution. The agent uses the feedback received from previously taken decisions to learn and adapt its next actions accordingly. A customized reward function was developed to consider the time windows of task and the delays caused by agent navigation between tasks. Numerical simulations show the behavior of the autonomous agent for different selected scenarios and corroborate the ability of Q-learning to handle complex vehicle routing problems with several constraints.

**Investigation of Feature Inputs for Binary Classification of Ultrasonic NDT Signals using SVM and Neural Networks** ..... 638

*Kushal Virupakshappa, Erdal Oruklu*

Illinois Institute of Technology, United States

The main objective of this study is to classify the ultrasonic A-scan data either as flaw echoes or clutter echoes (no flaw). The signal pre-processing has been done using Discrete Wavelet Transform (DWT). The refined low pass output has been used as feature input to the machine learning algorithms either directly or as a power signal. In case of SVM, direct low pass output in windowed format was tested with linear kernel and Radial Basis Function (RBF) kernel and the power signal of the low pass DWT in the windowed format was also tested with linear kernel and RBF kernel. SVM simulation results show that the direct low pass signal with linear kernel fails to converge while power of the low pass DWT achieves an accuracy of around 95%. RBF kernel accuracy was around 98% irrespective of the format of the signal. In case of Neural Network, both the direct low pass output and the power of the low pass output were tested and it was found that the direct low pass output with NN yielded 94% accuracy while the power of the low pass output with NN yielded an accuracy of 98%.

**Nondestructive Reading and Refreshment Circuit for Memristor-Based Neuromorphic Synapse** ..... 642

<sup>1</sup>*A.H. Hassan, <sup>1,2</sup>Hassan Mostafa*

<sup>1</sup>Cairo University, Egypt; <sup>2</sup>Zewail City of Science and Technology, Egypt

Memristor, the fourth circuit element found ten years ago, has attracted most scientific and engineering community pioneers. Its proficiency in nanoscale devices makes it very useful in today's new fast circuit applications. Neuromorphic computing is the new processing technique which is brain-inspired rather than old von-Neumann processors. The main advantage of using memristor in neuromorphic is that it contains both the processing and storing blocks in one place. The main components of any neural networks are the neuron and synapse. In this paper, a recent memristor-based synapse used in literature is introduced with rather a nondestructive reading mechanism for the stored weight in the memristor.

**A Comparison of Artificial Neural Network(ANN) and Support Vector Machine(SVM) Classifiers for Neural Seizure Detection** ..... 646

<sup>1</sup>*Mohamed A. Elgammal, <sup>1,2</sup>Hassan Mostafa, <sup>3</sup>Khaled N. Salama, <sup>1</sup>Ahmed Nader Mohieldin*

<sup>1</sup>Cairo University, Egypt; <sup>2</sup>Zewail City of Science and Technology, Egypt;

<sup>3</sup>King Abdullah University of Science and Technology, Saudi Arabia

In this paper, two different classifiers are software and hardware implemented for neural seizure detection. The two techniques are support vector machine(SVM) and artificial neural networks(ANN). The two techniques are pretrained on software and only the classifiers are hardware implemented and tested. A comparison of the two techniques is performed on the levels of performance, energy consumption and area. The SVM is pretrained using gradient ascent (GA) algorithm, while the neural network is implemented with single hidden layer. It is found that the ANN consumes more power than the SVM by a factor of 4 with almost the same performance. However, the ANN finishes classification in much less number of clock cycles than the SVM by a factor of 34.

**VAWS: Vulnerability Analysis of Neural Networks using Weight Sensitivity** ..... 650

<sup>1</sup>Muluken Hailesellasiye, <sup>1</sup>Jacob Nelson, <sup>2</sup>Faiq Khalid, <sup>1</sup>Syed Rafay Hasan

<sup>1</sup>Tennessee Technological University, United States; <sup>2</sup>Vienna University of Technology, Austria

Security vulnerabilities in machine learning (ML), especially in deep neural networks (DNN), is becoming a concern. Various techniques have been proposed, including data manipulations and model stealing. However, most of them are focused on ML algorithms and target threat models that require access to training dataset. In this paper, we present a methodology that analyzes the DNN weight parameters under the threat model that assumes the attacker has the access to the weight memory only. This analysis is then used to develop an attack that manipulates weight parameters with respect to their sensitivity. To evaluate this attack, we implemented our methodology on a MLP trained on IRIS dataset and LeNet (DNN architecture) trained on MNIST dataset.

**Session B2P-J: Linear and Nonlinear Systems**

**Chair:** *University of Paris Seine*

**Time:** Tuesday, August 6, 2019, 11:30 - 12:30

**Location:** Salon F

**Transimpedance Amplifier Graphical Design Technique** ..... 654

*Todd Wey*

Lafayette College, United States

A transimpedance amplifier (TIA) graphical design technique including transimpedance gain, signal bandwidth, feedback loop stability, and noise performance is presented. The proposed graphical method allows for a more extensive design tradeoff analysis and is applicable to both compensated and decompensated opamps. The method is validated with Spice simulation and contrasted with published experimental results.

**Design of Analog Circuits for Continuously Changing Constraints using Fixator Norator Pairs** ..... 658

*Reza Hashemian*

Northern Illinois University, United States

This presentation offers a design procedure when one or more constraints are continuously changing in an analog circuit. The components used for this are Fixator Norator Pairs (FNP). It starts with norators, where their variables ( $v$  and  $i$ ) are linearly dependent on the design constraints, represented by fixators. So, when the constraints are changing the norators variable (as circuit components) can change and adjust themselves. It is shown that the linear dependency is applicable to the voltage and current of the norator, but when it comes to replacing it with a resistor the dependency becomes bilinear. So, for  $m$  continuously changing constraints we only need  $m$  corresponding resistors (voltage sources or current sources are also candidates) to vary and tune. A simple and efficient computational method is presented for finding these equivalent resistors. One indication of this efficiency is that, no formal matrix inversion is needed in the entire process.

**Towards a Self-Organizing Deciphering System based on a Wave Digital Emulator** ..... 662

*Karlheinz Ochs, Enver Solan, Dennis Michaelis, Leon Schmitz*

Ruhr-University Bochum, Germany

Current cryptographic systems are based on functions that are easy to compute, yet finding the inverse operation is computationally complex. One of these functions is the prime factorization which is utilized in modern communication systems. Memristive circuits are challenging these standards because they enable self-organizing logic gates (SOLGs) which can be operated in reverse mode, where every node can electively be used as an input or output. So far, only investigations with idealized memristor models have been done. That is because manufacturing costs of real memristors are high. Thus, our goal is to create a highly flexible emulator for an universal SOLG to aid future investigations. We therefore exploit the wave digital algorithm to obtain an emulator which preserves stability, allows for exchangeable memristor models, and enables parameter optimization and sensitivity analyses during runtime for future research.

**Synchronization and Secure Transmission of Data in Incommensurate Fractional-Order Chaotic Systems using a Sigmoid-Like Controller** ..... 666

<sup>1</sup>Juan L. Mata-Machuca, <sup>2</sup>Ricardo Aguilar-Lopez

<sup>1</sup>UPIITA, Instituto Politecnico Nacional, Mexico; <sup>2</sup>Cinvestav, Mexico

In this contribution a control scheme for a class of fractional-order chaotic systems and its application in the synchronization and secure transmission of data problems is designed. The asymptotic stability of the synchronization error and the ultimate bound of the information recovery error are established employing the fractional Lyapunov direct method. The proposed sigmoid-like controller is used as input to the receiver system whose states are asymptotically synchronized with the transmitter system. The technique has been applied in the synchronization and secure communications of the incommensurate fractional-order Rössler and Chen systems.

## Session B2P-K: Digital Signal Processing

**Chair:** *University of Paris Seine*

**Time:** Tuesday, August 6, 2019, 11:30 - 12:30

**Location:** Salon F

### **High-Speed Sparse Ising Model on FPGA** ..... 670

*Akira Minamisawa, Ryoma Imura, Takayuki Kawahara*

Tokyo University of Science, Japan

To implement the Ising model on hardware and create "things" able to process optimization for the future IoT, a speeding up method is proposed for speeding up an Ising model. By implementing a  $6 \times 6$  spin Ising model in a 16 nm CMOS FPGA, we found that the traveling salesman problem and SVM can be solved. By implementing parallel updates, higher processing speed is achieved. Furthermore, the Ising model in which the interactions were reduced on the basis of the sparsity as more than nine times faster than the fully connected Ising model.

### **A Fully Adaptive Feedback ANC System Employing Online Estimation of the Cancellation Path** ..... 674

*Muhammad Tahir Akhtar*

Nazarbayev University, Kazakhstan

The filtered-x least mean square (FxLMS) algorithm for active noise control (ANC) systems requires filtering of the reference signal via the cancellation path modeling (CPM) filter. The CPM filter may be available from the offline experiments. However, in many practical situations the online estimation of CPM filter may be needed due to the possible time-varying nature of the cancellation path. This paper investigates estimation of cancellation path during the online operation of the FxLMS-based feedback-type ANC system. The key idea in the proposed approach is to employ a gain-controlled probe noise mixed with the cancellation signal. The gain-factor for the probe noise is adjusted such that a large-level probe signal is used during the transient state of the ANC system. This improves the convergence of the cancellation path estimation process. As the ANC system converges, the level of the probe noise is reduced to achieve a good noise reduction performance. Simulation results demonstrate the effectiveness of the proposed method.

### **Wedge Filters Designed from 1D Digital Prototypes** ..... N/A

*Radu Matei*

Gheorghe Asachi Technical University, Romania

This work proposes an efficient analytic method for designing a class of 2D filters useful in image processing, namely wedge-shaped filters, which can be considered components of a directional filter bank. The design starts from a 1D digital filter prototype transfer function. Using accurate approximations and specific frequency mappings, first an unilateral, half-plane filter with a given orientation is obtained. Using two such unilateral 2D filters with imposed orientation angles, a desired directional wedge filter is derived, with specified orientation and aperture angles. Its transfer function results directly in a factored form, which is an advantage in implementation. The resulted wedge filter is parametric and tunable, since the specified parameters occur in the final matrix form of the filter transfer function.

### **Efficient Time Series Forecasting using Time Delay Neural Networks with Domain Pre-Transforms** ..... 682

*Masoumeh Kalantari Khandani, Wasfy B. Mikhael*

University of Central Florida, United States

Time series forecasting has application in many domains. If the state of a system of interest can be modeled as a time series, the prediction of the future state can be viewed as a time series forecasting problem. There are countless examples of such applications ranging from weather forecasting to economic metric prediction or predicting a vehicle's position. The time scale of these problems may be very different, but they are all essentially time series. While there are many different methods for time series prediction, Time Delay Neural Networks (TDNNs) are one of the main tools for this purpose that have recently received attention. While most TDNNs may be shallow networks, other networks such as LSTM (Long Short-Term Memory) can also be used for this purpose; however, training time of LSTM is considerably more than FFTN. In this paper, we examine how a transform layer (called pre-transform layer) applied to the beginning layer of a TDNN can significantly reduce training time, while also maintaining accuracy or moderately improving it.

### **VLSI Architecture Design of 9/7 Discrete Wavelet Transform for Image Processing** ..... 686

*<sup>1</sup>Sadaf Javed, <sup>1</sup>Ch. Jabbar Younis, <sup>1</sup>Mehboob Alam, <sup>2</sup>Yehia Massoud*

<sup>1</sup>Mirpur University of Science and Technology, Pakistan; <sup>2</sup>Stevens Institute of Technology, United States

In image processing, transform coding de-correlate images to pre-condition them for efficient compression. In this work, we propose VLSI architecture design of a hardware-efficient 9/7 Discrete Wavelet Transform (DWT). The architecture takes advantage of Canonical Singed Digit (CSD) and Distributed Architecture (DA) to represent and optimally distribute coefficients to reduce the number of adder and shift registers. In addition, the co-efficient multiplication also exploits the horizontal and vertical redundancy in the architecture to reduce the hardware computational complexity. The result is a filter based designed architecture exploiting data path diagram of a CSD represented coefficients, which selectively finds sum of products to give minimum hardware realization. The proposed architecture is modeled and simulated using HDL (Hardware Description Language). A comparison with filter-based architectures of 9/7 DWT reveals a saving up to 18.75% in hardware. The designed solution is hardware efficient and provides a low-power architecture for high-speed real time applications.

## Session B2P-L: System Architectures and Embedded Systems II

**Chair:** *University of Paris Seine*

**Time:** Tuesday, August 6, 2019, 11:30 - 12:30

**Location:** Salon F

### **HLS based Optimizations of an FPGA Hardware Design for Plenoptic Image Processing Algorithm** ..... N/A

*Faraz Bhatti, Thomas Greiner*

Pforzheim University, Germany

Optical 3D image processing algorithms are used in a wide range of applications, such as research, healthcare, industry automation. Generally, such algorithms consist of computation intensive instructions. The performance of general purpose processor based system is a bottleneck because of its sequential nature. FPGA based hardware solution can be an alternative for such problems. Due to its architecture, FPGA can exploit spatial and temporal parallelization and hence the performance with respect to execution time and area can be improved. However, creating hardware with the help of a hardware description language (HDL), such as VHDL, is a complex and time taking process. High-level synthesis (HLS) tools can be employed to resolve this issue. This paper discusses the approach to optimize the HLS based hardware architecture for plenoptic 3D image processing algorithm. It is an iterative process that requires low-level knowledge of the hardware workflow. The results show that the performance is improved.

### **10 GHz Standing Wave Oscillator based Clock Distribution Network Considering Distributed Capacitance** ..... 694

*Gyunam Jeon, Yong-Bin Kim*

Northeastern University, United States

The paper presents 10 GHz standing wave oscillator (SWO) minimizing distributed capacitance  $C_d$  (distributed capacitance generated from multiple cross-coupled pairs (CCP)) for the clock distribution network. The conventional SWOs have been proposed for a negative resistance  $g_d$  (an equivalent transconductance per CCP) to get rid of conductance in RLGC extracted from a transmission line. The  $C_d$  can not only increase its phase constant but also decrease the unit length of the transmission line. Therefore, the  $C_d$  has to be minimized for better performance in the SWO. In the proposed SWO, MOS varactors,  $C_{var}(V)$  (voltage controlled capacitance), are added to minimize the parasitic capacitance between M1 drain and M2 drain to minimize the capacitance  $c_d$  (equivalent capacitance per CCP) caused by the parasitic capacitors. The proposed SWO generates the admittance  $(0.5(-g_{m1}-g_{m2}-sC_{var}(V)+g_{ds1,2}+g_{ds3,4}+s(C_{gs1,2}+C_{gs3,4}))$ . The FOM ( $\omega d$ ) of the proposed approach is about  $83 \times 10^9 \text{ Hz/unit CCP}$ , compared with  $71.6 \times 10^9 \text{ Hz/unit CCP}$  of the conventional design. The design is simulated by a 180nm CMOS technology node with 1.8V power supply, and the total power consumption is 5.4 mW.

## Session B2P-M: Communication Systems and Broadband Networks

**Chair:** *University of Paris Seine*

**Time:** Tuesday, August 6, 2019, 11:30 - 12:30

**Location:** Salon F

### **An Enhanced Error Control Scheme in Real-Time Wireless Sensor Networks** ..... N/A

<sup>1</sup>*Kamaldeen Ayodele Raji*, <sup>2</sup>*Kazeem Alagbe Gbolagade*, <sup>3</sup>*Ayisat Wuraola Yusuf-Asaju*

<sup>1</sup>Kwara State Polytechnic, Nigeria; <sup>2</sup>Kwara State University, Nigeria; <sup>3</sup>University of Ilorin, Nigeria

An improved reverse converter with error control scheme conspiring Redundant Residue Number System (RRNS) to boost the correctness of received message is proposed for real-time WSNs. The system utilized moduli set  $\{2n+1-1, 2n, 2n-1\}$  with additional redundant moduli set  $\{2n+1+3, 22n-3\}$  in order to achieve higher error correction. Maximum likelihood was utilized to identify and correct the corrupted values to the original data. The result obtained shows that the proposed moduli set provides low vitality utilization and c

### **Efficient Calibration for Robust Indoor Localization based on Low-Cost BLE Sensors** ..... 702

*Nizam Kuxdorf-Alkirata, Gerrit Maus, Dieter Brückmann*

University of Wuppertal, Germany

The fingerprinting method for indoor localization is associated with a high calibration effort. In order to improve the efficiency of this time-consuming method, a new calibration procedure is proposed. It allows to reduce the calibration effort associated with fingerprinting considerably and ensures a sufficient accuracy at the same time. The proposed procedure takes into account the geometry of the environment subject to study, in order to empirically estimate the distribution of the signal strength at predefined positions. Thus, mobile sensor localization can be carried out robustly and the deviation from real position is less than 0.75 m in about 90% of the cases. This is achieved even though the calibration effort is reduced by almost 84% compared to the original one.

**A New Small-Signal Modelling Approach for Analyzing HEMTs over a Broad Frequency Range** ..... 706

*Amirreza Ghadimi Avval, Samir M. El-Ghazaly*

University of Arkansas, United States

A new modelling approach is presented to obtain the 19-element active and passive equivalent circuit element values of high electron mobility transistors over a broad frequency range. In this method, a new technique is introduced to acquire the appropriate extrinsic values of the model suitable for the frequency of operation. The bias-dependent intrinsic values are also obtained using the extracted Y-parameters from a simulation scheme developed in SILVACO. The proposed method addresses the issues and limitations with existing extraction methods regarding their suitability for high-frequency ranges. A finite-difference scheme is also presented to analyze the device which is characterized by its small-signal equivalent circuit.

**An Optimized BCH Decoder Design Architecture for Adaptive M-ary Recording Channels** ..... 710

*Arvindhan Gunasekaran, Nimisha Chinnu Jose, Shayan Srinivasa Garani*

Indian Institute of Science, India

Error correction codes (ECCs) are used in storage devices to overcome noise and to meet stringent reliability requirements. Multi-level recording channels such as flash, phase change memories etc. require adaptive ECC schemes attuned to the recording channel characteristics that degrade over time. Each bit within M-ary coded data is realised via binary encoding using Bose-Chaudhuri-Hocquenghem (BCH) codes and exchanging side information over M-parallel binary coded channels. Designing optimized BCH decoders becomes critical towards high performance decoding circuits. In this paper, we develop a novel pipelined decoding architecture for BCH codes for such applications. Our proposed architecture is 45.8% more area efficient over the architecture proposed in [5] and realized by hardware sharing between the syndrome computation and Chien search stages of the pipeline. Implementation of the proposed design in Kintex-7 field programmable gate array (FPGA) achieves a throughput of 2.11 Gbps and synthesis with UMC's 45 nm technology achieves a throughput of 4.63 Gbps.

**A Highly Efficient Broadband mm-Wave 24-32.5 GHz SiGe PA for Potential 5G Applications** ..... 714

*<sup>1</sup>Jerry Tsay, <sup>1</sup>Jill Mayeda, <sup>1,2</sup>Jerry Lopez, <sup>1</sup>Donald Lie*

<sup>1</sup>Texas Tech University, United States; <sup>2</sup>NoiseFigure Research, United States

We present in this work a highly efficient broadband millimeter-wave power amplifier (mm-wave PA) design in a 90nm SiGe technology for potential 5G applications. The post-layout extraction simulations suggest that the PA achieves broadband power-added efficiency (PAE) >31.4%, gain >8.5 dB, and POUT, sat >13.3 dBm across 24-32.5 GHz, with peak PAE of 40.2% at 26 GHz. The PA shows good linearity with 16-QAM LTE 250 MHz modulated signal input, obtaining ACLR1 of -38.6/-37.3 dBc at 26 GHz with POUT, avg of 6.4 dBm. The PA is also robust against variation in bias  $V_B = 0.83-0.85$  V and supply  $V_{CC} = 1.0-1.4$  V and can be applicable toward multi-band 5G applications.

**DCO Gain Calibration Technique in Fractional-N  $\Delta$ - $\Sigma$  PLL based Two-Point Phase Modulators** ..... 718

*Shaoquan Gao, Hanjun Jiang, Fule Li, Zhihua Wang*

Tsinghua University, China

This paper proposes a digital-controlled oscillator (DCO) gain calibration technique in fractional-N  $\Delta$ - $\Sigma$  phase-lock loop (PLL) based two-point phase modulators. The technique is verified in a 400 MHz/2.4 GHz dual-band combo transceiver. Two-point modulated signal of the 2.4-GHz transmitter is divided by six and then processed in the 400-MHz receiver. Frequency measurement is realized with coordinate rotation digital computer (CORDIC) algorithm in the 400-MHz digital baseband. By reusing the 400-MHz receiver, hardware cost is reduced compared to existing gain calibration techniques. High calibration speed and accuracy is achieved with the aid of the CORDIC algorithm. Simulation results show significant performance improvement in the 2.4-GHz transmitter.

**A 0.045- to 2.5-GHz Frequency Synthesizer with TDC-Based AFC and Phase Switching Multi-Modulus Divider** ..... 722

*Ang Hu, Dongsheng Liu, Kefeng Zhang, Lanqi Liu, Xuecheng Zou*

Huazhong University of Science and Technology, China

A 0.045- to 2.5- GHz wideband frequency synthesizer (FS) with a time-to-digital converter (TDC) based automatic frequency calibration (AFC) and phase switching multi-modulus divider (MMD) for quantization noise suppression is presented in this paper. The counter-based AFC method takes several reference cycles to calculate the instantaneous voltage controlled oscillator (VCO) frequency, while the proposed TDC-based technique needs only 2 cycles. In order to suppress the quantization noise caused by the sigma-delta modulator (SDM) in the MMD, the loop division step is reduced from 2 to 0.5 by adopting the phase switching (PS) technique. The FS is designed and simulated using TSMC 180nm RF CMOS process. The simulation results of the AFC time are less than 1.4  $\mu$ s when employing a 48 MHz reference signal and the quantization noise is suppressed by 12 dB compared to the conventional MMD structure.



## Session B2P-N: Power Electronics and Hybrid Systems

**Chair:** *University of Paris Seine*

**Time:** Tuesday, August 6, 2019, 11:30 - 12:30

**Location:** Salon F

### **Linear, Time-Invariant Model of the Dynamics of a CMOS CC-CP** ..... 726

*Kenneth Palma, Francesc Moll*

Universitat Politecnica de Catalunya, Spain

This paper presents the development of a linear dynamic model of a MOS Cross Coupled Charge Pump (CC-CP) suitable for low voltage energy harvesting systems in the form of a Discrete-Time State-Space set of equations considering the resistive behavior of transistor switches. The dynamic model, easily extendable to a CC-CP of an arbitrary number of stages, includes parasitic elements without loss of generality. The validity of the dynamic model is evaluated through the comparison of Matlab simulations of the model to circuit simulations of an ideal CC-CP.

### **Review and Comparison of Integrated Inductive-Based Hybrid Step-Up DC-DC Converter under CCM** ..... 730

*Wen-Liang Zeng, Chi-Wa U, Chi-Seng Lam*

University of Macau, Macau

Two recent step-up DC-DC converter topologies: dual-path step-up converter (DPUC) and KY converter (KYC), are theoretically analyzed and compared with the conventional boost converter (CBC), in terms of inductor current ripple, efficiency, output voltage ripple, and load transient response performances in this paper. Simulation results are provided to verify the theoretical analysis.

### **A Low-Cost Planar Inkjet-Printed Carbon Nanotube Field Effect Transistor for Sensor Applications** ..... 734

*<sup>1</sup>Md Toriqul Islam, <sup>1</sup>Steven D. Gardner, <sup>1</sup>Ruikuan Lu, <sup>1</sup>Mohammad R. Haider,*

*<sup>1</sup>J. Iwan D. Alexander, <sup>2</sup>Yehia Massoud*

<sup>1</sup>University of Alabama at Birmingham, United States; <sup>2</sup>Stevens Institute of Technology, United States

The semiconductor based transistor is the most essential building block of electronic components, computing applications, and sensors. However, the fabrication of these primary electronic elements is complex and costly, especially when considering flexible electronics for bio-sensing applications. This work proposes a planar inkjet-printed carbon nanotube field effect transistor (CNTFET) on paper and polyethylene terephthalate (PET) substrate to reduce the complexity of the system and lower the cost of conventional fabrication schemes. Single walled carbon nanotubes (SWNTs) are used in this work as semiconductive ink for an inkjet-printer to facilitate and fabricate two types of transistors. Both thin (0.3 mm gate separation) and thick (0.5 mm gate separation) transistors with wide (4 mm) and narrow (2 mm) channel length have shown nearly linear characteristics of resistivity for a range of applied gate voltages. The mathematical model based on experimental results shows great usefulness of the proposed inkjet-printed CNTFET for various electronic applications including bio-sensors, healthcare measurements, and circuits.

### **Current-Voltage-Dual-Mode DC-DC Buck Converter with Adaptive Clock Control** ..... 738

*You-Te Chiu, Yu-Hsuan Liu, Ming-Rui Tsai, Chung-Chih Hung*

National Chiao Tung University, Taiwan

This paper presents a novel high-efficiency and fast-transient current-voltage-dual-mode (CVDM) dc-dc buck converter using adaptive clock controller (ACC). The proposed CVDM control can stably switch the control method between current mode and voltage mode to improve the performance according to different situations. By using the ACC technique, the circuit can dynamically and smoothly adjust the switching frequency during the transient response to improve the undershoot, overshoot voltage, and recovery time. The transient recovery time and undershoot voltage are less than 5 $\mu$ s and 60mV, respectively. Above 90% conversion efficiency can be achieved for load current from 30mA to 600mA.

### **Analysis of Charge Reuse in Switched-Capacitor Power-Converter Drivers** ..... 742

*Mark Lipski, Stefano Gregori*

University of Guelph, Canada

This paper presents a method of reducing the power lost when driving the gate capacitance of CMOS transistors in switched-capacitor power converters. The consequences of the increased rise and fall times on the transistor on resistance are investigated. Additionally, the effectiveness of charge reuse on the transistors of a switched-capacitor voltage doubler is simulated in 65-nm CMOS technology resulting in efficiency improvements.

**Opportunities and Challenges in Desktop-Inkjet based Flexible Hybrid Electronics** ..... 746  
*Mohammad Muhtady Muhaisin, Rafid Adnan Khan, Jonathan Telfort, Wolfgang Heger, Gordon W. Roberts*  
McGill University, Canada

The work-flow and challenges in developing the Flexible Hybrid Electronics prototypes of a wireless transceiver platform and a single stage amplifier using a desktop-inkjet printer are presented. The prototype has been designed using both surface mount and through-hole components to address and overcome the challenges associated with both types of interconnect methods. Various factors involved in building the prototype are analyzed and reliability concerns are addressed. Finally, the amplifier and wireless transceiver platforms are tested to validate the proper functioning of the developed prototypes.

**Design of Microscale Piezoelectric Energy Harvesting System** ..... 750  
<sup>1</sup>Ehab Belal, <sup>1,2</sup>Hassan Mostafa, <sup>1</sup>Amin Nassar  
<sup>1</sup>Cairo University, Egypt; <sup>2</sup>Zewail City of Science and Technology, Egypt

This paper presents design of microscale piezoelectric energy harvesting system, AC/DC converter is used to convert the AC power generated from piezoelectric to DC power, then DC/DC is used to convert the DC voltage to suitable voltage, Analog to digital converter is used to convert the analog signal produced from AC/DC to 8 bits digital signal then feed to digital control oscillator that produced the clock for DC/DC and hence guarantee maximum point power tracking of all system based on the input signal.

## **Session B3L-A: SAR ADCs**

**Chair:** Qiyuan Liu, *Qualcomm*

**Time:** Tuesday, August 6, 2019, 13:30 - 15:00

**Location:** Bent Tree I & II

**A Single Channel Bandpass SAR ADC with Digitally Assisted NTF Re-Configuration** ..... 754  
*Sanjeev Tannirkulam Chandrasekaran, Gaurav Kapoor, Arindam Sanyal*  
University at Buffalo, United States

A single channel band-pass (BP) SAR ADC has been presented in this work. The proposed ADC uses a maximum likelihood estimator (MLE) to estimate the SAR residue similar to a two-stage architecture. The ADC output is obtained by subtracting a delayed version of the MLE estimate from the SAR output thus generating a noise transfer function (NTF) which can be re-configured by changing the delay. A 65nm BP ADC prototype achieves a 67.8dB SNDR when clocked at 2MS/s over a 79kHz bandwidth. The ADC consumes 13uW from a 1V supply leading to a 166dB schreier FoM.

**Testing and Modeling of a SAR ADC for Cryogenic Applications** ..... 758  
<sup>1</sup>Will Norton, <sup>1</sup>Ziming Wang, <sup>1</sup>Benjamin J. Blalock, <sup>2</sup>Jean Yang-Scharlotta, <sup>2</sup>Miryeong Song,  
<sup>2</sup>Mohammad Ashtijou, <sup>2</sup>Mohammad Mojarradi

<sup>1</sup>University of Tennessee, United States; <sup>2</sup>Jet Propulsion Laboratory, United States

We investigate and model the effects of extreme low temperature on a commercial mixed-signal device. We then use the measured results to develop a black-box temperature-sensitive model. The black-box model consists of the INL function which expresses deviation in converter decision points from their ideal location, characterized across output code and temperature. In addition, a Simulink model of a SAR ADC is described.

**An 8-B 2b/Cycle Asynchronous SAR ADC with Capacitive Divider based RC-DAC** ..... 762  
*Jiu Xiong, Jiajun Ren, Jin Liu*  
University of Texas at Dallas, United States

This paper presents a 2b/cycle asynchronous SAR ADC with a capacitive divider based RC-DAC. The new architecture reduces the number of capacitors and resistors, leading to a smaller die area and lower hardware cost. It also allows for a new timing scheme with a merged sampling-conversion cycle to increase the conversion speed. An 8-b SAR ADC with the proposed architecture is designed in 180nm CMOS technology operating at sampling rate of 65MS/s. The post-layout simulation shows the proposed SAR ADC can achieve SNDR of 45.16dB at near-Nyquist frequency and occupies an active area of 0.045mm<sup>2</sup>. The FOM under a 1.2V&1.8V supply voltage is 216fJ/conversion-step with power consumption of 2.07mW.

**A Band-Pass Noise-Shaping Modulator using the Error-Feedback Structure on a 10-Bit SAR ADC** ..... 766

*Longheng Luo, Shuai Li, Jipeng Wei, Yimin Wu, Fan Ye, Junyan Ren*  
Fudan University, China

This paper presents a band-pass noise-shaping (NS) successive-approximation-register (SAR) analog-to-digital converter (ADC) with a second-order modulator which is comprised of a fully passive switched-capacitor (SC) filter and a gain-booster dynamic amplifier. It employs the error-feedback (EF) structure in a simple method to implement the complicated noise transfer function (NTF) zeros, which enhances the noise-shaping capability by minimally modifying a standard SAR ADC. Designed in 28 nm CMOS process, the prototype of proposed NS-SAR ADC achieves 76.84 dB signal-to-noise and distortion ratio (SNDR) with the bandwidth between 20 and 40 MHz and the FoMw is only 2.24 fJ/step at the oversampling ratio (OSR) of 5.

**A 500-MS/s 8.4-ps Double-Edge Successive Approximation TDC in 65 nm CMOS** ..... 770

<sup>1</sup>Rashed Siddiqui, <sup>1</sup>Fei Yuan, <sup>2</sup>Yushi Zhou

<sup>1</sup>Ryerson University, Canada; <sup>2</sup>Lakehead University, Canada

This paper presents an 8.4 ps 500 MS/s 4-bit successive approximation register time-to-digital converter (SAR-TDC). The TDC utilizes both the rising and falling edges of the cyclic signals defining the time input to perform time-to-digital conversion thereafter to low both the frequency of the cyclic signals and the power consumption of the system generating these signals by 50%. Pre-skewing is utilized to improve the resolution of the digital-to-time converter (DTC) subsequently the resolution of the TDC. Both the design and performance of the double-edge SAR TDC are compared with those of a corresponding single-edge SAR TDC. The TDCs was designed in a TSMC 65 nm CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM4 device models. Simulation results show at 500 MS/s, the TDC achieves a SFDR of 37.6, a SNDR of 25.5 dB, a resolution of 8.4 ps while consuming 0.86 mV.

**Session B3L-B: Amplifiers I**

**Chair:** Igor Filanovsky, *University of Alberta*

**Time:** Tuesday, August 6, 2019, 13:30 - 15:00

**Location:** Preston Trail I & II

**A Chopper Instrumentation Amplifier with Fully Symmetric Negative Capacitance Generation Feedback Loop and Online Digital Calibration for Input Impedance Boosting** ..... 774

*Safaa Abdelfattah, Aatmesh Shrivastava, Marvin Onabajo*  
Northeastern University, United States

A symmetric chopper instrumentation amplifier architecture with two identical 8-bit digitally programmable capacitor banks and online digital calibration block are presented. Designed for long-term brain signal monitoring applications, the feedback capacitor banks generate negative capacitance to cancel the input capacitance from electrode cables to boost the input impedance to above 2 gigaohms at 10Hz. These banks are controlled by an automatic digital background calibration that includes an oscillation prevention scheme to ensure stable operation. A chopping technique is introduced to enhance the noise performance of the instrumentation amplifier in combination with the capacitive feedback loop that also contains chopping switches.

**Gain and Bandwidth Enhanced Class-AB OTAs** ..... 778

<sup>1</sup>Shirin Pourashraf, <sup>1,2</sup>Jaime Ramirez-Angulo, <sup>3</sup>Alejandro Roman-Loera, <sup>1</sup>Manaswini Gangineni

<sup>1</sup>New Mexico State University, United States; <sup>2</sup>INAOE, Mexico; <sup>3</sup>Autonomous University of Aguascalientes, Mexico

Efficient class-AB OTAs with enhanced gain bandwidth, open loop gain, output current, and slew rate are presented. they are based on a gm-boosting technique (at least factor of two) and also use dynamically biased cascode transistors to achieve high gain and output currents much larger than the bias current. Measurement results of 180 nm CMOS test chip prototypes validate the improvements.

**Low-Voltage Tracking RC Frequency Compensation in Two-Stage Operational Amplifiers** ..... 782

*Yu-Wen Kuo, Pavan Kumar Ramakrishna, Ajmal Vadakkan Kayyil, David J. Allstot*  
Oregon State University, United States

A process, voltage, and temperature (PVT) insensitive low-voltage tracking RC compensation scheme is described which cancels the pole due to the load capacitance using a Miller zero generated by the compensation network. A low-voltage constant current source with no back-gate effect (a so-called "k' generator") is used to provide the bias currents for the OTA. The architecture, implemented in a TSMC 180nm CMOS process, achieves a 2X power reduction compared to a conventional active-RC compensation scheme. Small-signal settling times are compared across process corners for both approaches. The low-voltage approach is shown to be more robust than the latter which suffers slower settling due to the formation of doublets.

**Ultra Low Voltage Variable Gain Cherry-Hooper Amplifier with 1MHz Constant Bandwidth, 1.7 $\mu$ W Power Dissipation and  $\pm$ 0.2V Supply ..... 786**

<sup>1</sup>Hector Daniel Rico-Aniles, <sup>1,2</sup>Jaime Ramirez-Angulo, <sup>3</sup>Antonio J. Lopez-Martin, <sup>4</sup>Ramon G. Carvajal,

<sup>2</sup>Jose Miguel Rocha, <sup>2</sup>Alejandro Diaz-Sanchez

<sup>1</sup>New Mexico State University, United States; <sup>2</sup>INAOE, Mexico; <sup>3</sup>Public University of Navarre, Spain;

<sup>4</sup>Universidad de Sevilla, Spain

An ultra-low-voltage low-power amplifier is introduced. The design is based on the Cherry-Hooper architecture and operates with a  $\pm$ 0.2V supply and  $\pm$ 190mV linear input range. It has an approximately constant bandwidth of 1MHz with a power consumption of 1.7 $\mu$ W. The low-voltage operation is achieved using floating batteries that keep the gates of all differential pairs at a constant value close to the upper rail with large input signal variations. It has a figure of merit of 2.61 MHzpF/ $\mu$ W for a nominal gain A=15.6.

**A Regulated-Cascode based Current-Integrating TIA RX with 1-tap Speculative Adaptive DFE ..... 790**

<sup>1</sup>Antroy Roy Chowdhury, <sup>2</sup>Nijwm Wary, <sup>1</sup>Pradip Mandal

<sup>1</sup>Indian Institute of Technology Kharagpur, India; <sup>2</sup>University of Toronto, Canada

In this paper, an energy efficient receiver(Rx) with a regulated-cascode based current-integrating TIA (RGC-CI-TIA) has been presented. Use of RGC-CI-TIA over conventional common-gate (CG) CI-TIA eliminates the need of additional passive termination improving the current efficiency and also results in substantial power reduction of the Rx. The Rx also deploys a speculative 1-tap current-integrating decision-feedback equalizer (DFE) which along with a 2-tap Tx feed-forward equalizer (Tx-FFE) compensate 18 dB of loss at 2.5 GHz of a 41" FR4 PCB trace. The proposed Rx achieves a channel signal-swing of 20 mVppd and input sensitivity of 1.2 mVppd by means of a significant voltage gain of 15 offered by the RGC-CI-TIA. The Rx has been designed in 180 nm CMOS technology and consumes 5.25 mW from a 1.8 V supply for a data rate of 5 Gb/s resulting in an energy efficiency of 1.05 pJ/bit.

**Session B3L-C: Integrated DC/DC Converters**

**Chair:** Jose Silva-Martinez, *Texas A&M University*

**Time:** Tuesday, August 6, 2019, 13:30 - 15:00

**Location:** Mesquite I

**A Novel Single-Input-Multiple-Output DC/DC Converter for Distributed Power Management in Many-Core Systems ..... 794**

Xingye Liu, Paul Ampadu

Virginia Polytechnic Institute and State University, United States

We propose a novel single-input-multiple-output DC-DC converter as a distributed power management solution for large-scale many-core systems. From 1V input, output voltages range from 0.33V to 0.94V and supports up 60V/ $\mu$ s transitions. Maximum voltage ripple is limited to 50mV and three output voltages remain stable with a worst-case voltage droop of 30mV during load transitions. Cross regulation is minimized and only 28mV shift is observed at low-power Channel-3. Simulated in 32nm CMOS SOI technology with three in-package air-core inductor models, peak efficiency achieved at high-power Channel-1 is 92% and peak overall efficiency is 87.6% when all channels are delivering full power.

**Lowest  $V_{IN}$  Possible for Switched-Inductor Boost Converters ..... 798**

Tianyu Chang, Gabriel A. Rincón-Mora

Georgia Institute of Technology, United States

The minimum input voltage from which switched-inductor boost converters can draw power is a critical parameter for converters that draw power from low-voltage sources. When batteries are fully discharged, the converter relies on this low-voltage source to wake and supply the system. This paper theorizes the minimum source voltage both with and without a charged battery present. Analyses show that CMOS converters can wake with 44 mV, but not output power until the source voltage is 268 mV. With charged batteries, they can transfer energy with 4.6 mV, but not output net power until the source voltage is 64 mV.

**A Current-Density-Enhanced 12V-to-1.2V/10A, AOT-Controlled, 4-Phase Series-Capacitor Buck Converter with Embedded Current Balancing** ..... 802

<sup>1,2</sup>Shuyu Zhang, <sup>2</sup>Menglian Zhao, <sup>1</sup>Hoi Lee

<sup>1</sup>University of Texas at Dallas, United States; <sup>2</sup>Zhejiang University, China

This paper presents a 4-phase series-capacitor buck converter (SCB) for high step-down-ratio, high-current point-of-load applications. A current-balancing strategy embedded in the adaptive-on-time controller is proposed to effectively address the inductor current mismatch between different phases. This significantly reduces the required size of the external inductor and thus the converter volume. The proposed current balancing scheme also saves 2 current sensors compared to that of the traditional 4-phase interleaved buck converters. Implemented in a 0.35 $\mu$ m CMOS technology, the proposed 4-phase SCB converter with e-mode GaN FETs supports the full load of 10A and achieves the peak power efficiency of 92.5% under 12V-to-1.2V conversion and 2.5MHz/phase operation. The load current is verified to be equally distributed among 4 phases in both steady-state and transient conditions. Compared to state-of-the-art converters from industry and literature, the proposed 4-phase SCB converter simultaneously achieves the highest power efficiency and the largest current density.

**A Fast-Transient Switched-Capacitor DC-DC Converter with a Current Sensing Control Technique** ..... 806

Chi-Wei Chen, Hsin-Shu Chen, Wen-Jong Wu

National Taiwan University, Taiwan

A fully on-chip step-down Switched-Capacitor DC-DC converter with the proposed current sensing control technique is realized in 0.25- $\mu$ m 1P3M High Voltage Mixed Signal CMOS process. Measurement results shows that this current sensing technique gets faster transient response and relatively constant power efficiency by varying the switching frequency ( $F_{sw}$ ) depending on the difference of the current outflow from the converter and the load current.

**Switched-Capacitor Power Converters with Soft Charging via Auxiliary Capacitor Bank** ..... 810

Mark Lipski, Stefano Gregori

University of Guelph, Canada

This paper presents a circuit solution for increasing the efficiency of switched-capacitor power converters utilizing a soft charging technique. The technique is based on an auxiliary capacitor bank that reduces the energy losses associated with parasitic capacitances. The effective reduction in the parasitic capacitances is calculated, and a brief analysis of the design trade-offs is provided. The technique is then applied to a voltage doubler, and simulated in comparison to a standard converter.

**Session B3L-D: Communication Circuits II**

**Chair:** Steven Bibyc, *Ohio State University*

**Time:** Tuesday, August 6, 2019, 13:30 - 15:00

**Location:** Quorum I & II

**Trade-Offs between Data and Power Transfer in Near-Field Inductive Links** ..... 814

Parisa Dehghanzadeh, Hossein Zamani, Soumyajit Mandal

Case Western Reserve University, United States

This paper studies the fundamental trade-off between power transfer efficiency (PTE) and spectral efficiency for simultaneous power and data transfer through near-field inductive links. In particular, it shows how the highest bit rate achievable for a given bit error rate (BER), which is a measure of spectral efficiency, varies versus PTE for several common modulation schemes. The schemes studied include BPSK, QPSK, 8PSK, FSK, and ASK with various modulation depths (30% and 50%). Circuit simulations of an optimized inductive link in air, saline, and tissue are used to estimate PTE for each modulation scheme. Also, a theoretical model is used to simulate the received BER for the same set of schemes.

**System Design of a High-Temperature Downhole Transceiver: Part I – Receiver** ..... 818

Brannon Kerrigan, Fariborz Lohrabi Pour, Dong Sam Ha

Virginia Polytechnic Institute and State University, United States

The paper presents a system level design of a receiver for high-temperature downhole communications. The receiver achieves required specifications necessary to have flexibility between power consumption and performance. The budget analysis considering the minimum system specifications for downhole communication is done. The simulations are performed in AWR design environment software. The simulation results show that the receiver can support a data rate up to 68 Mbps at 250 °C using Quadrature Phase Shift Keying (QPSK) modulation. Detailed simulation results and temperature effects on receiver specifications are included to prove its superior and reliable performance at high temperature using the 2.4 GHz – 2.5 GHz ISM band for the transceiver.

**System Design of a High-Temperature Downhole Transceiver: Part II – Transmitter** ..... 822

*Brannon Kerrigan, Fariborz Lohrabi Pour, Dong Sam Ha*

Virginia Polytechnic Institute and State University, United States

This paper presents a system level design of a transmitter for high-temperature downhole communications. The transmitter aims to operate up to 250 °C. The transmitter is simulated in the AWR design environment. The simulation results indicate that the transmitter can adaptively support a data rate up to 170 Mbps for 32-QAM at 250 °C across ten channels. Simulation results also show that the proposed transmitter operates reliably over the temperature range of 25 °C to 250 °C.

**Single Ended and Differential Passive RF Impedance Tuners for 2.4 GHz ISM Band Applications** ..... 826

<sup>1</sup>*Ram Krishna, <sup>2</sup>Abhishek Kumar, <sup>2</sup>Sankaran Aniruddhan*

<sup>1</sup>Birla Institute of Technology and Science, Pilani, India; <sup>2</sup>Indian Institute of Technology Madras, India

This paper presents the design of two electronically tunable passive RF impedance tuners operating between 2.4 GHz and 2.5 GHz. Theoretical analysis and simulation were performed on two pi matching networks in cascade which helped in increasing the load voltage standing wave ratio (VSWR) coverage. The linearity of the optimized single ended matching network was improved by converting it into a differential structure. Both the impedance tuners based on this theory were fabricated on a two layered FR4 PCB. The fabricated single ended tuner was tested for load impedance variation up to  $VSWR \leq 9.5$  wherein insertion loss stayed between 0.4 dB and 5.1 dB. The differential network was tested for load impedances up to  $VSWR \leq 6$  wherein an insertion loss between 0.6 dB and 6.1 dB was obtained. The measured IIP3 of the differential and single ended networks were 37.4 dBm and 34.2 dBm respectively.

**Adjustable Radio Frequency Front End Receiver for SDR and CR Applications Employing Noise Cancelling** ..... 830

*Ahmed Hussein Ahmed AbdelRahman, Mohamed El-Nozahi, Hani Fikry Ragai*

Ain Shams University, Egypt

This paper presents a highly linear radio frequency front end (RFFE) receiver (Rx) with its frequency response characterized by having an adjustable shape, center frequency, and bandwidth (BW). The RFFE Rx output is sampled at an adjustable sampling rate to be fed to an ADC for further baseband processing. The architecture employs a generalization of noise cancelling theory to reduce the noise figure (NF) by including an auxiliary path besides its main path to be able to subtract the noise at the output. Simulated on 65 nm technology, this method is proved to reduce the NF from 6.5 dB to 3.5 dB for a selected filter impulse response and down to 2.3 dB in case of implementing a Sinc frequency response.

**Session B3L-E: SPECIAL SESSION: Internet of Things: Sensors to Cyber-Security**

**Chair:** Neeraj Magotra, *Western New England University*

**Time:** Tuesday, August 6, 2019, 13:30 - 15:00

**Location:** Salon G & H

**Considerations when Selecting a Software Development Kit (SDK) for the Creation of Internetconnected Products** ..... N/A

*Adrian Fernandez*

Texas Instruments Inc., United States

This session aims to cover the unique considerations a product developer should think through when selecting a microcontroller platform to develop their products on top of. In particular, the software development kit (SDK) that is offered by silicon vendors should be evaluated closely, as this is the aspect that product developers will be most intimately working with as they bring their products to life. Few considerations come to mind when evaluating an MCU platform SDK: Software portability, stack support and integration, availability of integrated middleware (i.e. graphics, sensor drivers, etc), licensing, documentation, and more. Finding the right combination of the items listed can help developers go to market more quickly with not just a single IoT product, but a portfolio of interconnected products that might span across different technologies (from Wi-Fi to BLE to ZigBee, etc).

**The Last Thing IoT Device Engineers Think About: End of Battery Life Behavior for IoT Devices** ..... 837

*Brad Jolly*

Keysight Technologies, United States

Battery-powered devices eventually consume their battery charge, and the device's behavior as it nears the end of battery life can have surprising and significant consequences for the application success, customer satisfaction, and even patient safety in the context of medical devices. Event-based power analysis at different supply voltages gives design and validation engineers quick, visual insights into device behavior and charge consumption. Engineers can then implement strategies to extend the device's lifetime and measure the effects of those strategies.

**AI, IoT Hardware and Algorithmic Considerations for Hearing Aid and Extreme Edge Applications** ..... 841

*Robert L. Brennan*

ON Semiconductor, Canada

Recently, driven by enhanced computational power and necessity, hearing aid edge applications have arisen to the forefront including voice command, environment sensing and fall detection. This brought up a number of concerns 1) the transmission of possibly private data across an insecure channel, 2) the channel may not exist in remote or adverse transmission environments. 3) The delay from the transmission latency required to obtain cloud computation and 4) Transmission power. It was deemed that the edge processing capabilities must be supported and hardware acceleration of the discussed DNN, GRU and LSTM structures should be pursued. Results are ongoing and will be presented.

**Internet of Things (IoT) and Electrical and Computer Engineering Curriculums** ..... 845

*Neeraj Magotra, Amer Qouneh, John Burke*

Western New England University, United States

Over the last five to ten years, Electrical and Computer Engineering (ECE) programs worldwide have realized the growth of the Internet of Things (IoT) phenomenon. The challenge for ECE departments is to integrate IoT into their curriculums. The general consensus amongst ECE faculty is that our curriculums, particularly for the four year BS programs, are already quite crowded, so how do we introduce yet another major topical area. In our department we have an Electrical Engineering (EE) program and a Computer Engineering (CPE) program. Being cognizant of the fact that in today's world of complex systems all development efforts, by necessity, require a team of players, our department has taken the path of weaving the IoT theme into our existing curriculums. This will ensure that our graduates are cognizant about the IoT and can be part of the IoT design teams in various capacities/roles.

**Study of Convolutional Neural Network for Recognition of Baseband Signals** ..... 848

*Christopher Gravelle, Ruolin Zhou*

University of Massachusetts Dartmouth, United States

We study the behavior of a functional, pre-defined deep learning convolutional neural network (CNN) used to classify baseband signal modulation types adopted from MathWorks. We examine the behavior of the CNN as the architecture is altered, decreasing and increasing the volume of the hidden layers. We test the viability of the pre-constructed CNN as a solution to real-world communications problems by testing the deep learning networks ability to recognize modulation schemes with a signal-to-noise ratio (SNR) significantly lesser than that used to train the network. We investigate the ability of the pre-constructed CNN to be trained with waveforms of a lower SNR in the interest of more accurate modulation recognition overall. We also demonstrate the efficacy of the CNN model using Universal Software Radio Peripheral (USRP) radios. A long-term goal is to develop the optimized CNN on an SoC-FPGA (System-on- Chip Field Programmable Gate Array) to enable autonomous self-learning as well as self-defense of an intelligent radio system.

**Session B3L-F: Trusted Electronics and Security II**

**Chair:** Manuel Jimenez, *Univ. of Puerto Rico*

**Time:** Tuesday, August 6, 2019, 13:30 - 15:00

**Location:** Addison

**(HIADIoT): Hardware Intrinsic Attack Detection in Internet of Things; Leveraging Power Profiling** ..... 852

<sup>1</sup>Hawzhin Mohammed, <sup>1</sup>Tolulope A. Odetola, <sup>1</sup>Syed Rafay Hasan, <sup>2</sup>Sari Stissi, <sup>3</sup>Isaiah Garlin, <sup>4</sup>Falah Awwad

<sup>1</sup>Tennessee Technological University, United States; <sup>2</sup>Earlham College, United States;

<sup>3</sup>Columbia University, United States; <sup>4</sup>United Arab Emirates University, U.A.E.

Internet of Things (IoT) device usage has grown and has been adopted in various daily use devices such as healthcare, smart homes, smart grids, connected cars and the list goes on. IoT devices have security vulnerabilities and cannot completely guarantee data privacy. As is the case with any network, IoT devices are also prone to hacks and Hardware Intrinsic (HI) attacks such as Hardware Trojans (HT), Firmware Modification and Memory Manipulation. The manifestation of HI attack can lead to various types of security issues which includes data theft and denial of service. Traditional HT attack detection techniques are valid for integrated circuit level only, and considered to be very invasive for an IoT device. Therefore, in this paper we propose a non-invasive approach that investigates Hardware Intrinsic Attack Detection in IoT (HIADIoT) devices. This approach detects covert channel and power depletion attacks through the power profile of IoT devices in different modes of operation utilizing machine learning algorithm. The data points are preprocessed and provided to Random Forest Algorithm, which creates a model that correctly classified 95.5% of the data points.

**Long-Term, Time-Synchronized Temperature Monitoring using Self-Powered CMOS Timers** ..... 856

<sup>1</sup>Sri Harsha Kondapalli, <sup>2</sup>Liang Zhou, <sup>1</sup>Kenji Aono, <sup>1</sup>Shantanu Chakrabartty

<sup>1</sup>Washington University in St. Louis, United States; <sup>2</sup>Analog Devices, United States

The proposed method uses a chip-scale self-powered timing device that has been shown to be robust and capable of tracking time for years. The sensitivity to temperature and the ability to synchronize time across multiple devices are leveraged to mathematically model the ambient temperature trends. Measurement results from fabricated chips demonstrate deviation errors under 1 degree C, without the need for an external power source. The chip-scale approach opens the door to sample-scale monitoring with finer granularity than batch-level monitoring.

**Side-Channel Attack Resilient Design of a 10T SRAM Cell in 7nm FinFET Technology** ..... 860

Kangqi Chen, Erdal Oruklu

Illinois Institute of Technology, United States

The non-invasive Side-Channel Attacks (SCA) for integrated circuits have been a concern for many years and Leakage Power Analysis (LPA) is among the leading threats for the IC security. For SRAM blocks, LPA would exploit the correlation between data in memory cell and its corresponding leakage power, and possibly decrypt the secret key inside the memory of crypto-systems. This paper proposes a new SRAM design countering against LPA, based on a recent low-power single-ended 9T cell design. Leakage balance issue for the 9T cell is discussed and a new cell design is presented. Simulation results confirm that the proposed SRAM cell preserves the advantages from the 9T design and have a well-balanced leakage behavior preventing against SCA.

**Complete Security Stack FPGA Implementation of the Software Defined Radio on ZYNQ** ..... 864

<sup>1</sup>Abdelrhman M. Abotaleb, <sup>1</sup>Abdulkareem M. Abotaleb, <sup>1</sup>Amr G. Wassal, <sup>1,2</sup>Hassan Mostafa

<sup>1</sup>Cairo University, Egypt; <sup>2</sup>Zewail City of Science and Technology, Egypt

The increasing deployment of the Internet of Things (IoT) in every life aspects makes the different communications methodologies used in IoT applications are vulnerable to cyber-attacks, either through passive attacks to intercept un-authorized messages between two communications parties or by masquerade active attacks being able to modify or even fabricate new message to communications parties, This work implements the whole Software Defined Radio (SDR) with GSM, UMTS, and Bluetooth communications block then integrating the communications blocks with focus in optimizing the added security layers, including the authentication to overcome masquerading and encryption to overcome passive attacks , for the 2G (Comp128, A3, A5 and A8), 3G and 4G (the KASUMI, F8 and F9) and the Bluetooth (SAFER+,E1, E2 and E3) algorithms on the Field programmable gate array of the ZYNQ System-On-Chip while focusing on minimizing the utilization and power consumption of the security functions part.

**Signal Rate Activity as a Formal Method for Fault Discovery and Monitoring in Trusted and Secure Electronics Development** ..... 868

Richa Verma, Steven B. Bibyk

Ohio State University, United States

Switching Rate Activity SRA is developed as a candidate formal security measure for hardware design. SRA of fault models can be used for detection of faults by comparison to designs without faults. SRA is often calculated using test vectors, which we demonstrated in a trusted electronics paper in mwscas 2016. We improve those methods by developing formal methods for calculating SRA, which increases the verification coverage needed for trusted hardware.

**Session B3L-G: Recent Advances in Digital Arithmetic Devices and Digital Filter Designs**

**Chair:** William Jenkins, *Pennsylvain State University*

**Time:** Tuesday, August 6, 2019, 13:30 - 15:00

**Location:** Salon I & J

**Parallel GF(2<sup>n</sup>) Modular Squarers** ..... 872

Trenton J. Grale, Earl E. Swartzlander Jr.

University of Texas at Austin, United States

Operations over polynomial Galois fields GF(2<sup>n</sup>) are employed in a variety of cryptographic systems, including elliptic curve cryptography (ECC). These operations include multiplication and squaring, and reduction with respect to an irreducible polynomial modulus. Computing the square of a GF(2<sup>n</sup>) polynomial is trivial, and modular reduction can be performed faster and with less hardware complexity compared to the general multiplication case. A fully parallel polynomial n-bit squarer is presented with O(log2n) latency, and is compared to a polynomial multiplier of similar design.



**Near-Linear-Phase IIR Filters using Gauss-Newton Optimization** ..... 876

*Jasper Tan, C. Sydney Burrus*  
Rice University, United States

In this paper, we present a simple optimization-based method for designing near-linear-phase IIR filters based on the Gauss-Newton method, and we explore its benefits over symmetric FIR filters. We demonstrate IIR low-pass filters, with lower group delay, lower order, and lower magnitude errors than corresponding FIR filters while still maintaining a phase response linearity of  $R2 > 0.99$  in the passband. Such filters can be beneficial in applications where approximate, rather than exact, linear phase is sufficient

**Facial Recognition System Employing Transform Implementations of Sparse Representation Method** ..... 880

*Taif Alobaidi, Wasfy B. Mikhael*  
University of Central Florida, United States

A new discriminative sparse representation approach for robust face recognition via l2 regularization (SRFR) was recently published. Here, a FR system implementation employing coefficients from two non-orthogonal transform domains, namely, Two-Dimensional Discrete Wavelet Transform (2D DWT) and 2D Discrete Cosine Transform (2D DCT), is presented. The use of these coefficients in this Mixed Wavelet Cosine Sparse Representation for Face Recognition (MWCSRFR) system as features shown to appreciably lower the computational complexity and the final storage size while maintaining the high recognition rate of the SRFR. Extensive simulations were carried out on five face databases, namely, ORL, YALE, FERET, Cropped AR, and Georgia Tech. The improved properties of the MWCSRFR are proved as shown in the given sample results.

**An Artificial Intelligent Flexible Gas Sensor based on Ultra-Large Area MoSe<sub>2</sub> Nanosheet** ..... 884

*Shiqi Guo, Dong Yang, Baichen Li, Quan Dong, Zhenyu Li, Mona E. Zaghoul*  
George Washington University, United States

In this work, we successfully transferred ultra-large area of MoSe<sub>2</sub> atomic layer flakes on Kapton film with gold-mediated exfoliation method. The large area MoSe<sub>2</sub> nanosheet works as active chemical gas sensing channel for the flexible functional devices. The two terminal flexible gas sensor exhibited high responsivity under low concentration for NH<sub>3</sub> and NO<sub>2</sub>. The flexible electronics were bended and further tested with external circuit. In addition, an artificial intelligent data processing method with machine learning is applied to localize the toxic gas source. These results suggested that wearable large area MoSe<sub>2</sub> atomic layer is promising for wearable environmental detection applications.

**Performance Evaluations of Bio-Inspired Adaptive Algorithms Applied to IIR Digital Filters Designed with Coupled Form Second Order Sections** ..... 888

*<sup>1</sup>M. Hussain, <sup>1</sup>W.K. Jenkins, <sup>2</sup>C. Radhakrishnan*  
<sup>1</sup>Pennsylvania State University, United States; <sup>2</sup>University of Illinois at Champaign-Urbana, United States

During many past decades it has been known that when using finite word-length binary arithmetic in IIR digital filters coupled form second order sections implement conjugate-pair poles that have relatively uniform pole locations located inside the unit circle in the z-plane. However, coupled form 2nd order sections could never be used in IIR adaptive filter designs using steepest descent adaptive algorithms due to the multi-modal error surfaces created by coupled form structures. Results presented in this paper demonstrate that the LFFA can be effectively applied to IIR adaptive filter structures designed with parallel or cascade second order coupled form sections.

**Session B4L-A: Design Techniques for TDCs, ADCs and DACs**

**Chair:** Sebastian Hoyos, *Texas A&M University*

**Time:** Tuesday, August 6, 2019, 15:30 - 17:00

**Location:** Bent Tree I & II

**Digitally Interpolated Pre-Skewed Delay-Line Digital-to-Time Converter with Minimum Nonlinearity and Latency** ..... 892

*Daniel Junehee Lee, Fei Yuan, Gul Khan*  
Ryerson University, Canada

This paper presents the design of an 8B digital-to-time converter (DTC) using a pre-skewed delay line and digital time interpolation. The impact of pre-skewing signals on the per-stage-delay, linearity, and power consumption of pre-skewed delay lines is investigated. The linearity of the digital interpolator is explored. The impact of the slope of the inputs of the interpolator on the delay and linearity of the interpolator is analyzed and the maximum slope of the inputs of the interpolator that yields the minimum latency without sacrificing linearity is obtained. The DTC is designed in a TSMC 65 nm 1.0 V CMOS technology and analyzed using Spectre with BSIM4.4 device models. Simulation results show the DNL and INL of the time interpolator are less than 0.1 LSB and 0.18 LSB, respectively. The DNL and INL of the DTC are less than 0.16 LSB and 0.48 LSB, respectively.

**ADC Quantization with Overlapping Metastability Zones and Dual Reference Calibration** ..... 896

*Jiajun Ren, Jiu Xiong, Jin Liu*

University of Texas at Dallas, United States

This paper presents a new ADC quantization method using overlapping metastability zones with dual reference metastability zone detectors. Dual reference calibration is proposed to define both the upper bound and the lower bound of each metastability zone. Therefore, the metastability zones are defined with higher precision, and the ADC can resolve finer input voltage differences for a smaller input LSB voltage.

**Selecting the Fastest Settling-Time Filter in PDM-Based DACs used for Dynamic Calibration Applications** ..... 900

<sup>1</sup>Ahmed Emara, <sup>1</sup>Gordon W. Roberts, <sup>2</sup>Sadok Aouini, <sup>2</sup>Mahdi Parvizi, <sup>2</sup>Naim Ben-Hamida

<sup>1</sup>McGill University, Canada; <sup>2</sup>Ciena Corporation, Canada

A study was performed to select the filter type and order that yields the lowest settling time with an area and power efficient design, for calibration DACs. It was shown that the use of a 3rd order Bessel or Gaussian filter produces a system that settles faster than the ones using Butterworth. Then a 3rd order Bessel LPF was realized in the implementation of a 10-bit DAC as a design example. This design provided 25% lower settling time compared to other architectures, with comparable power consumption and area occupancy. Similar results were also obtained for 8-12 bits of resolution.

**Novel Control Unit Design for a High-Speed SHA-3 Architecture** ..... 904

*Pranav Gangwar, Neeta Pandey, Rajeshwari Pandey*

Delhi Technological University, India

This paper presents a control unit design for improving the throughput of SHA3-256 architecture. The Iterative data path design is employed to process multi-block messages, which makes the design functional for any input size. A higher throughput is achieved by reducing the number of control signals in the critical path, and optimizing the counter which generates the memory address and affects the maximum operating frequency. The synchronization problems caused by this approach between the generated Hash and its corresponding Valid signal, are overcome by the Synchronizer. The proposal exhibits 920 Mbps higher throughput, i.e. a 7% improvement over state of the art.

**Machine Learning based Image Calibration for a Twofold Time-Interleaved High Speed DAC** ..... 908

<sup>1,2</sup>Daniel Beauchamp, <sup>2</sup>Keith M. Chugg

<sup>1</sup>Jariet Technologies, United States; <sup>2</sup>University of Southern California, United States

In this paper, we propose a novel image calibration algorithm for a twofold time-interleaved DAC (TIDAC). The algorithm is based on simulated annealing, which is often used in the field of machine learning to solve derivative-free optimization (DFO) problems. The digital-to-analog converter (DAC) under consideration is part of a digital transceiver core that contains a high speed analog-to-digital converter (ADC), microcontroller, and digital control via a Serial Peripheral Interface (SPI). These are used as tools for designing an algorithm which suppresses the interleave image to the noise floor. The algorithm is supported with experimental results in silicon on a 10-bit twofold TIDAC operating at a sample rate of 50 GS/s in 14nm CMOS technology.

**Session B4L-B: Amplifiers II**

**Chair:** Aydin Karsilayan, *Texas A&M University*

**Time:** Tuesday, August 6, 2019, 15:30 - 17:00

**Location:** Preston Trail I & II

**Passive Slew Rate Enhancement Technique for Switched-Capacitor Circuits** ..... 913

*Manjunath Kareppagoudr, Emanuel Caceres, Yu-Wen Kuo, Jyotindra Shakya, Yanchao Wang, Gabor C. Temes*

Oregon State University, United States

A passive charge compensation technique is proposed for switched capacitor circuits which increases the slew rate of its amplifiers. Higher linearity can be achieved by adding a small amount of circuitry with low power consumption. The proposed technique is implemented in a single-bit discrete time second-order delta-sigma modulator in 65-nm CMOS technology, where simulation results show an improvement of 12 dB SNDR. Alternatively, the same performance can be achieved with almost half of the power consumption with charge compensation circuit activated.

**MOS-Only Current-Mode Analog Signal Processing Functional Cores** ..... 917

<sup>1</sup>Ali Ibrahim Ozkan, <sup>1</sup>Bilgin Metin, <sup>2</sup>Norbert Herencsar, <sup>1</sup>Oguzhan Cicekoglu

<sup>1</sup>Bogazici University, Turkey; <sup>2</sup>Brno University of Technology, Czech Rep.

MOS-only type signal processing devices received significant attention mainly due to trends in analog design works toward low-voltage low-power designs. Using this approach many limitations of analog filters especially frequency limitation among others is less pronounced compared to classical approach employing Op-Amps, Operational Transconductance Amplifiers, Current Conveyors, or similar active elements. In this work we present three MOS-only type current-mode analog functional filter cores. For illustration purpose, an application filter design example is given that is a novel filter topology and compared with its counterparts previously published in the literature.

**Design of a 52.5 dB Neural Amplifier with Noise-Power Trade-Off** ..... 921

Nishat T. Tasneem, Ifana Mahbub

University of North Texas, United States

A neural signal recording amplifier is designed using two-stage topology and a capacitive-resistive feedback network. It achieves the mid-band gain of >52 dB with a total power consumption of <4  $\mu$ W. The amplifier is designed taking into account the noise-power trade-off and the input-referred noise is found to be 3.16  $\mu$ Vrms. The amplifier shows a good performance over the bandwidth of 0.125-1 kHz to record the low-frequency neural signals.

**A 1.1V 1.3GHz 4th Order Filter with Feedforward Miller Compensation OPAMP for 5G Applications** ..... 925

<sup>1</sup>Vikas Aggarwal, <sup>1</sup>Ritabrata Bhattacharya, <sup>1</sup>Ashish Gupta, <sup>1</sup>Taranjit Kukal, <sup>2</sup>Sankaran Aniruddhan

<sup>1</sup>Cadence Design Systems, India; <sup>2</sup>Indian Institute of Technology Madras, India

A 1.3 GHz bandwidth 4th order analog filter in a 45nm bulk CMOS process is reported in this work. The filter is a cascade of two Rauch bi-quads. The operational amplifiers for these biquad cells are based on an unique combination of both feedforward and miller compensation to achieve a high unity gain bandwidth of 4.5GHz, a high dc gain of 45dB and a good phase margin of 75 degrees. Post-layout simulations of the filter shows a 3dB cut off frequency of 1.3GHz with an IIP3 of + 12dBm and a total in band integrated noise voltage of 660 $\mu$ VRMS. The total dc power consumption of this filter is 24 mW at a 1.1V power supply.

**Session B4L-C: SPECIAL SESSION: Advanced Power Management ICs: Design, Analysis and Methodology**

**Chair:** Punith Surkanti, *Maxim Integrated*

**Co-Chair:** Paul Furth, *New Mexico State University*

**Time:** Tuesday, August 6, 2019, 15:30 - 17:00

**Location:** Mesquite I

**Imbalanced High-Current Multi-Phase Buck Converters for High-Performance CPUs** ..... 929

<sup>1,2</sup>Manmeet Singh, <sup>1</sup>Ayman Fayed

<sup>1</sup>Ohio State University, United States; <sup>2</sup>Dialog Semiconductor Inc., United States

High-performance CPUs require buck converters with high-current ratings (4-12 A), fast dynamic response, and high efficiency across a wide load range. The most common approach for realizing such buck converters is the conventional multi-phase topology with phase-shedding, where all the active phases are identical in terms of the inductor, the switching frequency, and the share of the total load current, i.e. balanced phases. Instead, this paper proposes using a different inductor, switching frequency, and share of the total load current for each individual phase, i.e. imbalanced phases. This approach provides additional degrees of freedom by the independent choice of the inductor and the switching frequency of each phase, which enables higher maximum load current rating and higher efficiency across the entire load current range compared to conventional balanced multi-phase designs. To demonstrate the viability and the advantages of imbalanced multi-phase buck converters in high-current application, a 12-A 4-phase design in 0.13- $\mu$ m CMOS for high-performance CPUs is presented and compared to three conventional balanced reference designs in the same process technology.

**Ratio Extension Technique for Ladder- / Dickson-Based Multiple-Output Switched-Capacitor DC-DC Converters** ..... 933

<sup>1,2</sup>Zhe Hua, <sup>1</sup>Hoi Lee

<sup>1</sup>University of Texas at Dallas, United States; <sup>2</sup>Apple Inc., United States

This paper presents a conversion ratio extension technique for both step-up and step-down Ladder- / Dickson-based multiple-output switched-capacitor (MOSC) DC-DC converters. The proposed ratio-extension cells double / quadruple the number of conversion ratios of all outputs in a MOSC DC-DC converter, and thus significantly improve power efficiency and line regulation performance over a wide input voltage range in Lithium-Ion battery-input applications. A Dickson-based triple-output step-down switched-capacitor (TOSC) DC-DC converter with the proposed ratio-quadrupler cell (RQC) is designed and simulated in a 130nm CMOS process. The proposed converter can simultaneously provide three regulated outputs of 0.8V, 1.6V and 2.5V. With 8 conversion ratios per output, the converter power efficiency over the input voltage range of 2.7 – 4.5V is improved by a maximum of 17.5% compared to the 2-ratio traditional counterpart.

**A Low Output Voltage Ripple Fully-Integrated Switched-Capacitor DC-DC Converter** ..... 937

*Anurag Veerabathini, Paul M. Furth*

New Mexico State University, United States

A fully-integrated switched-capacitor (SC) DC-DC converter that steps down 3.3V to 1.5V with a peak efficiency of 68% is implemented in a 2P3M 0.6- $\mu\text{m}$  CMOS process with a 555pF poly-poly flying capacitor and a 1.34nF MOS tank capacitor. This paper demonstrates a means of applying a low-frequency input clock as part of a time-interleaving technique for a symmetric charge-discharge topology that reduces the output voltage ripple. Burst-mode pulse-frequency modulation is used to maintain high efficiency over a wide range of load currents. A maximum 27mV in output voltage ripple is measured for load current between 590 $\mu\text{A}$  and 8mA. In response to a load transient from 560 $\mu\text{A}$  to 5.1mA, the SC converter shows no undershoot and an overshoot of only 19mV. Measured load regulation is 13.2mV/mA.

**Multi-Channel LED Driver with Accurate Current Matching for Portable Applications** ..... 941

*Punith R. Surkanti, Disha Mehrotra, Paul M. Furth*

New Mexico State University, United States

LED drivers are required to regulate the current through the LEDs by providing sufficient forward voltage. Multiple LEDs can be driven by single LED driver as a single series string or parallel strings. In this paper, we propose a multi-string LED driver based on current-limiting hysteretic boost converter, which is capable of driving ten LEDs in five parallel strings. An accurate current matching circuit with low voltage headroom requirement is implemented to match the LED currents in all strings. A PFM dimming block is designed to operate with a 200 kHz clock and has 11 programmable dimming ratios ranging from 2:1 to 2048:1. This LED driver is implemented in 0.5- $\mu\text{m}$  CMOS process and operates with a Li-ion battery with a voltage range 3 – 4.2 V. This LED driver is suitable for backlight LED displays in mobile devices.

**A 10-MHz Current-Mode Fixed-Frequency Hysteretic Controlled DC-DC Converter with Fast Transient Response** ..... 945

*Siddharth Agarwal, Ashis Maity*

Indian Institute of Technology Kharagpur, India

This paper proposes a fixed-frequency current-mode hysteretic controlled DC-DC buck converter operating at 10 MHz. The proposed converter senses the inductor current through a current-sensing filter and compares the sense node voltage with only one threshold of the hysteretic comparator. The reference clock synchronizes the switching frequency of the converter by forcedly altering the present state of the hysteretic comparator. The simulation results show that for a reference clock frequency of 10 MHz, inductor and output capacitor value of 200 nH and 4.7  $\mu\text{F}$  respectively, and a load step from 50 mA to 450 mA in 1 ns, the maximum overshoot and the settling time are below 12 mV and 1.9  $\mu\text{s}$  respectively. The output voltage load regulation is 2.5 mV/A.

## **Session B4L-D: Communication Circuits III**

**Chair:** Yushi Zhou, *Lakehead University*

**Time:** Tuesday, August 6, 2019, 15:30 - 17:00

**Location:** Quorum I & II

**Optimized Microwave Multiport Beam-Forming Circuit Design for Wideband Applications** ..... 949

<sup>1</sup>*Hung Tran, G.R. Branner, B. Preetham Kumar*

<sup>1</sup>University of California, Davis, United States; <sup>2</sup>California State University, Sacramento, United States

This paper presents a practical modeling methodology for wide-band microwave applications on curved surfaces that focuses on the design of the beam-forming network playing a role similar to that of multiport power combiners/splitters. The beam-forming network was developed to provide equal electrical paths from the radiators to the common power receiver. While multiport Wilkinson-like power combiner design methodology are not available for those applications, phase shifting technique and symmetric power splitting devices are utilized to achieve flatter response compared to conventional techniques.

**An Adaptive Control Approach to Securely Transmit Colored Images using Chaos-Based Cryptography** ..... 953

*Ashraf A. Zaher, Jibran Yousafzai*

American University of Kuwait, Kuwait

Colored images are converted into three parallel time series that correspond to the basic RGB color components. The time series modulate the parameter of the chaotic transmitter, using a simple digital encryption function. Synchronization between the transmitter and the receiver is achieved, using an adaptive control approach. A single time series of the transmitter is transmitted in the public communication channel to promote security, while eight different chaotic attractors are generated to have a superior performance. Tuning the parameter update law that guarantees both stability and satisfactory transient performance is investigated to highlight advantages and limitations of the proposed strategy.

**An Optimized Check-Node Architecture for 5G New Radio LDPC Decoders** ..... N/A

<sup>1</sup>Fakhreddine Ghaffari, <sup>1,2</sup>Khoa Le, <sup>1</sup>Duc-Phuc Nguyen, <sup>1</sup>David Declercq

<sup>1</sup>Université Paris Seine, Université de Cergy-Pontoise, ENSEA, CNRS, France;

<sup>2</sup>Hochiminh City University of Technology, Vietnam

This paper presents an efficient hardware architecture of the Check Node (CN) units for the fifth generation (5G) new-radio Low-Density Parity-Check (LDPC) decoders. The proposed CN architecture is designed by splitting the high-degree CN operations into several phases and simplifying computing circuitry and connection wires. The critical path is shortened while the latency increment for one decoding iteration is negligible. Also, the proposed architecture allows to apply adaptively different offset factors when decoding different CN degree. This technique enhances the error rate and performance of our quantized LDPC decoder. The ASIC synthesis results confirm the advantages of the proposed architecture.

**Design of Two-Band Multiplier-Free QMF Filter Banks** ..... N/A

<sup>1</sup>L.M. Barba-Maza, <sup>1</sup>G. Jovanovic Dolecek, <sup>2</sup>Alfonso Fernández-Vázquez

<sup>1</sup>INAOE, Mexico; <sup>2</sup>Instituto Politécnico Nacional, Mexico

This work presents novel design of a multiplier free Quadrature Mirror Filter (QMF) bank with perfect reconstruction (PR) characteristic with the goal to reduce the computational cost and time. Two methods are elaborated for the filter bank (FB) design: One method uses the Remez algorithm to get equiripple filters, while the other one uses the minimizing the energy in the filter stopband. The FB designs are presented in their lattice form. Finally on the base of lattice coefficients, the minimum energy method is chosen to create the final FB. The proposed method is compared with the similar approaches from literature, using Matlab simulations

**35  $\mu$ W Linearized LNA for WSN Applications** ..... 965

Jared Mercier, Yushi Zhou

Lakehead University, Canada

In this work, a linearized ultra-low-power (ULP) low noise amplifier (LNA) designed in GF 130 nm CMOS technology is presented for wireless sensor network (WSN) applications. The LNA targets the 915MHz ISM band to meet the stringent power requirements of the wireless sensor node. Furthermore, to enhance the linearity, the design employs complementary derivative superposition (DS) to a common-source (CS) topology. The NFET is optimally biased for voltage gain, power, and bandwidth efficiency. The PFET load is sized accordingly for nonlinear compensation. The simulated voltage gain, IIP3, input compression point, and NF are 15.7 dB, -6.5 dBm, -17.5 dBm and 5.7 dB respectively. The total power consumption is 35 uW from a 0.7 V supply voltage. The evaluated performance of the design using a classical figure of merit (FOM), achieves the highest known value by a significant margin.

**Session B4L-E: SPECIAL SESSION: RFID-Based Sensors for the Internet of Things**

**Chair:** Juan Montiel-Nelson, *University of Las Palmas de Gran Canaria*

**Time:** Tuesday, August 6, 2019, 15:30 - 17:00

**Location:** Salon G & H

**UHF RFID Localization based on a Frequency-Stepped Continuous-Wave Approach** ..... 969

<sup>1</sup>Martin Scherhäufl, <sup>1</sup>Markus Pichler-Scheder, <sup>1</sup>Christian Kastl, <sup>2</sup>Andreas Stelzer

<sup>1</sup>Linz Center of Mechatronics GmbH, Austria; <sup>2</sup>Johannes Kepler University Linz, Austria

This paper introduces a 2-D position measurement system for passive UHF RFID tags based on a frequency-stepped continuous-wave approach. The main application is the localization of objects tagged with RFID transponders. Using this method, no system calibration is required, and phase-ambiguity can be avoided by evaluating the backscattered transponder signals using multiple transmit frequencies of the interrogator signal. To prove the localization method, a local position measurement system demonstrator was used comprising conventional passive EPCglobal Class-1 Gen-2 UHF RFID tags, a commercial off-the-shelf RFID reader, eight transceiver frontends, baseband hardware, and signal processing. Measurements were carried out in an indoor office environment where a measurement zone of 5.0 m x 3.5 m was surrounded by drywalls, concrete floor and ceiling. The experimental results showed accurate localization with a root-mean-square error of 22.2 cm and a median absolute error of 17.0 cm.

**A High Accuracy 3.1V Voltage Limiter for Enabling High Performance RFID Sensor Applications** ..... 973

<sup>1</sup>Andoni Beriain, <sup>1</sup>Ainhua Rezola, <sup>2</sup>David Del Rio, <sup>1</sup>Hector Solar, <sup>2</sup>Iñaki Gurutzeaga, <sup>1</sup>Roc Berenguer

<sup>1</sup>University of Navarra, Spain; <sup>2</sup>CEIT, Spain

This paper presents a low power voltage limiter design that avoids possible damages in the analog front-end of a RFID sensor due to voltage surges whenever the tag gets close to the reader. The proposed voltage limiter design takes advantage of the implemented bandgap reference block in order to provide a highly accurate limiting voltage in spite of temperature variation and process dispersion. The measured limiting voltage is 3.1V while showing a low current consumption of 100nA when the reader and the tag are far away, so that the sensitivity of the tag is not impacted due to an undesired consumption in the voltage limiter. The circuit is implemented in a low cost 180nm CMOS technology.

**Design of a Wireless Sensor Network for Oceanic Floating Cages in Aquaculture** ..... 977

*Judith Santana Abril, Graciela Santana Sosa, Javier Sosa*

University of Las Palmas de Gran Canaria, Spain

This paper presents the design of a wireless sensor network for oceanic floating cages in aquaculture. The deployment of the sensor network over current aquaculture installations is discussed. The software and hardware of a sensor node are outlined. A wireless information and power transfer interface, based on the ISO 11784/11785 HDX standard, for underwater sensor nodes are studied. The misalignment problem in the wireless interface antennas is evaluated in depth. In addition, it is determined the maximum allowed misalignment to keep the information and power transfer efficiency over 70%. Moreover, we establish a linear function to model the charging rate with a maximum error of a 2.2%. Finally, all data presented in this paper is based on real measurements over the sensor node prototypes implemented with commercial devices.

**Session B4L-F: System Architectures I**

**Chair:** Yong-Bin Kim, *Northeastern University*

**Time:** Tuesday, August 6, 2019, 15:30 - 17:00

**Location:** Addison

**Effectively Partitioned Implementation for Successive-Cancellation Polar Decoder** ..... 981

<sup>1</sup>*Yuta Ideguchi, <sup>1</sup>Norifumi Kamiya, <sup>2</sup>Masashi Tawada, <sup>2</sup>Nozomu Togawa*

<sup>1</sup>NEC Corporation, Japan; <sup>2</sup>Waseda University, Japan

This paper studies the FPGA implementation of a successive-cancellation (SC) decoder for polar codes which have recently attracted attention as error-correcting codes adopted for 5G wireless systems. We focus on effective ways of partitioning the SC decoding procedure into combinatorial and sequential logic parts. We demonstrate an FPGA implementation of the decoder architecture for a 1024-bit length polar code and show that our FPGA decoder can achieve three times higher throughput than the conventional sequential semi-parallel decoder without significantly increasing the hardware resources.

**A New Hardware Accelerator for Data Sorting in Area and Energy Constrained Architectures** ..... 985

<sup>1</sup>*Amin Norollah, <sup>1</sup>Hakem Beitollahi, <sup>2</sup>Ahmad Patooghy*

<sup>1</sup>Iran University of Science and Technology, Iran; <sup>2</sup>University of Central Arkansas, United States

Sorting is one of the most important computational tasks in data processing applications. Recent studies show that the FPGA-based hardware accelerators are more efficient than the general-purpose processors and GPUs. By increasing the input records in the sorting network, the number of Compare- And-Swap (CAS) units would be increased, which in turn, will lead to increased resource consumption. In some applications, the number of available resources is limited. Thereby, it is necessary to optimize resource requirements while maintaining a sufficient level of performance. This paper presents a new sorting architecture that reduces the number of required resources compared to the state-of-the-art sorting architecture and achieves the desired performance using Unary processing. Results indicate that the proposed architecture increases throughput by 29.1% and reduces the number of LUTs by 42%, for sorting 8-input records, compared to other architecture.

**Reconfigurable Threshold Logic Networks in FPGA for Moving Object Detection** ..... 989

<sup>1</sup>*Alex Pappachen James, <sup>1</sup>Kizheppatt Vipin, <sup>2</sup>Bhaskar Choubey*

<sup>1</sup>Nazarbayev University, Kazakhstan; <sup>2</sup>Siegen University, Germany

Threshold logic inspires from the principle of the firing of neurons mimicking synaptic connections of a binary neural network to create generalized logical functions for solving complex cognitive tasks such as object detection. We propose an implementation of modular and hierarchical threshold logic network in FPGA that aims to provide a low complexity near sensor co-processing hardware solution for object detection in digital cameras. The proposed network has been designed and implemented on a Xilinx Zynq SoC. The solution is robust in terms of object detection even in the presence of high levels of occlusion, noise and illumination changes. The total power consumption of the design is estimated to be 8.6 W. Performance analysis of the detector IP core is thoroughly simulated on test databases for computer vision with real-world images. The object detection module ensures a high performance rate of about 5000 frames per second at 100 MHz clock frequency while processing 100 × 100 pixel images.

**Implementation of a Real-Time Distance Evaluation Algorithm for Wireless Localization Systems** ..... 993

<sup>1</sup>*G. Piccinni, <sup>1</sup>G. Avitabile, <sup>1</sup>G. Coviello, <sup>2</sup>C. Talarico*

<sup>1</sup>Polytechnic University of Bari, Italy; <sup>2</sup>Gonzaga University, United States

The paper describes the FPGA implementation of a novel TDOA distance evaluation algorithm that combine the characteristics of an OFDM symbol with the properties of the Zadoff-Chu mathematical sequences. The distance evaluation system has been validated in presence of severe multipath interference and allows to achieve an accuracy that is always within 1.2cm of the target position. The algorithm is implemented using the FPGA (Cyclone IV-E EP4CE115F29C8L Cyclone IVE) available on the Altera's DE2-115 development board. The implementation requires about 120k bit of memory and less than 40k logic elements (of which about 30k are registers).

**Efficient Hardware Architecture for Overlap-Add Method of Short-Time Fourier Analysis/Synthesis** ..... N/A

*Mohammed Bahoura*

University of Quebec at Rimouski, Canada

This paper presents an efficient hardware architecture of the overlap/windowing and overlap-add techniques for real-time FFT/IFFT-based signal processing algorithms. Short-time overlapped frames are extracted and windowed before applying short-time Fourier analysis/synthesis. The original signal is perfectly reconstructed from the windowed (modified) frames using the overlap-add (AOL) technique. This architecture has been implemented on Field Programmable Gate Array (FPGA) using a high-level programming tool.

**Session B4L-G: Control Systems, Mechatronics, and Robotics I**

**Chair:** Ying-Khai Teh, *San Diego State University*

**Time:** Tuesday, August 6, 2019, 15:30 - 17:00

**Location:** Salon I & J

**Magnetic Angular Position Sensing with High Stray Field Immunity for Mechatronic Applications** ..... 1001

*Marcus Prochaska, Kris Rohrmann, Marvin Sandner, Phil Meier*

Ostfalia University of Applied Sciences, Germany

Magnetic field sensors are of prime importance for robotics, industrial and automotive applications. Due to the digital transformation there is a increasing density of electronic systems in mechatronics. Thus, the number of stray field sources is rising. In this paper a novel approach for the suppression of disturbing magnetic fields is presented. Instead of a single angle sensor the proposed methodology uses an array consisting of 2D magnetometers. An efficient sensor signal processing, which is based on 2D DFT, calculates the angular position and eliminates angle errors. Simulations were conducted in order to validate the presented methodology.

**A Numerical Methodology for a 6 DOF Pose Estimation with 3D Magnetic Field Sensors** ..... 1005

*Phil Meier, Kris Rohrmann, Marvin Sandner, Marcus Prochaska*

Ostfalia University of Applied Sciences, Germany

Linear and angular position sensing using magnetic field sensors play a decisive role in automotive, industrial and consumer applications. Recently powerful 3D Hall sensors have become available, which enables simple measurement setups for 3D position sensing. In this paper a numerical concept for the determination of linear and angular position in the three-dimensional space is presented, which bases on an analytic model of an encoder magnet. To prevent numerical instabilities, a modified Newton-Raphson algorithm with adaptive dynamic step size control is used. Simulation results validate the applicability of our approach.

**Predictive Control of a Robot Manipulator with Deep Reinforcement Learning** ..... N/A

*Eduardo Bejar*

Pontificia Universidad Catolica del Peru, Peru

This paper tackles the problem of trajectory following of a two-link rigid robot manipulator. The proposed controller bases its operation on the idea behind preview control in which the control law is divided in two parts: a feedback component that depends only on the present state of the system, and a predictive component that only uses future values of the reference trajectory. In this sense, the designed controller uses for training and control both present and future states of the system. Simulation results when following a test trajectory are presented to validate the proposed method and to show that the proposed controller exhibits better performance with respect to a neurocontroller that does not use a predictive component neither for training nor control.

**Power Quality Evaluation and Optimization of Sensor-Less Field Oriented Controller on 32-Bit ARM Cortex Microcontroller** ..... 1013

*Xin Xue, Ying-Khai Teh*

San Diego State University, United States

Electronic speed controller (ESC) is an important subsystem in drones, which are used to control and regulate the speed of its electric motor. For the high-end drones which require longer flight times, higher dynamic behavior with smooth and stable performance, Field Oriented Controllers (FOC) which power three-phase sinusoidal back-EMF motors are typically used to provide the required high efficiency, small torque ripple and dynamic performance. This paper proposes an analysis method based on discrete Fourier transform (DFT) over the measured motor current, in order to optimize the system parameters such as modulation period, CPU clock frequency and power supply voltage. As proof of concept, a FOC-based ESC implemented in a generic 32-bit microcontroller is studied. Findings show that the power quality and motor dynamic performance of a FOC ESC depends strongly on modulation period and relatively insensitive with respect to CPU voltage and frequency scaling.

Wednesday, August 7, 2019

**Session C1L-A: Circuits for RF Communication**

**Chair:** Sebastian Hoyos, *Texas A&M University*

**Time:** Wednesday, August 7, 2019, 8:00 - 9:30

**Location:** Bent Tree I & II

**A 2.6 MHz Bandwidth, 3rd/5th Order Active-RC Polyphase Filter with Quadrature Offset**

**Cancellation for Low-IF GPS Radio** ..... 1017

*Siamak Delshadpour*

NXP Semiconductors, United States

In this paper a low power active-RC filter exhibiting a reconfigurable transfer function, 3rd/5th order Butterworth, integrated in a low IF GPS receiver and fabricated in 0.35um SiGe BiCMOS technology is presented. This 17/26 dB gain filter has a bandwidth of 2.6MHz which is centered at 4.1MHz. It drains 1/1.25mA from a 2.7V supply in 3rd/5th order modes. The average in-band image rejection of this 0.58 mm<sup>2</sup> filter is better than 25dB. This trimmed filter employs a quadrature offset cancellation circuit to remove all the available offset coming from the mixer output and its own mismatches.

**On Design of 60 GHz Solid-State Transformers Modeled as Coupled Bitter Coils** ..... 1021

*I.M. Filanovsky*

University of Alberta, Canada

The paper describes design of solid-state transformers operating at the frequency around 60 GHz. These transformers are approximated as two flat coils located in parallel planes (Bitter coils). A well-known formula for the mutual inductance between two loops located in parallel planes (Maxwell coils) is used to derive the approximate value of mutual inductance of two such coils. The result is improved using three correction factors. The first factor considers the increase of inductance when the round loop is substituted by an octagon. The second factor considers the reduction of inductance when the ideal wire is substituted by a strip. The third factor considers the skin-effect and proposes increasing the effective distance between the coils. The calculation of the primary (or secondary) self-inductance is based on the well known formula of ideal loop inductance, and this result is improved by the first and second correction factors. Two transformers are designed as examples: a planar transformer using the top metal for both primary and secondary, and a stacked transformer with primary in the top metal and secondary in the second from the top metal.

**A Quenching Waveform with an Optimal Crossing Point Calibration for**

**Sensitivity Optimization of SR Receivers** ..... 1025

*Ximing Fu, Kamal El-Sankary*

Dalhousie University, Canada

This paper presents a new quenching waveform generation and calibration for sensitivity optimization of super-regenerative (SR) receivers. To achieve high sensitivity, calibration of the slope and step variations of the optimal quenching waveform (OQW) is needed. The proposed sensitivity optimization uses an optimal crossing point waveform calibration technique to achieve maximum sensitivity during the sensitivity accumulation (SA) region. The proposed OQW circuit and its calibration loops are implemented in 180nm CMOS technology and tested within an SR receiver with a center frequency of 2.4GHz.

**A High Speed, High Conversion Gain RF Envelope Detector for SRO-Receivers** ..... 1029

<sup>1</sup>*Ximing Fu, <sup>1</sup>Kamal El-Sankary, <sup>2</sup>Jianjun Zhou*

<sup>1</sup>Dalhousie University, Canada; <sup>2</sup>Shanghai Jiao Tong University, China

A high speed and high conversion gain envelope detector (ED) is designed for RF super-regenerative-oscillator (SRO) receivers. To reduce glitches from RC filtering used for common mode signal rejection, the proposed ED is implemented using a band-pass buffer as a first stage. To avoid introducing excessive time delay and maintain good performance under high data rate, the proposed design introduces back-to-back inverters operating in linear mode to enhance the conversion gain while reducing the settling time. Simulation results using 0.18um CMOS technology shows that the proposed ED achieves a high data rate of 6.66Mbps while consuming 8.45uW.



## Session C1L-B: Oscillators

**Chair:** Qiyuan Liu, *Qualcomm*

**Time:** Wednesday, August 7, 2019, 8:00 - 9:30

**Location:** Preston Trail I & II

### **Analysis of Linearity in FD-SOI Body-Input Voltage Controlled Ring Oscillators – Application to ADCs** ..... 1033

*Javad Ahmadi-Farsani, José M. de la Rosa*

Instituto de Microelectrónica de Sevilla IMSE-CNM, Spain

This paper studies the use of the body terminal as control voltage of ring oscillators implemented in Fully Depleted Silicon on Insulator (FD-SOI) CMOS. This technology allows to increase the body factor with respect to conventional (bulk) processes, thus allowing a wider tuning range of the threshold voltage. This effect is exploited in this work to improve the linearity of Voltage-Controlled Ring Oscillators (VCROs) to be used as building blocks of Analog-to-Digital Converters (ADCs). An intuitive analysis of basic VCRO current-starved inverter cells is carried out in order to derive an approximate expression of the voltage-to-frequency characteristic. Electrical simulations in a 28-nm node are shown to get insight about the influence of main design parameters and applied to the design of VCRO-based Sigma-Delta (SD) ADCs up to the layout level, whose performance metrics demonstrate the benefits of the presented approach

### **A 1.52-GHz Super-Harmonic Injection-Locked Ring Oscillator in 130nm CMOS** ..... 1037

*Eman Salah El-Din Fahmy, Sameh Assem Ibrahim, Ismail Mohamed Hafez*

Ain Shams University, Egypt

In this paper, a super-harmonic injection-locked ring oscillator (ILRO) is proposed. The proposed ILRO has been designed and simulated using a 130-nm CMOS technology. The circuit is injected with a 7.6-GHz clock signal and generates 10 output clocks of 1.52 GHz each. The proposed design occupies an area of approx. 0.001 (mm)<sup>2</sup>, has a phase noise of -148.1 dBc/Hz at 1-MHz offset frequency and consumes 9.97 mW from a 1.2-V supply achieving a figure of merit (FoM) of 201.8 dBc/Hz.

## Session C1L-C: SPECIAL SESSION: Low-Power Devices, Circuits, Systems, and Algorithms for the Internet of Things I

**Chair:** Aatmesh Shrivastava, *Northeastern University*

**Co-Chair:** Vishal Saxena, *University of Idaho*

**Time:** Wednesday, August 7, 2019, 8:00 - 9:30

**Location:** Mesquite I

### **Design Techniques for Zero Steady-State Output Ripple in Digital Low Dropout Regulators** ..... 1041

*Saurabh Chaubey, Meghna Madhusudan, Ramesh Harjani*

University of Minnesota, United States

We present two technology portable design techniques to achieve zero steady-state output voltage ripple in digital LDOs. Traditional digital LDOs have an inherent output voltage ripple due to the limit cycle oscillations at a frequency of  $F_{\text{clock}}/(2 \cdot \text{Mode})$ . We use a 4-bit digital LDO as the test vehicle to investigate these two new techniques. The first method uses body biasing of the switches via an auxiliary analog loop to minimize the ripple voltage. Effectively, the analog loop enables the power switches to carry the extra ripple current and has little impact on the efficiency. In the second method, zero steady-state ripple is achieved by modulating the gate-driver voltage-swings at the power-switch gate. In both the techniques, when the digital LDO is in steady state, the analog loop only carries the ripple current magnitude. Control from the analog and digital loops are ping-ponged based on load transients. The LDO design handles inputs from 0.5-1.5V and supports a 0.4-1.2V output voltage for a load range of 0.1-to-20mA (200X). The LDO achieves 99.4% current efficiency and near-zero output voltage ripple.

### **Efficient Broadband Class AB Amplifier** ..... 1045

*Jose Silva-Martinez, Tanwei Yan, Junning Jiang, Jian Shao*

Texas A&M University, United States

In this paper, feed-forward and class AB techniques are explored for the design of high-frequency Operational Transconductance Amplifiers (OTA) suitable for ADC architectures. The paper is focused on high gain broadband amplifiers; the first part of the paper revisited the recycling folded-cascode (RFC) architectures. These topologies are power efficient solutions but careful design is needed to avoid the presence of medium-frequency zero-pole pairs that may significantly increase residue amplifier settling time. The two stage class AB amplifier is revisited as well; the popular Monticelli's biasing circuit for class AB amplifiers is power efficient and result in high slew-rate solutions. An alternative class AB solution is proposed in this paper. The biasing of the class AB output stage employs a common-mode feedback, and results in a faster and more power efficient architecture; power consumption is around 75% that of the conventional class AB architecture and shows 3dB lower IM3 for the design of a state-variable 25MHz high-Q biquadratic filter.

**A Femto/Pico-Watt Feedforward Leakage Self-Suppression Logic Family in 180 nm to 28 nm Technologies ... 1049**

<sup>1</sup>Joao P. Cerqueira, <sup>2</sup>Jieyu Li, <sup>1</sup>Jiangyi Li, <sup>2</sup>Weifeng He, <sup>1</sup>Mingoo Seok

<sup>1</sup>Columbia University, United States; <sup>2</sup>Shanghai Jiao Tong University, China

We present a novel logic family, titled feedforward leakage self-suppression logic (FSL), for nanowatt and sub-nanowatt always-on circuits. It addresses the prohibitively long delay of existing ultra-low leakage logic families without requiring sleep or mode control signals to exercise the leakage-suppression mode. Implemented in 180-nm CMOS, the proposed logic family achieves femto-watt per-gate leakage and a fan-out-of-4 (FO4) delay of 10.2  $\mu$ s, a remarkable speed enhancement of 150X over the prior art in the same process in the same leakage level. We also investigate the impact of technology scaling by designing the FSL logic family additionally in 65-nm and 28-nm processes. In a 28-nm process, the FSL can achieve about 70 ns FO4 delay and 10 picowatts per-gate leakage. Finally, we prototype a finite impulse response filter core for physical sensing systems in a 180 nm. The filter can achieve the power consumption of 109 picowatts for sparse, i.e., predominantly constant or slowly changing, input signals at 1 kHz clock frequency.

**Session C1L-D: SPECIAL SESSION: Wireline Communications for High-Performance Computing Applications I**

**Chair:** Armin Tajalli, *University of Utah*

**Time:** Wednesday, August 7, 2019, 8:00 - 9:30

**Location:** Quorum I & II

**Affordable Sequence Decoding Techniques for High Speed SerDes ..... 1053**

Zarraf Huda, Shovon Dey, Aaron Monai, Aurangozeb, Masum Hossain

University of Alberta, Canada

Higher data rate requirements in data centers have motivated more spectrum efficient modulation to combat additional ISI at higher frequencies. But this also leads to significant SNR penalty. In addition to that technology scaling is shifting equalization from analog domain to the digital domain. Therefore, recent trend is to explore ADC-DSP based receiver where higher performance equalization such as viterbi decoder can be implemented. But the power consumption and complexity have limited their adoption in conventional SerDes applications. In this work we will introduce several low power implementation techniques such as analog to sequence conversion and direct branch matrix estimation to explore possibility of sequence decoding in SerDes domain. Implemented prototype validates that the proposed sequence decoding is capable of compensating 35+ dB loss at 10 Gb/s with better than 10 pJ/bit energy efficiency.

**A Stochastic Wireline Communication System ..... 1057**

Tejasvi Anand

Oregon State University, United States

This paper proposes a stochastic wireline communication system. In the proposed stochastic system, the information is encoded in the statistical parameter of noise such as standard deviation, and the noise signal is transmitted on the channel. The receiver estimates the standard deviation of the received noise signal and recovers the information. A stochastic receiver architecture, which can differentiate between the noise signals with two different standard deviations is presented. Using mathematical modeling, this paper demonstrates that the proposed stochastic transceiver has a potential to improve the SNR by more than 3dB over a conventional uncoded deterministic transceiver.

**Spectrum-Efficient Communication over Copper using Hybrid Amplitude and Spatial Signaling ..... 1061**

Rajath Bindiganavile, Armin Tajalli

University of Utah, United States

This article analyzes the potentials of different signaling methods to reach very high data communication speeds over copper channels. As the available bandwidth is limited in this type of channels, sensitivity to ISI (inter-symbol interference) turns out to be the key parameter influencing both data rate, and energy consumption. Performance of some of the main common signaling methods, all based on non-return to zero (NRZ), used in wire-line communications, are examined for implementing short-reach links. Moreover, it is shown that proper combination of spatial and amplitude domain coding improves the signal quality (i.e. eye opening), enabling data transfer rates beyond 112 Gb/s.

## Session C1L-E: Digital Signal Processing I

**Chair:** Tarek Elarabi, *Penn State University*

**Time:** Wednesday, August 7, 2019, 8:00 - 9:30

**Location:** Salon G & H

### **Hardware Implementation of a Parallel EVD Processor based on Jacobi Method** ..... N/A

*Yudong He, Feixiang Huo, Youjiang Liu, Botao Xiong*

China Academy of Engineering Physics, China

Computing eigenvalues and eigenvectors of a symmetric matrix is frequently encountered in adaptive array processing. In this paper an efficient parallel architecture of EVD (eigenvalue decomposition) processor based on Jacobi method is proposed. Cordic based fixed-point vector translators and rotators are its basic processors. A scheme of Jacobi ordering is also designed to provide a very high degree of parallelism. With appropriate number of Jacobi sweeps and word-length, convergence time and computation accuracy can be ensured. Implementation results show that it achieves lower resource utilization and higher performance with respect to floating-point operations.

### **Linear Error Modeling and Noise Smoothing for Improved Low-Cost IMU-Based Indoor Positioning** ..... 1069

*Nizam Kuxdorf-Alkirata, Fotios Kasolis, Dieter Brückmann, Oliver Koch*

University of Wuppertal, Germany

In order to improve the accuracy of indoor positioning systems, an auxiliary signal analysis method is embedded to a path reconstruction algorithm. The proposed method takes into account calibration data that is obtained from an inertial measurement unit while it is at rest, and continues to work on the fly to adjust the output of the path reconstruction algorithm adaptively. A post-processing filter is employed to further reduce fluctuations in the reconstructed path.

### **Design of a 2D Median Filter with a High Throughput FPGA Implementation** ..... 1073

*Anish Goel, M. Omair Ahmad, M.N.S. Swamy*

Concordia University, Canada

In this paper, a hybrid technique for median filtering of images affected by impulse noise is implemented. Our technique combines impulse noise detection, histogram based median calculation and bit-plane processing to obtain approximate median with the aim of optimizing throughput. Implementation of the proposed median filter hardware results in a throughput of 282 Full High Definition (FHD) frames per second on Zynq-7 FPGA; 48% higher than the throughput of low-latency median filter. Compared to FPGA implementation of low complexity noise removal technique, the proposed median filter utilizes 45% of FPGA slices and provides a speed-up of 2.2 on Zynq-7 FPGA.

## Session C1L-F: System Architectures II

**Chair:** Hakduran Koc, *University of Houston-Clear Lake*

**Time:** Wednesday, August 7, 2019, 8:00 - 9:30

**Location:** Addison

### **Impact of Uncertainty and Correlations on Mapping of Embedded Systems** ..... 1077

*Wenkai Guan, Milad Ghorbani Moghaddam, Cristinel Ababei*

Marquette University, United States

The impact of multiple levels of uncertainty in design parameters and uncertainty correlations on the quality of mapping solutions in embedded systems is investigated. The investigation is done with a simulation tool developed to conduct multi-objective design space exploration in order to generate robust Pareto frontiers in the solution space formed by reliability, execution time, and energy as design objectives. The simulation tool integrates proposed models for uncertainty and a hyper volume based technique for quantifying the difference between Pareto frontiers. Simulations results show that by not considering uncertainty and correlations between different sources of uncertainty can lead to overestimation of the performance of the optimal solutions.

### **Soft Voting-Based Ensemble Approach to Predict Early Stage DRC Violations** ..... 1081

*Riadul Islam, Md. Asif Shahjalal*

University of Michigan-Dearborn, United States

Reducing human effort and design schedule time is facing a tremendous challenge from the cutting-edge technology node, which hinders profitability from IC manufacturing. Initiatives like DARPA IDEA have addressed this challenge by aiming for a 24-hour design turnaround time, maximum resource utilization, and productivity of ICs. In this paper, we proposed a robust ensemble learning model to predict DRC from the placement stage, which precisely predicts design routability and DRC hotspots of a design. The proposed algorithm uses a soft voting classifier to combine random forest and gradient boosting algorithms. Our approach achieved a maximum precision, recall, and F1 score of 97%, 97%, and 96%, respectively, which are significantly better than the state-of-the-art support-vector machine (SVM)-based prediction scheme.

**A Single-Stage RISC-V Processor to Mitigate the Von Neumann Bottleneck** ..... 1085

<sup>1</sup>Toshiki Kanamoto, <sup>2</sup>Masami Fukushima, <sup>2</sup>Koichi Kitagishi, <sup>2</sup>Seijin Nakayama, <sup>3</sup>Hideki Ishihara, <sup>1</sup>Koki Kasai, <sup>1</sup>Atsushi Kurokawa, <sup>1</sup>Masashi Imai

<sup>1</sup>Hirosaki University, Japan; <sup>2</sup>Uno Laboratories, Ltd., Japan; <sup>3</sup>Aquaxis Technology, Japan

This paper presents a micro-processor which alleviates the major limitations on throughput caused by fetching instructions from program memory into the instruction register as a part of the von Neumann architecture. The proposed processor directly reads instructions from memory without latching into the instruction register. It enables to realize an efficient single stage operation, which is comparable to the pipelines. We experimentally show the effectiveness of the proposed configuration by implementing processors with the RISC-V instruction set architecture. Replacing the pipelines, the proposed processor promisingly maintains the efficiency even in applications including embedded systems which has many conditional branches.

**Charging Scheduling of Electric Vehicles using Charge Time Priority** ..... 1089

Hakduran Koc, Myrzabek Murataliev

University of Houston-Clear Lake, United States

In this paper, we focus on the charging scheduling problem considering the impact it will have on the electric grid infrastructure especially during peak hours. After studying the existing algorithms, we propose a novel algorithm to solve the charging scheduling problem considering charging priority (CTP). The CTP algorithm schedules the vehicles considering their charging time interval requests, travel time to the charging station and queuing time in addition to the actual charging time. The algorithm also equally distributes the long time-taking charging processes to available charging stations/outlets. The experimental evaluation performed using various charging scenarios clearly shows viability of the proposed algorithms that outperform the existing approaches significantly.

**WITHDRAWN**

**Session C1L-G: Control Systems, Mechatronics, and Robotics II**

**Chair:** Sorore Benabid, *Institut polytechnique des sciences avancées*

**Time:** Wednesday, August 7, 2019, 8:00 - 9:30

**Location:** Salon I & J

**FPGA-Based Real-Time Embedded Vision System for Autonomous Mobile Robots** ..... 1093

Sorore Benabid, Loïc Latour, Solène Poulain, Mohamed Jaafar

Institut Polytechnique des Sciences Avancées, France

In this paper, we developed an embedded vision system for autonomous mobile robots. This system enable to help a robot to measure in real-time the distance of an obstacle that we have defined in advance and avoid it. The vision system uses a single front camera as sources of information on the surrounding environment and an FPGA as reconfigurable and flexible device for image processing. The whole system was implemented only in VHDL a parallel programming language on a Nexys 4 DDR development board with Artix FPGA device from Xilinx that operates at 100 MHz. This allowed obtaining a real-time image processing for a 640x480 @ 30 fps video stream.

**Leader-Follower Strategy based on Distance and Heading Angles using Local Vision** ..... 1097

<sup>1</sup>J.C. Sales-Ortiz, <sup>1</sup>J.F. Ciprián-Sánchez, <sup>1</sup>E.G. Hernandez-Martinez, <sup>2</sup>E. Ferreira-Vazquez,

<sup>3</sup>J. González-Sierra, <sup>1</sup>G. Fernandez-Anaya, <sup>5</sup>J.J. Flores-Godoy, <sup>1</sup>P. Paniagua-Contro

<sup>1</sup>Universidad Iberoamericana Ciudad de Mexico, Mexico; <sup>2</sup>Universidad Católica del Uruguay, Uruguay;

<sup>3</sup>Instituto Tecnológico de La Laguna, Mexico; <sup>4</sup>Universidad Católica del Uruguay, Uruguay

This paper presents a leader-follower motion coordination strategy of an omnidirectional robot with mecanum wheels and a differential-drive robot. The follower robot is formed with respect to the leader robot using a local vision system to measure its relative distance and heading angle. Because the sensing range of the camera is bounded, the leader robot, who has better motion capabilities, follows a desired trajectory in the plane, while converging to the follower's angle using a consensus approach. The performance of the control strategy is evaluated in an experimental setup composed by two industrial robots and a motion capture system.

**Aluminum-Doped Zinc Oxide (ZnO) Inkjet-Printed Piezoelectric Array for Pressure Gradient Mapping** ..... 1101

<sup>1</sup>Steven D. Gardner, <sup>1</sup>Mohammad R. Haider, <sup>1</sup>Md Toriqul Islam, <sup>1</sup>J. Iwan D. Alexander, <sup>2</sup>Yehia Massoud

<sup>1</sup>University of Alabama at Birmingham, United States; <sup>2</sup>Stevens Institute of Technology, United States

Inexpensive and flexible sensors are being designed as inkjet-printed circuits (iPCs) to solve a dynamic range of conditional issues in the biomedical, environmental, civil and industrial fields. The combination of print pattern, material choice and layering structure give iPCs a robust platform for developing products not attainable with printed circuit boards (PCBs). In this report, a fully printed pressure sensing array was created as a multipurpose device useful for pressure mapping applications. The printed array of gate-less field effect transistors utilizes aluminum-doped zinc oxide (ZnO) as the semiconducting layer due to its piezoelectric properties. Testing shows single nodes in the array detect various levels of pressure and the entire array acts as a pressure gradient map, depending on the circuit containment method. The report ends with a discussion of testing and research for future applications.

**Implementing Stochastic Bayesian Inference: Design of the Stochastic Number Generators** ..... 1105

*David H.K. Hoe, Chet Pajardo II*

Loyola University Maryland, United States

Bayes' rule can be computed stochastically using a simple Muller C-element, providing an efficient means of implementing Bayesian inference for autonomous robots. This provides such machines with the ability to make decisions when there is uncertainty in the data or models, enabling adaptation to unknown or dynamic environments. Prior studies have not addressed the practical aspects of designing the stochastic number generators (SNGs) required for creating the probabilistically-encoded values at the inputs. In this work, two approaches are evaluated: the use of linear feedback shift registers (LFSRs) and the use of low discrepancy sequence (LDS) generators. In the case of the LFSRs, this paper shows that there is no significant degradation in performance when several SNGs are shared with one LFSR provided a sufficient amount of circular shifting is used between each SNG. Results show an LDS generator is beneficial for lowering the amount of autocorrelation that is input into the C-element, resulting in improved performance.

**Session C2L-A: Photonics**

**Chair:** Samuel Palermo, *Texas A&M University*

**Time:** Wednesday, August 7, 2019, 11:30 - 12:30

**Location:** Bent Tree I & II

**Modeling of Silicon Photomultiplier based on Perimeter Gated Single Photon Avalanche Diode** ..... 1110

*Mst Shamim Ara Shawkat, Md Sakib Hasan, Nicole McFarlane*

University of Tennessee, United States

In this paper, we present a new electrical model for perimeter gated single photon avalanche diode (PGSPAD) based silicon photomultiplier (SiPM) detector. PGSPAD is a SPAD with an added polysilicon gate. The extra gate terminal of the PGSPAD device mitigates the perimeter edge breakdown and tunes the operating range, noise performance, efficacy. The proposed PGSPAD SiPM model allows to accurately simulate the static, dynamic and stochastic noise behavior of the SiPM detector considering the built-in randomness of the physical process fundamental to the device operation with the effect of additional gate terminal. Simulation results are validated with experimental measurements of the PGSPAD SiPM fabricated in 0.5  $\mu\text{m}$  CMOS process. Simulation results show very good matching with experimental measurements. The proposed model is a helpful simulation tool for the CMOS PGSPAD SiPM designer to evaluate the effect of parameters with additional gate terminal to optimize the performance and the PGSPAD SiPM user to design the optimum readout electronics.

**A CMOS Photonic Optical PAM4 Transmitter Linearized using Three-Segment Ring Modulator** ..... 1114

*Rui Wang, Vishal Saxena*

University of Idaho, United States

A scheme to realize Optical PAM-4 transmitter by driving a three-segment microring modulator with tunable voltage-mode drivers is presented. This proposed scheme provides linearly spaced PAM-4 levels and is further categorized into two schemes, namely higher "0" and lower "1" tuning. The two schemes are verified using co-simulation of voltage-mode drivers implemented in 65nm CMOS and Verilog-A compact models for photonic components based on a silicon photonic process from IMEC. Also, the robustness of our proposed scheme can be proved by achieving high linearity when phase-shifter length variation is present.

**Segmented Digital SiPM** ..... 1118

*<sup>1</sup>Vikas Vinayaka, <sup>1</sup>Sachin P. Namboodiri, <sup>1,2</sup>Angsuman Roy, <sup>1</sup>R. Jacob Baker*

<sup>1</sup>University of Nevada, Las Vegas, United States; <sup>2</sup>Freedom Photonics, LLC, United States

A digital silicon photomultiplier (SiPM) using segmentation technique is designed, simulated and fabricated in the AMS 0.35  $\mu\text{m}$  SiGe BiCMOS process. The digital SiPM is intended for photon counting applications. The digital SiPM consists of 16 avalanche photodiodes (APD) each with active area of 24  $\mu\text{m}$  x 24  $\mu\text{m}$  arranged in a 4x4 array with series 236 k ohm quench resistors. The SiPM has a peak responsivity at 490 nm wavelength and a fill factor of 12.6%. The digital SiPM generates an output 5-bit digital word. The digital SiPM occupies an area of 0.38 mm<sup>2</sup>.

## Session C2L-B: Nanoelectronics and Nanotechnology

**Chair:** Mohamed Shaban, *Southern Arkansas University*

**Time:** Wednesday, August 7, 2019, 11:30 - 12:30

**Location:** Preston Trail I & II

### Exploring Carbon Nanotubes for VLSI Interconnects ..... 1122

*Joshua A. Santos, Troy F. Kelly Jr., Muhammad S. Ullah*

Florida Polytechnic University, United States

As a result of a decrease in cross-section, increases have been noted in several thermal and electric properties of copper interconnects. To mitigate such concerns, new approaches are being considered for new wiring solutions for VLSI technologies. The incorporation of carbon nanotubes (CNTs) in VLSI design to replace existing interconnection material, may be an efficient and cost-effective evolution from current materials. Carbon nanotubes, more specifically multi-walled carbon nanotubes (MWCNT), have been identified as potential alternatives to diminish such concerns. This paper will delineate the shared and differing aspects of each of the CNT structures.

### Simulation and Experimental Studies of Electrical Characteristics of Nano Metal–Semiconductor Interfaces ..... 1127

*Fatmah Alkindi, Shashikant P. Patole, Hassan Barada, Moh'd Rezeq*

Khalifa University of Science and Technology, U.A.E.

Nano M-S contacts show a non-conventional I-V behavior compared to the planar–Schottky contacts. The enhanced tunneling current due to the narrowing barrier width results from the enhanced electric field at the nano M-S interface. Nano Schottky junctions are sensitive to different doping concentrations of n-type semiconductor substrates. The low dope concentration substrate increases the probability of free electrons in the metal to tunneling through the thin junction barrier to the conduction band of the semiconductor. The model was examined using conductive Atomic Force Microscope with a gold coated nano tips and compared with the simulation model.

### Design Considerations for Insulator Metal Transition based Artificial Neurons ..... 1131

*Sherif Amer, Md Sakib Hasan, Md Musabbir Adnan, Garrett S. Rose*

University of Tennessee, United States

This work presents an Insulator Metal Transition (IMT) based Integrate-And-Fire (IAF) neuron. The proposed neuron leverages the switching mechanism of the IMT device to deliver the neuron functionality without the need for complex CMOS circuitry. The IMT neuron parameters such as the threshold voltage and the refractory period, however, are dependent on the device parameters. Design expressions for the IMT neuron are derived. These expressions can aid designers choosing the proper circuit variables given a specific IMT device with a particular set of device parameters.

## Session C2L-C: SPECIAL SESSION: Low-Power Devices, Circuits, Systems, and Algorithms for the Internet of Things II

**Chair:** Aatmesh Shrivastava, *Northeastern University*

**Co-Chair:** Vishal Saxena, *University of Idaho*

**Time:** Wednesday, August 7, 2019, 11:30 - 12:30

**Location:** Mesquite I

### Asynchronous Stream Computing for Low Power IoT ..... 1135

*Patricia Gonzalez-Guerrero, Mircea R. Stan*

University of Virginia, United States

Asynchronous circuits have many advantages over their synchronous counterparts in terms of robustness to parameter variations, wide supply voltage ranges, and potentially low power by not needing a clock, yet their promise has not been translated yet into commercial success due to several issues related to design methodologies and the need for handshake signals. Stochastic computing is another processing paradigm that has shown promises of low power and extremely compact circuits but has yet to become a commercial success mainly because of the need for a fast clock to generate the random streams. The Asynchronous Stream Processing circuits described in this paper combine the best features of asynchronous circuits (lack of clock, robustness) with the best features of stochastic computing (processing on streams) to enable extremely compact and low power IoT sensing nodes that can finally fulfill the promise of smart dust, another concept that was ahead of its time and yet to achieve commercial success.

<b>CMOS based Ultra-Low Power High-Precision Analog Vector Matrix Multiplication Circuit with <math>\pm 0.1\%</math> Error for Vision Application</b> .....	1139
<i>Nikita Mirchandani, Aatmesh Shrivastava</i>	
Northeastern University, United States	

This paper presents the design of a low power multiplier cell which multiplies an input voltage with current. The multiplier achieves high precision with  $\pm 0.1\%$  error for a wide range of both voltage and current. An approach to increase the range of current is also presented. The multiplier cell is used to perform 2-D discrete convolution on input matrix of size  $3 \times 3$  with a  $2 \times 2$  kernel. The outputs of the matrix multiplier are available after  $7.5 \mu s$ , which is independent of the matrix size.

<b>High LRS-Resistance CMOS Memristive Synapses for Energy-Efficient Neuromorphic SoCs</b> .....	1143
<i>Vishal Saxena</i>	
University of Idaho, United States	

A gamut of emerging non-volatile memory (NVM) devices, aka memristors, are currently being explored for mixed-signal hardware implementation of artificial neural networks. These constitute vector by matrix multipliers (VMMs) and Neuromorphic computing circuit implementations using NVM crossbar arrays. However, transistor-level circuit designers need to accommodate non-ideal behavior of these devices, that includes variability, low-resistance, finite resolution, relaxation of states, and endurance. In this work, we explore techniques for high-LRS (low resistance state) synapses/weights using CMOS-NVM integration that are essential for energy-efficient implementation of Neuromorphic System-on-a-Chip (NeuSoC).

## **Session C2L-D: SPECIAL SESSION: Wireline Communications for High-Performance Computing Applications II**

**Chair:** Armin Tajalli, *University of Utah*

**Time:** Wednesday, August 7, 2019, 11:30 - 12:30

**Location:** Quorum I & II

<b>Design Considerations and Performance Trade-Offs for 56Gb/s Discrete Multi-Tone Electrical Link</b> .....	1147
<sup>1</sup> <i>Gain Kim</i> , <sup>1</sup> <i>Woohyun Kwon</i> , <sup>2</sup> <i>Thomas Toifl</i> , <sup>3</sup> <i>Yusuf Leblebici</i> , <sup>1</sup> <i>Hyeon-Min Bae</i>	
<sup>1</sup> Korea Advanced Institute of Science and Technology, Korea; <sup>2</sup> Cisco Systems, Switzerland;	
<sup>3</sup> Ecole Polytechnique Federal de Lausanne, Switzerland	

For communicating over mid-to-long-reach electrical links at a data-rate above 56Gb/s, ADC-based receiver (RX) has become a dominant architecture due to its strong equalization capability using complex digital signal processing algorithm benefiting from the extreme process node shrinkage. This paper discusses the design of  $>56$ Gb/s DAC/ADC-based wireline transceiver (TRX) with discrete multi-tone (DMT) modulation. Some notable differences between wireless orthogonal frequency division multiplexing (OFDM) systems and wireline DMT systems are discussed, and some practical design considerations for a multiple tens-of-Gb/s DMT RX is provided.

<b>Jitter-Robust Multicarrier ADC-Based Serial Link Receiver Architecture</b> .....	1151
<sup>1</sup> <i>Julian Camilo Gomez Diaz</i> , <sup>2</sup> <i>Shiva Kiran</i> , <sup>1</sup> <i>Samuel Palermo</i> , <sup>1</sup> <i>Sebastian Hoyos</i>	
<sup>1</sup> Texas A&M University, United States; <sup>2</sup> Intel Corporation, United States	

A multicarrier serial link receiver architecture allows for expanded symbol times to significantly relax the sampling clock jitter requirements that are currently imposing major limitations on achieving higher data rates. The proposed receiver utilizes a correlator-bank architecture with frequency channelization performed with down-conversion mixers, filters, and analog-to-digital converters (ADCs) for digitization. Continuous frequency-domain channel allocation is achieved with the utilization of digital inter-channel interference (ICI) cancellation. A detailed receiver noise analysis is presented and transient bit-error-rate simulations are utilized to evaluate the system performance with different modulation formats used on the multicarriers. Relative to a conventional four-level pulse amplitude modulation (PAM-4) system, the proposed receiver allows for a 3X improvement in jitter tolerance when operating at 64 Gb/s over a channel with 25 dB loss at 16 GHz.

<b>Design of a 180 nm CMOS Transceiver for Implantable Wireline Communication, Achieving 800 Mbps at BER<math>&lt;1e-12</math> with 22.4 dB of Channel Loss</b> .....	1155
<i>Naila Tasneem, Taufiq Ahmed, Ross M. Walker</i>	
University of Utah, United States	

Wireline communication for implantable devices is an emerging topic in circuits and systems research, motivated by progress in electronic interfaces that are used in experimental neuroscience and neural prosthetic applications. Special considerations are required for maintaining robust operation in a physiological environment, including low voltage signaling over specialized interconnect that experiences high channel loss. This manuscript reports on the design and simulation of a full wireline transceiver in 180 nm CMOS, which achieves 800 Mbps at BER  $< 1e-12$  with -22.4 dB of channel loss, with power utilization of 10.8 pJ/bit in the TX and 2.3 pJ/bit in the RX. The design was simulated with S-parameters extracted from characterization of a  $\sim 1$ -meter implantable wireline link immersed in saline solution. Implementation in the 180 nm process, which is highly suitable for integration with neural recording and stimulation electronics, presents circuit design challenges for simultaneously achieving high speed, low voltage operation, low power, and small area.

## Session C2L-E: Digital Signal Processing II

**Chair:** M. Omair Ahmad, *Concordia University*

**Time:** Wednesday, August 7, 2019, 11:30 - 12:30

**Location:** Salon G & H

### **Modified Corrector-Comb-Based Decimator with Improved Passband and Aliasing Rejection** ..... 1159

*Gordana Jovanovic Dolecek, Loth M. Barba-Maza*

INAOE, Mexico

This paper presents a modified two-stage corrector comb-based decimation structure with an improved magnitude characteristic in all folding bands. This is achieved by inserting a simple multiplierless filter into the first stage of the two-stage corrector-comb-based structure. Additionally, the maximum absolute value of the passband deviation is decreased and it is equal to 0.1 dB, for the cascade of three and four combs, while for the cascade of two and five combs it is equal to 0.2 dB. The method is illustrated with one example. The comparisons with the methods in literature are also included.

### **An Improved Multi-Dimensional Approach to Wave Digital Filters with Topology-Related Delay-Free Loops using Automatic Differentiation** ..... 1163

*Lech Kolonko, Jörg Velten, Anton Kummert*

University of Wuppertal, Germany

To avoid the occurrence of non-computable, delay-free loops, classic Wave Digital Filters (WDFs) usually exhibit a tree-like topology. However, recent advances led to a strictly modular realization of the former structures by identification of contractivity properties of WDFs, allowing an assured converging iterative procedure, which depends on the presence of artificial port resistances. In this paper, an improved semi-modular approach based on Multi-dimensional Wave Digital Filters (MDWDFs) is presented for the mentioned topologies. Therefore, a new method of Automatic Differentiating Wave Digital Filters (ADWDFs) is proposed to overcome convergence speed limitations induced by artificial port resistances, making the improved approach independent of the same.

## Session C3L-B: Analog Design Applications

**Chair:** Jose Silva-Martinez, *Texas A&M University*

**Time:** Wednesday, August 7, 2019, 13:30 - 15:00

**Location:** Preston Trail I & II

### **Inrush-Current Limiting and Soft-Switching Techniques for Filament Light Source Regulator** ..... 1167

*Islam Mostafa, Ahmed Saeed, Mina Gad, Botros George*

Si-Ware Systems, Egypt

Inrush-current limiting voltage regulators are considered important components in many voltage and current drivers applications, to reduce the startup surge of current from the voltage supply to the supplied loads. Moreover, driving stable current to multiple filament light sources is necessary to improve their life-time and reduce light fluctuations. In this paper, a fully-integrated soft-start linear voltage regulator is proposed, for driving high current to filament light sources. In addition to the soft startup feature, this proposed technique is used to allow introducing new loads during operation without disturbing the regulated output. The design has been implemented in 130nm technology. The maximum driving current is 1.5A from 5V supply. Minimum drop-out voltage of 250mV is used to supply different filament light sources.

### **Energy-Efficient Analog Front-End Design for Ultrasound Imaging Applications** ..... 1171

*Jianguo Diao, Shuai Li, Yimin Wu, Fan Ye, Jun Xu, Junyan Ren*

Fudan University, China

An energy-efficient analog front-end circuit for ultrasound imaging applications in X-FAB's 0.18-micron Modular high-voltage (HV) SOI CMOS technology is presented. The front-end circuit is composed of a supply-doubled three-level HV pulser and a low power complementary noise-canceling (NC) low noise amplifier (LNA). The proposed HV pulser can generate a three-level 53 V<sub>pp</sub> pulse from 30 V supply at 10MHz frequency, which improves transmitter (Tx) efficiency when compared with conventional methods. The low power LNA can achieve a 2.5 dB noise figure (NF), 15.2 dB voltage gain while only consuming 0.27 mW at 1.8 V supply voltage.

### **VCO-Based Feature Extraction Architecture for Low Power Speech Recognition Applications** ..... 1175

*Eric Gutierrez, Carlos Perez, Fernando Hernandez, Luis Hernandez*

Carlos III University of Madrid, Spain

A new approach for circuits devoted to speech recognition and voice activity detection is proposed. This new approach is based on using VCO-based ADC filters, which enable us to implement an architecture with very small area and low power consumption. The architecture is validated by behavioral simulation and designed in a 130-nm CMOS process to estimate the occupied area and the power consumption. The simulated results show that the solution is the best in terms of area with a competitive power consumption, very suitable for portable devices and Internet-of-things (IoT) applications.



## Session C3L-C: MEMS, NEMS and Emerging Technologies

**Chair:** Mohamed Shaban, *Southern Arkansas University*

**Time:** Wednesday, August 7, 2019, 13:30 - 15:00

**Location:** Mesquite I

### **Compact Scalable Dynamic TSV IR Drop Compensation for Power Delivery in 3D Packages** ..... 1179

<sup>1</sup>Arjun Chaudhuri, <sup>2</sup>Sukeshwar Kannan, <sup>3</sup>Luke England, <sup>3</sup>Jack Golz

<sup>1</sup>Duke University, United States; <sup>2</sup>Lightmatter, United States; <sup>3</sup>GlobalFoundries, United States

We present a low-area, scalable compensation method for the IR drop appearing across a power through-silicon via (TSV) in a 3D package. The proposed architecture provides real-time IR drop compensation of the top-die voltage supplied by the integrated voltage regulator (IVR) in the bottom die and has an area overhead of 0.053 mm<sup>2</sup> only.

### **Approximate in-Memory Computing on ReRAM Crossbars** ..... 1183

Amad Ul Hassen, Salman Anwar Khokhar

University of Central Florida, United States

To fulfill the growing demands of modern computing tasks such as multimedia processing, artificial intelligence, pattern matching, and data mining etc, advancements have been made in approximate hardware and software designs for such error tolerant, "soft" applications. We present a novel framework for approximate in-memory computing on memristive crossbars. First, we generate "Approximate Reduced Ordered Binary Decision Diagram" (ROBDDs) representations of arbitrary compute kernels. These Approximate ROBDDs are then mapped to crossbar circuits for flow-based in-memory execution. We make improvement on two fronts, (i) approximation approach reduces computational requirements without sacrificing much accuracy (ii) in-memory computing circumvents the von Neumann bottleneck by unifying processing and storage. Our approach generates designs that are \$approx\$ 10-80% more compact than exact designs while sacrificing small (less than 10%) amounts in accuracy. Our approach synthesized a crossbar design for edge detection that is 72% more compact than the state of the art on approximate synthesis for flow-based computing.

### **Chemico-Capacitive Sensing via Dielectric Loading** ..... 1187

Parthiban Rajan, Savas Kaya, Jason Wright, Akanksha Rohit, Tianyi Cai, Patrick Hanlon

Ohio University, United States

We illustrate a novel approach of capacitive sensing via selective adsorption of metal ions into its dielectric layer, hence leading to measurable differences in its capacitance. Printed interdigitated capacitors capped with dielectrics capable of selectively adsorbing Zn ions and heavy metal ions are presented as examples to the proposed dielectric loading approach. Magadiite (Na<sub>2</sub>Si<sub>14</sub>O<sub>29</sub>) provides the high selectivity for Zn and Dowex G26 (DG26) ion exchange resin serves as a dielectric with high affinity toward heavy-metal ions. Measured characteristics of these simple but effective capacitors show that they can be especially beneficial in low-cost sensing solutions for qualitatively and quantitatively environmental and biomedical monitors.

### **Memristor based Multifunction Oscillator** ..... 1191

Isaac Abraham, Saiyu Ren

Wright State University, United States

Computing with memristors is a nascent yet active field with circuit applications spanning neuromorphic, digital and analog domains. This paper presents the SPICE implementation of a nontrivial multifunction voltage controlled oscillator. The SPICE model for the memristor is a derivative based on research associating vacancy migration with a Burgers-like variable coefficient advection partial differential equation. The unique topology, biasing and use of a single comparator makes the design a novel, low power, simple CMOS compatible architecture.

## Session C3L-D: Wireless and Wearable Systems

**Chair:** Vishal Saxena, *University of Idaho*

**Time:** Wednesday, August 7, 2019, 13:30 - 15:00

**Location:** Quorum I & II

### **Design of a Wearable Carpal Tunnel Syndrome Monitoring Device** ..... 1195

Michael Mack, Cheol-Hong Min

University of St. Thomas, United States

This paper outlines our research and development of a wireless wearable wrist position detection system that monitors and tracks aggravated symptoms of Carpal Tunnel Syndrome using sensors, microcontroller, and Bluetooth communication. The proposed system uses flex sensors to detect the changes in the wrist positions. Corresponding voltage values are A/D converted and transmitted to a computer to be displayed, saved and further analyzed to determine the position of the wrist. The proposed system provides non-invasive methods that enable a long term, mobile monitoring of the wrist positions with minimal intrusion to a patient. The proposed system is also equipped with a feedback system to alert the user of aggravating conditions.

**A Low-Cost BLE based Sensor Platform for Efficient Received Signal Strength Monitoring** ..... 1199

*Gerrit Maus, Nizam Kuxdorf-Alkirata, Dieter Brückmann, Mustafa Gemci*

University of Wuppertal, Germany

In order to support optimized Received Signal Strength monitoring, a low-cost sensor platform based on Bluetooth Low Energy is introduced. Using this platform RSS measurements of individual radio channels can be performed within a highly configurable mesh network with sampling rates of up to 5 kHz and an accuracy of 0.2 dB. Measured RSS can be either shared between all devices in the network in real-time or they may be stored inside each device during the time of measurement and get distributed afterwards. We analyse and describe the characteristics of the suggested platform in detail and present, as an example, a device-free indoor localization application.

**A Monolithically Integrated Time-of-Flight Sensor with Large Area Silicon Avalanche Photodiode** ..... 1203

*Asif Chowdhury, Robert F. Karlicek, Mona M. Hella*

Rensselaer Polytechnic Institute, United States

This paper presents a monolithically integrated CMOS receiver integrated circuit (IC) for a pulsed time-of-flight (TOF) laser range-finder in 0.35 $\mu$ m CMOS technology. To the best of the author's knowledge, this is the first reported fully integrated TOF CMOS receiver including the photo detector for an indoor pulsed based laser rangefinder.

**Performance Evaluation of RZF Precoding in Multi-User MIMO Systems** ..... 1207

*<sup>1,2</sup>Bishoy Saleeb, <sup>2</sup>Mohamed Shehata, <sup>2,3</sup>Hassan Mostafa, <sup>2</sup>Yasmine Fahmy*

<sup>1</sup>Modern Sciences and Arts University, Egypt; <sup>2</sup>Cairo University, Egypt; <sup>3</sup>Zewail City of Science and Technology, Egypt

In this paper, the transmission performance of the downlink of linearly precoded multi-user multiple input multiple output (MIMO) systems is investigated. The zero forcing (ZF), regularized ZF (RZF) and minimum mean squared error (MMSE) precoding schemes are considered, and the bit error rate (BER) is adopted as the performance metric of interest. Simulation results indicate that, an adequate BER performance is achieved by the proper control of the design parameters of RZF precoding. Moreover, a relationship between the number of users' antennas and the BS is observed, such that an adequate BER performance is achieved.

## **Session C3L-E: Embedded Electronics**

**Chair:** Juan Montiel-Nelson, *University of Las Palmas de Gran Canaria*

**Time:** Wednesday, August 7, 2019, 13:30 - 15:00

**Location:** Salon G & H

**A LiDAR based Proximity Sensing System for the Visually Impaired Spectrum** ..... 1211

*Nethra Krishnan*

Jasper High School, United States

A low-cost LiDAR embedded proximity sensing system is conceptualized and prototyped targeting the needs of the Blind and Deaf-Blind. The efficacy of low-cost LiDAR is studied and its applicability is demonstrated using a single microcontroller. Servo based panning of the LiDAR is integrated enabling a 2D topographical capture, which is mapped to the brain by a novel audio balance technique. For the deaf-blind, an alternative haptic glove is devised with haptic mapping. Finally, an active in-motion (AIM) guidance is proposed by harvesting the data dynamically and providing the user a directional guidance actively.

**Power Optimization of Arduino-Based Sensor System for Salton Sea Environmental Monitoring** ..... 1215

*Kristian Diaz, Ying-Khai Teh*

San Diego State University, United States

Commercial-off-the-shelf (COTS) microcontroller based embedded system and sensors are used to monitor the Salton Sea environmental hazard. Power consumption data of microcontroller CPU core, I/O buses (UART, SPI and I2C), and peripheral sensors (GPS and optical-based dust sensor) are first presented, followed by optimization techniques using software control and hardware-assisted power gating technique. A set of logic based on sensor input is introduced to create a conscious way to optimize system power. Caveats of hidden power cost during field operation of peripheral sensors are also discussed. Our findings show that a conscious power-optimized design can simultaneously extend system run time to collect additional data up to 84% higher compared to LEAP-like approach.

**Design of Wireless Smart Chair System for People with Cognitive Deficiency** ..... 1219

*Vasily G. Moshnyaga, Koji Hashimoto, Tomohiro Nogami, Kazuki Nojima*

Fukuoka University, Japan

This article describes a sensor-based wireless system which monitors sitting postures of a person with cognitive impairment, assesses risks and alarms both the person and his caregiver when the risk of falling is high. Unlike existing smart chairs, the proposed system identifies postures that might cause a person to fall from chair by using minimal number of sensors and a simple posture classification algorithm. Experimental evaluation shows that the system operates in real-time, is robust yet inexpensive.

*Pranav Gangwar, Satvik Maurya, Shubham Garg, Sakshi Goyal, Aditya S. Kumar, Preyesh Dalmia, Neeta Pandey*

Delhi Technological University, India

This paper presents an improved Othello game solver using the Hardware/Software Co-Design approach. Enhancements in Data Communication, Searching Algorithm, and Evaluation function have been made to beat the prevalent implementations. A novel 64-bit Communication model is proposed which transfers the current board position from the Processing System to the Programmable Logic through a 64-bit change board, instead of the complete 128-bit board. The proposal uses NegaScout searching algorithm along with Transposition Table and Node Ordering; and features like Opening Book, Killer Heuristics, and Bitboards. An Adaptive Evaluation function assigns variable weights to Mobility, Stability, Corner Occupancy, and Disc Differential depending upon the game stage. At a search depth of eight, the proposed communication model improves the communication overhead by 19.5%. Overall, the proposed design demonstrates 75.06% improved performance as compared to the prevalent implementation, and 6.53 times faster than its software implementation on the same platform.