

# **2020 IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS 2020)**

**San Jose, Costa Rica  
25 – 28 February 2020**



**IEEE Catalog Number: CFP20LAS-POD  
ISBN: 978-1-7281-3428-4**

**Copyright © 2020 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP20LAS-POD
ISBN (Print-On-Demand):	978-1-7281-3428-4
ISBN (Online):	978-1-7281-3427-7
ISSN:	2330-9954

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# Table of Contents

## Special Session I: Signal and Power Integrity

SS1-1	Majid Ahadi Dolatsara and Madhavan Swaminathan. <b>Determining worst-case eye height in low BER channels using Bayesian optimization.....1</b>
SS1-2	Srinidhi Ganeshan, Naveen Kumar Elumalai, and Ramachandra Achar. <b>A Comparative Study of MAGMA and cuBLAS Libraries for GPU based Vector Fitting.....5</b>
SS1-3	Xinying Wang, Thong Nguyen, and Jose E. Schutt-Aine. <b>PAM-4 Behavioral Modeling using Machine Learning via Laguerre-Volterra Expansion.....9</b>
SS1-4	José E. Rayas-Sánchez, Francisco E. Rangel-Patiño, Benjamin Mercado-Casillas, Felipe Leal-Romo, and José L. Chávez-Hurtado. <b>Machine Learning Techniques and Space Mapping Approaches to Enhance Signal and Power Integrity in High-Speed Links and Power Delivery Networks.....13</b>

## Session: Analog and Mixed Signal Design I

AMS1-1	Daniel Schrögendorfer, Thomas Leitner, and Harald Pretl. <b>A 1.2V, 1.1-dB NF, CMOS Low-Noise Amplifier using an Active-Tank Broadband Output Stage.....17</b>
AMS1-2	Arnaldo del Risco Sánchez, Robson Luiz Moreno, Luís Henrique de Carvalho Ferreira, Paulo César Crepaldi, and Tales Cleber Pimenta. <b>A minimum supply voltage Operational Transconductance Amplifier for wireless biomedical acquisition systems.....21</b>
AMS1-3	Mahmood A. Mohammed and Gordon W. Roberts. <b>The Impact of the Scaled-Down CMOS Technologies on the Step Response Degradation Caused by the Pole-Zero Doublets in the OTAs.....26</b>
AMS1-4	David Rivadeneira, Marco Villegas, Luis Miguel Procel and Lionel Trojman. <b>Optimization of active voltage rectifier/Doubler designed in 90nm technology.....30</b>
AMS1-5	Leonardo Agis, Denisse Hardy, Kenji Nakasone, Alfredo Arnaud, Joel Gak, Matias Miguez, Ronny García-Ramírez, Alfonso Chacon-Rodriguez, and Renato Rimolo-Donadio. <b>Integrated Programmable Current Source for Implantable Medical Devices.....34</b>

**Session: Imaging Techniques**

IT1-1	Ícaro Siqueira, Guilherme Corrêa, and Mateus Grellert. <b>Rate-Distortion and Complexity Comparison of HEVC and VVC Video Encoders.....38</b>
IT1-2	Jan-Harm Betting, Vincenzo Romano, Laurens Bosman, Zaid Al-Ars, Chris De Zeeuw, and Christos Strydis. <b>Stairway to Abstraction: an Iterative Algorithm for Whisker Detection in Video Frames.....42</b>
IT1-3	Vinicius Borges, Murilo Perleberg, Vladimir Afonso, Marcelo Porto, and Luciano Agostini. <b>A Low-Complexity Algorithm and Its Low-Power and High-Throughput Architecture for 3D-HEVC DMM-1 Encoding Tool.....46</b>
IT1-4	Ryota Ishikawa, Masashi Tawada, Masao Yanagisawa, and Nozomu Togawa. <b>Multi-Resolutional Image Format Using Stochastic Numbers and Its Hardware Implementation.....50</b>
IT1-5	Eduardo Zummach, Roberta Palau, Jones Goebel, Luciano Agostini, and Marcelo Porto. <b>High Throughput CDEF Architecture for the AV1 Decoder Targeting 4K@60fps Videos.....54</b>

**Session: Interactive Presentations**

IP1-1	Carlos Alberto Sanabria, Mónico Linares-Aranda, Rogelio M. Higuera, and Francisco Javier De la Hidalga Wade. <b>Impact and Modeling of Möbius Connection in the Rotary Traveling Wave Oscillator Performance.....58</b>
IP1-2	Md Adnan Zaman, Rajeev Joshi, and Srinivas Katkooori. <b>Analysis of Radiation Impact on Memristive Crossbar Arrays.....62</b>
IP1-3	David Pollreisz and Nima Taherinejad. <b>Reliable Respiratory Rate Extraction using PPG.....66</b>
IP1-4	Thomas V. Fontanari, Guilherme Paim, Leandro M. G. Rocha, Patrícia Ücker, Eduardo Costa and Sergio Bampi. <b>An Efficient N-bit 8-2 Adder Compressor with a Constant Internal Carry Propagation Delay.....70</b>
IP1-5	Tiago Mallmann Rohde and João Baptista dos Santos Martins. <b>Multi-Bit-Upset Memory Using New Error Correction Code Methodology.....74</b>
IP1-6	William Teles Medeiros, Hamilton Klimach, and Sergio Bampi. <b>A 40 nW 32.7 kHz CMOS Relaxation Oscillator with Comparator Offset Cancellation for Ultra-Low Power Applications.....78</b>
IP1-7	Lesley Ferreira, Mateus Moreira, Bárbara Souza, Sandro Ferreira, Filipe Baumgratz and Sergio Bampi. <b>Review on the Evolution of Low-power and Highly-linear Time-to-Digital Converters – TDC.....82</b>
IP1-8	Luis D. Murillo-Soto and Carlos Meza Benavides. <b>Fault detection in a solar arrays based on an efficiency threshold.....86</b>

**Session: Analog and Mixed Signal Design II**

AMS2-1	Siamak Delshadpour, Marc Steger, and Shrikant Singh. <b>A 0.7 <math>\mu</math>w Explicit Bandgap Less POR Circuit With Brownout Detection.....90</b>
AMS2-2	Rolando Torres, Luis E. Rueda, Nestor Cuevas, and Elkim Roa. <b>On the Design of Reliable and Accurate Current References.....94</b>
AMS2-3	Oscar Jair Cinco Izquierdo, Maria Teresa Sanz Pascual, Carlos Aristoteles De la Cruz Blas, and Belen Calvo-López. <b>Low Power CMOS Chopper Preamplifier Based on a Source-Degeneration Transconductors.....98</b>
AMS2-4	Sudipta Saha, Shoba Krishnan, and Allen A Sweet. <b>A triple mode wide locking range, low phase noise injection locked oscillator based phase shifter covering the Sub-6 GHz 5G bands.....102</b>
AMS2-5	Johan Solis-Arbustini, Pablo Mendoza-Ponce, Wolfgang H. Krautschneider, and Matthias Kuhl. <b>A 16-bit pressure sensing interface integrating a 460 fJ/conv Incremental Sigma Delta ADC for medical devices.....106</b>

**Session: Digital Circuits and Systems I**

DCS1-1	Henrique Seidel, Morgana Macedo Azevedo da Rosa, Guilherme Paim, Eduardo da Costa, Sergio Almeida, and Sergio Bampi. <b>Energy-Efficient Haar Transform Architectures Using Efficient Addition Schemes.....110</b>
DCS1-2	Esteban Garzón, Benjamin Zambrano, Tatiana Moposita, Ramiro Taco, Luis-Miguel Prócel, and Lionel Trojman. <b>Reconfigurable CMOS/STT-MTJ Non-Volatile Circuit for Logic-in-Memory Applications.....114</b>
DCS1-3	Richard Calusdian and Aaron Stillmaker. <b>Hardware Implementation of HEVC Inverse Transform in 45nm CMOS.....118</b>
DCS1-4	Akhilesh G. Naik, Debarshi Deka and Dipankar Pal. <b>ASIC Implementation of High-Speed Adaptive Recursive Karatsuba Multiplier with Square-Root-Carry-Select-Adder.....122</b>
DCS1-5	Duarte L. Oliveira, Gabriel C. Duarte, Gracieth C. Batista, Diego A. Silva and Leonardo Romano. <b>Synthesis of Asynchronous State Machines from Synchronous Specifications.....126</b>

**Session: Sensors**

<b>S1-1</b>	Roman Fragasse, Ramy Tantawy, Shane Smith, Teresa Specht, Zahra Taghipour, Phillip Van Hooser, Christopher Taylor, Theodore J. Ronningen, Earl Fuller, Rudy Fink, Sanjay Krishna, and Waleed Khalil. <b>Advancing Uncooled Infrared Imagers Using an Open-Circuit Voltage Pixel.....130</b>
<b>S1-2</b>	Kota Mizushima, Satomi Ogawa, and Takahide Sato. <b>A High-Accuracy Capacitance-to-Voltage Converter for Capacitive Sensors.....134</b>
<b>S1-3</b>	Andry Contreras, Leonardo Steinfeld, Mariana Siniscalchi, Javier Schandy, and Benigno Rodríguez. <b>A Rectenna as Energy Source for Wireless Sensor Nodes.....138</b>
<b>S1-4</b>	Alexandre de Jesus Aragão, Dionísio de Carvalho, Bruno Sanches and Wilhelmus Adrianus Maria Van Noije. <b>An improved confocal algorithm for breast cancer detection using UWB signals.....142</b>
<b>S1-5</b>	Diego Deotti, Jose Luis Ramirez Bohorquez, and Fabiano Fruett. <b>Design and characterization of a Smart Temperature sensor.....146</b>

**Session: Digital Signal Processing**

<b>DSP1-1</b>	Daniel Massicotte, Marwan A. Jaber, Chokri Neili, and Messaoud Ahmed Ouameur. <b>FPGA Implementation for the Multiplexed and Pipelined Building Blocks of Higher Radix-2<sup>k</sup> FFT.....150</b>
<b>DSP1-2</b>	Kaya Demir and Salih Ergün. <b>Analysis of Random Number Generators Based on Chaos-Modulated Dual Oscillator Architecture.....154</b>
<b>DSP1-3</b>	Matheus Mitsuo De Almeida Kotaki and Maximilian Luppe. <b>FPGA Implementation of a Pseudorandom Number Generator Based on k – Logistic Map.....158</b>
<b>DSP1-4</b>	Burak Acar and Salih Ergün. <b>A Robust Digital Random Number Generator Based on Transient Effect of Ring Oscillator.....162</b>
<b>DSP1-5</b>	Jakub Podivinsky, Ondrej Cekan, Martin Krcma, Radek Burget, Tomas Hruska, and Zdenek Kotasek. <b>Iterative Algorithm for Multidimensional Pareto Frontiers Intersection Determination.....166</b>
<b>DSP1-6</b>	Jai Gopal Pandey, Sanskriti Gupta, and Abhijit Karmakar. <b>A Unified Architecture for AES/PRESENT Ciphers and its Usage in an SoC Environment.....170</b>

**Special Session II: REHAB-CAS**

SS2-1	Beatriz Coto-Solano. <b>Challenges in the Incorporation of Rehabilitation Technology to Public Health in Costa Rica.....174</b>
SS2-2	Samuel Gaardsmoe, Maria Ovando, Kevin Bui, and Michelle J. Johnson. <b>Development of a low-cost balance assessment system for use in an affordable robot gym in low and middle income countries.....178</b>
SS2-3	Karla J. Bustamante Valles, Daniel Comaduran, Marquez, and Michelle J. Johnson. <b>Robotic Rehabilitation Therapy in Chihuahua Mexico, challenges from translating a clinical research protocol to clinical practice.....184</b>
SS2-4	Verónica Valverde-Arredondo and Arys Carrasquilla-Batista. <b>Haptic system for upper limb rehabilitation with hand grip strength measurements and Internet of Things capabilities.....188</b>
SS2-5	Carla Gomez-Carrasquilla, Karol Quiros-Espinoza, and Arys Carrasquilla-Batista. <b>Wheelchair control through eye blinking and IoT platform.....192</b>

**Session: Analog and Mixed Signal Design III**

AMS3-1	Pablo Mendoza Ponce, Gayas Mohiuddin Sayed, Lait Abu Saleh, Wolfgang Krautschneider, and Matthias Kuhl. <b>A 1.9 nW Timer and Clock Generation Unit for Low Data-Rate Implantable Medical Devices.....196</b>
AMS3-2	Eduardo Vilela Pinto dos Anjos, Dominique M. M.-P. Schreurs, and Guy A. E. Vandenbosch. <b>Phase-Control Techniques for Sub-Sampling Phase-Locked Loops.....200</b>
AMS3-3	Nader El-Zarif, Mohamed Ali, Ahmad Hassan, Morteza Nabavi, Christian Jesus B. Fayomi, and Yvon Savaria. <b>A High Efficiency and Fast Response PLL Based Buck Converter: Implementation and Simulation.....204</b>
AMS3-4	Juan Andrés Bozzo, Angel Abusleme, and José Silva-Martínez. <b>A blind calibration scheme for switched-capacitor pipeline analog-to-digital converters.....208</b>
AMS3-5	Yulang Feng, Qingjun Fan, Hao Deng, Jeffrey Chen, Runxi Zhang, Phaneendra Bikina, and Jinghong Chen. <b>An Automatic Comparator Offset Calibration for High-Speed Flash ADCs in FDSOI CMOS Technology.....212</b>

**Session: Digital Circuits and Systems II**

DCS2-1	Patrícia Ücker, Miguel R. Weirich, Guilherme Paim, Eduardo Antônio César da Costa, and Sergio Bampi. <b>Optimizing Iterative-based Dividers for an Efficient Natural Logarithm Operator Design.....216</b>
DCS2-2	Rodrigo N. Wuerdig, Vitor G. Lima, Filipe Baumgratz, Rafael Soares, and Sergio Bampi. <b>Evaluating Cell Library Sizing Methodologies for Ultra-Low Power Near-Threshold Operation in Bulk CMOS.....220</b>
DCS2-3	Arghavan Asad, Furat AL-Obaidy, and Farah Mohammadi. <b>Efficient Power Consumption using Hybrid Emerging Memory Technology for 3D CMPs.....224</b>
DCS2-4	Juliano Cavinato Zanelli, Carolina Metzler, and Ricardo Reis. <b>Gate Sizing for Power-Delay Optimization at Transistor-level Monolithic 3D-Integrated Circuits.....228</b>
DCS2-5	Jose Somarribas Escalante and Adrian Loteanu. <b>Using Micro-Processor Vector Instructions to Optimize Unsupervised Machine Learning K-Means Algorithm.....232</b>

**Session: Artificial Intelligence**

AI1-1	Jorge Castro-Godínez, Deykel Hernández-Araya, Muhammad Shafique, and Jörg Henkel. <b>Approximate Acceleration for CNN-based Applications on IoT Edge Devices.....236</b>
AI1-2	Brunno F Goldstein, Sudarshan Srinivasan, Dipankar Das, Kunal Banerjee, Leandro Santiago, Victor C. Ferreira, Alexandre S. Nery, Sandip Kundu, and Felipe M. G. França. <b>Reliability Evaluation of Compressed Deep Learning Models.....240</b>
AI1-3	Mingxin Zhao, Xuemin Zheng, Ke Ning, Chunhe Yao, Qian Luo, Shuangming Yu, Liyuan Liu, and Nanjian Wu. <b>A verification method for array-based vision chip using a fixed-point neural network simulation tool.....245</b>
AI1-4	Lenin Torres-Valverde, Nevrez Imamoglu, Antonio González-Torres, Toru Kouyama, and Atsunori Kanemura. <b>Evaluation of neural networks with data quantization in low power consumption devices.....249</b>
AI1-5	Sree Bala Bhamidi and Mohamed El-Sharkawy. <b>3-Level Residual Capsule Network for Complex Datasets.....253</b>



**Special Session III: Neurotechnology, Circuits and Systems Design Challenges**

SS3-1	Alfredo Arnaud and Matías Miguez. <b>Stacking Multiple Differential Pairs for a NEF&lt;1 Amplifier aimed at Electroneurographic Signal Recording.....257</b>
SS3-2	Rui Guan, Pedro G. Zufiria, Vasiliki Giagka, and Wouter A. Serdijn. <b>Circuit Design Considerations for Power-Efficient and Safe Implantable Electrical Neurostimulators.....261</b>
SS3-3	Dorian Haci, Yan Liu, Sara S. Ghoreishizadeh, and Timothy G. Constandinou. <b>Key Considerations for Power Management in Active Implantable Medical Devices.....265</b>
SS3-4	Renzo Caballero, Gonzalo Carozo, María C. Costa-Rauschert, Pablo Aguirre, Conrado Rossi-Aicardi, and Julián Oreggioni. <b>Biopotential integrated preamplifier.....269</b>

**Session: Computer Architecture**

CA1-1	Alfredo Arnaud, Matías Miguez, Joel Gak, R. Puyol, Ronny García-Ramírez, E. Solera-Bolaños, R. Castro-González, R. Molina-Robles, Alfonso Chacon-Rodriguez, and Renato Rimolo-Donadio. <b>A RISC-V Based Medical Implantable SoC for High Voltage and Current Tissue Stimulus.....273</b>
CA1-2	Ronny García-Ramírez, Alfonso Chacón-Rodríguez, Reynaldo Castro-González, Alfredo Arnaud, Matías Miguez, Joel Gak, Roberto Molina-Robles, G. Madrigal-Boza, M. Oviedo-Hernandez, E. Solera-Bolanos, D. Salazar-Sibaja, D. Sanchez-Jimenez, M. Fonseca-Rodriguez, J. Arrieta-Solorzano, and Renato Rimolo-Donadio. <b>SIWA: a RISC-V RV32I based Micro-Controller for Implantable Medical Applications.....277</b>
CA1-3	Jose Somarribas Escalante, Esteban Meneses, and Kimberly Olivas. <b>Predictive Power Consumption Model for Compute Intensive Applications in Clustered ARM A53 Embedded Systems.....281</b>
CA1-4	Wilmer Ramirez, Marco Sarmiento, and Elkim Roa. <b>A Flexible Debugger for a RISC-V Based 32-bit System-on-Chip.....285</b>
CA1-5	Bruno Sanches and Wilhelmus Van Noije. <b>A Radiation Tolerant Baseline Correction Filter for Readout Front-ends in High Energy Physics Experiments.....289</b>

**Session: Digital Communications**

DC1-1	Luiz Claudio Sampaio Ramos, Felipe Gonçalves Serrenho, and José Antonio Apolinário Jr. <b>Least squares optimized Doppler effect-based DoA estimation.....293</b>
DC1-2	Siamak Delshadpour and Michael Geng. <b>A PLL Based FSK Demodulator With Auxiliary Path.....297</b>
DC1-3	William De Carvalho Rodrigues and José Antonio Apolinário Jr. <b>An on-the-Fly FDOA-based Target Localization System.....301</b>
DC1-4	Andres Cornejo, Salvador Landeros-Ayala, Jose M. Matias and Ramon Martinez. <b>Applying Learning Methods to Optimize the Ground Segment for HTS Systems.....305</b>
DC1-5	Samuel L. Moreira, Tales C. Pimenta, Francisco M. Portelinho Junior, and Romulo M. Volpato. <b>Coexisting Analysis of 5G Networks with ISDB-T System in TV White Spaces.....309</b>

**Session: Embedded Systems**

ES1-1	Matheus F. Stigger, Victor H. S. Lima, Leonardo B. Soares, Cláudio M. Diniz, and Sergio Bampi. <b>Approximate SATD Hardware Accelerator Using the 8x8 Hadamard Transform.....313</b>
ES1-2	Ronny Zarate-Ferreto, Kaleb Alfaro-Badilla, Carlos Meza Benavides, Carlos Salazar-García, and Alfonso Chacon-Rodriguez. <b>SoC-FPGA Implementation of a Temperature-Dependent Parameters Estimator for Photovoltaic Generators.....317</b>
ES1-3	Andres Quesada-Martinez, Javier Aparicio-Morales, Jose Campos-Araya, Alfonso Chacón-Rodríguez, Ronny Garcia-Ramirez, and Renato Rimolo-Donadio. <b>Evaluation of 8b/10b FPGA Encoder Implementations for SerDes Links.....321</b>
ES1-4	Ruiqi Luo, Xiaolei Chen, and Yajun Ha. <b>Optimization of FPGA Routing Networks with Time-Multiplexed Interconnects.....325</b>
ES1-5	Deykel Hernández-Araya, Jorge Castro-Godínez, Muhammad Shafique, and Jörg Henkel. <b>AUGER: A Tool for Generating Approximate Arithmetic Circuits.....329</b>

**Special Session IV: IoT in Agribusiness**

SS4-1	Laura Hernández-Alpizar, Arys Carrasquilla-Batista, and Lilliana Sancho-Chavarría. <b>IoT application for water quality monitoring: nitrates.....333</b>
SS4-2	Alfredo Arnaud and Guillermo Costa. <b>Ultra low-cost sensors using RFID standards for data collection, for IoT systems in food production and logistics.....337</b>
SS4-3	Carlos Muñoz, Juan Huircan, Fernando Huenupan, and Pedro Cachaña. <b>PTZ camera tuning for real time monitoring of cows in grazing fields.....341</b>
SS4-4	Victor Grimblatt. <b>IoT for Agribusiness: An Overview.....345</b>

**Session: Electronic Devices**

ED1-1	Maximilian Reuter, Johannes Pfau, Tillmann A. Krauss, Mahdi Moradinasab, Udo Schwalke, Jürgen Becker, and Klaus Hofmann. <b>Towards Ambipolar Planar Devices: The DeFET Device in Area Constrained XOR Applications...349</b>
ED1-2	Oleg V. Dvornikov, Vladimir A. Tchekhovski, Yaroslav D. Galkin, Nikolay N. Prokopenko, and Anna Bugakova. <b>The Research Methodology of Dependence Mode at Parameters Dispersion of a Differential Pair on Integral JFETs in a Radiation-Hardened Structured Array MH2XA010.....353</b>
ED1-3	Marina Sparvoli, Lucas G. Silvestre, and Mario A. Gazziro. <b>Graphene oxide resistive memories with threshold switching behavior.....357</b>
ED1-4	Zarin Tasnim Sandhie, Farid Uddin Ahmed, and Masud H. Chowdhury. <b>GNRFET based Ternary Logic – Prospects and Potential Implementation.....361</b>
ED1-5	Arturo Sarmiento-Reyes and Marco A. Zamudio Hernández. <b>Image Edge Detection with a Memristive Grid: a Massive Parallel Approach.....365</b>

**Session: Filter Design**

FD1-1	Ahmed Elgarewi, Iman Moazzen, and Panajotis Agathoklis. <b>Analysis of Optimization Algorithms for Non-Uniform Filter Bank Design.....369</b>
FD1-2	Venkata Suresh Rayudu, Heechai Kang, and Ranjit Gharpurey. <b>An N-Path Filter with Multiphase PWM Clocks for Harmonic Response Suppression.....373</b>
FD1-3	George E. Antoniou and Constantine A. Coutras. <b>A New 4D Lattice FIR Digital Filter.....377</b>

**Session: System Simulation and Test**

SST1-1	Gabriel Madrigal-Boza, Marco Oviedo-Hernández, Allan Carmona-Cruz, Luis A. Chavarría-Zamora, Daniel Leon-Gamboa, Daniel Kohkemper, Ronny Garcia-Ramírez, Alfonso Chacon-Rodriguez, and Renato Rimolo-Donadio. <b>An IC Mixed-Signal Framework for Design, Optimization, and Verification of High-Speed Links...381</b>
SST1-2	Andres Malavasi Mora and Renato Rimolo-Donadio. <b>Voltage Drop Mitigation by Adaptive Voltage Scaling using Clock-Data Compensation.....385</b>
SST1-3	Jakub Podivinsky, Jakub Lojda, Richard Panek, Ondrej Cekan, Martin Krcma, and Zdenek Kotasek. <b>Evaluation Platform For Testing Fault Tolerance: Testing Reliability of Smart Electronic Locks.....389</b>
SST1-4	Siamak Delshadpour, Gijs De Raad, and Leo Liu. <b>A Type-C USB Power Delivery Chip Faced Catastrophic Failure.....393</b>
SST1-5	Eduardo Garcia, Enrique Gonzalez-Garcia, Adolfo Hernandez-Padilla, Raymundo Aguillon, and Paulo Lopez-Meyer. <b>Thermal debugging tool for servers.....397</b>