International Engineering Consortium

Euro DesignCon 2005

October 24-27, 2005 Munich, Germany

Volume 1 of 2

Printed from e-media with permission by:

Curran Associates, Inc. 57 Morehouse Lane Red Hook, NY 12571 www.proceedings.com

ISBN: 978-1-60423-625-5

International Engineering Consortium

Euro DesignCon 2005

TABLE OF CONTENTS

Volume 1

TecF	or	um	s
-------------	----	----	---

TF-MA1: Process/Design Learning from Production Test Bernd Koenemann, Chief Scientist, Mentor Graphics Corporation David Abercrombie, Design for Manufacturing Program Manager, Mentor Graphics	1
TF-MA2: Low-Power Design Techniques for SoC and Microprocessors: An Industry Perspective	V/A
TF-MA3: Advances in Time and Frequency Domain Measurements, Modeling, and Signal-Integrity Analysis of Gigabit Interconnects Dima Smolyansky, Tektronix	.13
TF-MP1: Using SystemVerilog Assertions in an AMBA 3.0 (AXI) System Design Environment	√A
TF-MP2: C/C++ Design Flow: From a C/C++ Reference to Silicon Martin Speitel, Group Manager, Fraunhofer IIS Martin Meindl, Senior Technical Manager, Co Ware Jean-Marie Saint-Paul, European Product Specialist ESL, Mentor Graphics	.89
TF-MP3: Recent Developments in Signal-Integrity Measurements and Analysis	134
TF-THA1: Practical Guidance in Achieving Design Portability	224
TF-THA2: Discussing the Limitations and Accuracies of Time and Frequency Domain Analysis of Physical-Layer Devices	348
TecPreview	
TP-TA3: Addressing DSM Design Risks with Mask-less Structured ASICs Peter Woo, eASIC Corporation Calin Monor, eASIC Corporation	399
Track 1 Application Specific Solutions	
1-TA1: Challenges in Power PC440-FS Soft Core Development: Timing Perspective	412

1-TA2: Galvanic Isolation Using Capacitive Coupling: CMOS-Technology Allows 100 Mbps and High Integration
Frank Dehmelt, FAE, Texas Instruments
1-TA3: Alternator Control IC: A High-Integration System IC with High-Power Capability and Serial Interface in an Automotive Environment
1-TP1: Design and Thermal Management of Power Distribution Units for Automotive Applications 450 Stefan Masak, Supervisor, FEM Group, Tyco Electronics AMP GmbH Andre Dressel, Development Engineer, Tyco Electronics AMP GmbH
Track 2 Chip-Level Physical Design and Verification
2-TP2: Static Timing Analysis in Ultra Deep Micron Technologies
2-WA1: Physical Optimization Algorithms for Timing Closure
2-WA2: A Flexible and Adaptive Pipelining Concept for Low Latency Interconnects
2-WA3: Addressing Design for Manufacturability (DFM) Issues in Nanometer Designs and Beyond518 Ganesan Nagasubramanian, Project Manager, Infineon Technologies Balamurugan Selvaraj, Infineon Technologies Manoj Sundareswaran, Senior Design Engineer, Infineon Technologies Arun Venkatesan, Design Engineer, Infineon Technologies Jagadeesh Kotturashettar, Senior Design Engineer, Infineon Technologies Murali Sundaram, Design Engineer, Infineon Technologies
2-WP1: Modeling Complex Silicon Effects in Nanometer Designs
2-WP2: EDA Platform: Buzzword or True Technological Benefit?
Volume 2
Track 3 IC System-Level Design
3-TA1: Evaluation of Temporal-Spatial Voltage Scaling for Processor-Like Reconfigurable Architectures 555 Thomas Schweizer, Research Assistant, University of Tübingen Wolfgang Rosenstiel, Professor, University of Tübingen Julio Oliveira Filho, Research Assistant, University of Tübingen Tobias Oppold, Research Assistant, University of Tübingen Dr. Tommy Kuhn, Research Assistant, University of Tübingen
3-TA2: Raising the Level of Abstraction for Design and Verification: SystemC and SystemVerilog in a Multilanguage Environment
Victor Berman, Group Director of Language Standards, Cadence Design Systems
3-TA3: Build and Verify Sophisticated System-on-Chip Designs in Minutes by Leveraging the Power of SPIRIT Format
Alexander Hahn, Mentor Graphics

3-WA1: Full Chip Simulation Enables Pre-Silicon Software Development
3-WA2: DSP Synthesis: A Breakthrough for System-Level FPGA Designers
3-WA3: A Novel Technique for VCO Design Having Multiple Tuning Ranges with Inbuilt Digital Controller
3-WP1: Improving the IP Evaluation Process
4-TP1: Creating a Provably Correct Design Methodology
4-TP2: Managing Verification of SoCs: An Integrated Framework for System, Design, Firmware, and Silicon Verification
4-WA1: Coverage-Driven Verification with SystemC Testbenches
4-WA2: Technical and Managerial Data about Property Checking with Complete Functional Coverage 693 Joerg Bormann, Senior Manager Verification Methodology, OneSpin Solutions GmbH Claudia Blank, Staff Engineer Formal Verification, Infineon Klaus Winkelmann, Project Manager Formal Verification, OneSpin Solutions GmbH
4-WP2: Coverage Driven HW/SW Co-Verification
Track 5 High-Speed Interconnect System Design
5-TA1: S-Parameter Based Eye Diagrams of High-Speed Links in Comparison to Direct Measurements in Time Domain

5-TA2: Simulation for Electromagnetic Compatibility (EMC) and Signal Integrity (SI) in an Integrated Environment
Christos Christopoulos, Professor, University of Nottingham T M Benson, Professor, University of Nottingham D W P Thomas, Senior Lecturer, University of Nottingham A Vukovic, , University of Nottingham S Greedy, University of Nottingham X Liu, University of Nottingham K Biwojno, University of Nottingham Y. Liu, University of Nottingham
5-TA3: Backplane Channels and Correlation between Their Frequency and Time Domain Performance . 769 John D'Ambrosia , Manager Semiconductor Relations, Tyco Electronics Adam Healey , Agere Systems
5-TP1: Modeling of Gigabit Backplanes from Measurements
5-TP2: Validating Transceiver FPGAs Using Advanced Calibration Techniques
5-WA1: Beyond 10 Gbps
5-WA2: Investigating Microvia Technology for 10 Gbps and Higher Telecommunications Systems855 Thomas Gneiting, AdMOS GmbH Advanced Modeling Solutions Roland Mödinger, ERNI Elektroapparate GmbH Remi Tuijtelaars, BSW TestSystems and Consulting by
5-WA3-1: Infotainment Communication via PCS (Polymer Cladded Silica) Fiber for Car Application880 Andreas Engel, Manager Communications Systems Technologies, Tyco Electronics
5-WA3-2: The Duobinary Format: A New Application for an Idea Published Long Ago
5-WP1: Impacts of Interconnect Solutions on Crosstalk within the Via Construction at 10Gbps907 Yianni Antoniades, Signal-Integrity Engineer, Northrop Grumman Kelvin Clarke, Signal-Integrity Engineer, Northrop Grumman
5-WP2: Connector Footprint Optimization Enables 10-Gb+ Signal Transmission
Track 6 Test and Debug
6-TA1: At-Speed Scan Transition and Path Delay Testing Using On-Chip PLL for High-Frequency Device and Low-Frequency Tester

6-TA3: Transfer Functions for the Reference Clock Jitter in a Serial Link: Theory and Applications in PCI Express
6-TP1: The Next Generation of Automated Test Pattern Generation
Awards Track
A-WA1: Measurements of Impedance, Current, and Worst-Case Noise on Chip Power-Delivery Systems
Isaac Kantorovich, Senior Hardware Engineer, Intel Victor Drabkin, Senior Hardware Engineer, Intel Chris Houghton, Principal Engineer, Enterprise Platforms Group, Intel Jim St. Laurent, Hardware Engineer, Intel
A-WA2: The Recessed Probe Launch: A New Signal Launch for High Frequency Characterization
of Board-Level Packaging
A-WA3: Hybrid Stripline Analysis II: Propagation Characteristics, Crosstalk Effects, and PCB Routability1046 James Broomall , Signal-Integrity Engineer, W.L. Gore and Associates Tamera Yost , Team Leader, Signal Integrity, W.L. Gore and Associates Glen Walther , Technical Leader, PWB Research and Development Laboratory, W.L. Gore and Associates Gregg Wildes , Smiths Aerospace
A-WP2: Total Jitter Measurement at Low Probability Levels, Using Optimized BERT Scan Method 1061 Marcus Müller, Research and Development Engineer, Agilent Technologies Ransom Stephens, Research Scientist, Teraspeed Consulting Group Russ McHugh, Application Engineer, Agilent Technologies