Electrical Performance of Electronic Packaging

October 23–25, 2006

Radisson Fort McDowell Resort
Scottsdale, Arizona

Sponsored by:

The IEEE Microwave Theory and Techniques Society

and

The IEEE Components, Packaging and Manufacturing Technology Society

Copyright © 2006 by The Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republications permission, write to IEEE Copyrights Manager, IEEE Operations Center, 445 Hoes Lane, Piscataway, New Jersey USA 08854. All rights reserved.

IEEE Catalog Number: 06TH8920

ISBN: 1-4244-0668-4

Library of Congress: 2006933046

Additional Copies of This Publication Are Available from:

IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08854
IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08854
Phone: (800) 678-IEEE
(732) 981-1393
Fax: (732) 981-9667
E-mail: customer-service@ieee.org

TABLE OF CONTENTS

Introduction iii
Technical Program Committee v
John Prince Memoriam vii
Table of Contents ix

Monday, October 23, 2006

Session II – Systems

Designing for Low Power 3
Signal Integrity Impact of Ultra Low Power IO Initiatives 7
Fine Pitch Inductively Coupled Connectors for Multi-Gbps Pulse Signaling 11
Increasing Channel Margin of Distorted Serial Systems 15

Session III – Measurements

Jitter Amplification Characterization of Passive Clock Channels at 6.4 and 9.6 Gb/s 21
On-die Decoupling Capacitor Measurement Using Vector Network Analyzer 25
Dielectric Constant and Loss Tangent Characterization of Thin High-K Dielectrics Using Corner-to-Corner Plane Probing 29
A Method to Measure Impedance of Chip/Package/Board Power Supply System Using Pseudoimpulse Current 33
Measurement of Via Currents in Printed Circuit Board Using Inductive Loops 37

Session IV – Power Distribution

A New Approach to the Design of Power Distribution Networks Containing Electromagnetic Bandgap Structures 43
Switching Noise Suppression in Mixed Signal System Applications Using Electromagnetic Band Gap (EBG) Synthesizer 47
A Low Frequency Hybrid EBG Structure for Power Plane Noise Suppression 51
Analysis of Embedded Package Capacitors for High Performance Components 55
Efficient Modeling of Package Power Delivery Networks with Fringing Fields and Gap Coupling in Mixed Signal Systems 59

Session V – I/O Macromodeling

Guaranteed Locally-Stable Macromodels of Digital Devices via Echo State Networks 65
Developing Improved IO Buffer Behavioral Modeling Methodology Based on IBIS 69
Genetic Algorithms with Scalable I/O Macromodels to Find the Worst Case Corner in High-Speed Server Electrical Analysis 73

Session VI - Open Forum (Posters) Modeling and Simulation

S-parameters Based Transmission Line Modeling with Accurate Low-Frequency Response 79
An Efficient and Flexible Modeling for Power/Ground Planes....83
Power Supply Noise Simulation Considering Dynamic Effect of On-Chip Current....87
Evaluation of Crosstalk in High-Frequency Interconnects with an Enhanced Transmission Line Model 91
Application of an Efficient Full-Wave Simulator UA-FWLIS on Complicated Stripline Structures 95
A Preconditioned Hierarchical Algorithm for Impedance Extraction of Interconnects in Packages....99
Automated Timing and Electrical Analysis of a DDR2 Memory Interface 103
Barnes-Hut Accelerated Capacitance Extraction Via Locally Corrected Nyström Discretization 107
Broadband Rational Modeling via Adaptive Frequency Sampling for Full-Wave Simulation 111
Crosstalk Superposition of Multiple Aggressors in Electronic Package System Pre-PD Signal Integrity Simulations 115
CPU Core Impedance Profile Correlation between Simulations and Measurements....119
Causal Transient Simulation of Systems Characterized by Frequency-Domain Data in a Modified Nodal Analysis Framework....123
On the Effect of Mobile Device Shape Characteristics to Interconnection Noise Coupling to an RF Chip Antenna....127
Broad-Band Characterization of Conductors with Arbitrary Topology Using a Surface Integral Formulation 131

Tuesday, October 24, 2006

Session VIII – On-Chip Interconnect

Multi-Rate Latency Insertion Method for the Fast Transient Simulation of Large Networks with Nonlinear Termination 137
Design of Compact Meander Delay Lines on Si Substrate 141
Transient Signal Distortion in Silicon-Based Interconnects over Thin-Film Metal Ground Layers 145
Analytical Estimation of Interconnect Loss Due to Dummy Fills 149
Simulation, Measurement and Modeling of Orthogonal On-Chip Interconnects 153

Session IX – High Speed Channels

Controlled Inter-Symbol Interference Design Techniques of Conventional Interconnect Systems for Data Rates Beyond 20 Gbps 159
Multiple Edge Responses for Fast and Accurate System Simulations 163
Maximum Tolerable Power Supply Noise for Data-Clock Synchronization 167
Accurate System Voltage and Timing Margin Simulation in CDR Based High Speed Designs 171
Distortion Minimization for Packaging Level Interconnects 175

Session X – Linear Macromodeling

Causality-Constrained Interpolation of Tabulated Frequency Responses 181
A Passive Algorithm for Modeling Frequency-Dependent Parameters of Coupled Interconnects 185
A General Approach for Time-Domain Sensitivity Analysis of High-Speed Interconnects 189
Model Order Reduction with Load Constraints 193

Session XI – Linear Macromodeling II

Delay-Based Macromodels for Long Interconnects via Time-Frequency Decompositions 199
An Efficient Closed Form Macromodeling Algorithm using Method of Characteristics for Lossy Multiconductor Transmission Lines 203
Waveform Relaxation Technique for Longitudinal Partitioning of Transmission Lines 207
Recursive Multi-Parameter Closed-Form Expressions for High-Speed Transmission Line Networks 211

Session XII - Open Forum (Posters) Systems

Design and Performance Analysis of Dual Die Pentium® 4 Package 217
Networks-in-Package; Design, Analysis and Implementation 221
BlueGene/L Hardware as a Springboard to Future Products..225
Interconnects Analyses in Quasi-Monolithic Integration Technology (QMIT) 229
Improving the Radiated Immunity of the Strip-Lines Using a Novel Hybrid EBG Structure..233
Packaging Considerations for a Compact Reconfigurable RF Tuner with a Broadband Tuning Range 237
Eye-Pattern Improvement for Design of High-Speed Differential Links Using Passive Equalization 241
Design of Wideband Impedance Matching for Through-Hole Via Transition Using Ellipse-Shaped Anti-Pad...245
Low-cost, Low-noise Vref Design for High-speed DDR Memory Modules 249
Effect of EBG Structures for Reducing Noise in Multi-Layer PCBs for Digital Systems 253
Common Mode Return Loss Consideration in Wirebond Packaging for High Speed SerDes Links 257
Study of Electrical Performance of Flip-Chip Package Via Designs for Gigahertz Applications...261
Performance Analysis of Edge-based DFE..265
Experimental Evaluation of High-speed Data Transmission in a Waveguide-based Interconnect...269
High-Speed Flex Chip-to-Chip Interconnect 273
Full Characterization of Substrate Integrated Waveguides from *S*-Parameter Measurements 277
Study of PCB Trace Crosstalk in Backplane Connector Pin Field.................................281

Wednesday, October 25, 2006

Session XIII – Special Session

A Framework and Simulator for Parallel Fast Integral Equation Simulation of Microelectronic Structures 287
Large Scale Simulation of an Integrated Circuit Package 291
Modeling Multilayered Packages Using the Parallel Finite Difference Time Domain (PFDTD) Approach 295
Large Scale Signal and Interconnect FDTD Modeling for BGA Package 299
Parallelized Full Package Signal Integrity Analysis Using Spatially Distributed 3D Circuit Models 303
Multi-threaded Adaptive Multigrid Finite Element Method for Package Modeling 307

Session XIV – EM Modeling for TL

A Layered Finite Element Method for High-Frequency Modeling of Large-Scale Three-Dimensional On-Chip Interconnect Structures 313
Frequency-Domain Finite Element Electrodynamic Modeling of Lossy Interconnects from DC to Multi-GHz Frequencies 317
Principles for Physical-Based Gridding of Package Structures 321

Session XV – EM

Full-Circuit Design Optimization of a RF Silicon Integrated Passive Device 327
Novel Capacitance Extraction Method Using Direct Boundary Integral Equation Method and Hierarchical Approach 331
The Use of Fast Integral Equations Solvers for Practical Package and Interconnect Analysis 335
Complex Structures Modeling Using Equivalence Principle Algorithm 339
Generation of Geometrically Parameterized Reduced Order Models for Full Wave Problems 343

Author Index 347