

Seventh International Workshop on
MICROPROCESSOR TEST AND VERIFICATION
MTV 2006

PROCEEDINGS



Seventh International Workshop on
MICROPROCESSOR TEST AND VERIFICATION
MTV 2006

TABLE OF CONTENTS

.....
Preface **vii**
Acknowledgement **viii**
Workshop Organizing Committee **ix**
Program Committee..... **X**
.....

SECTION 1: TEST

Software-Based On-Line Test of Communication Peripherals in Processor-Based Systems
for Automotive Applications..... 3
P. Bernardi, L. Bolzani, A. Manzone, M. Osella, M. Violante, and M. Sonza Reorda

Circuit Profiling Mechanisms for High-Level ATPG 9
Jorge Campos and Hussain Al-Asaad

Functional Test Selection for High Volume Manufacturing..... 15
Vijay Gangaram, Deepa Bhan, and James K. Caldwell

Test Calculation for Logic and Delay Faults in Digital Circuits 20
József Sziray

SECTION 2: VERIFICATION AND TEST GENERATION

Directed Micro-architectural Test Generation for an Industrial Processor: A Case Study..... 33
Heon-Mo Koo, Prabhat Mishra, Jayanta Bhadra, and Magdy Abadir

Advanced SAT-Techniques for Bounded Model Checking of Blackbox Designs..... 37
Marc Herbstritt, Bernd Becker, and Christoph Scholl

Embedded Software Validation: Applying Formal Techniques for Coverage and Test Generation..... 45
Tamarah Arons, Elad Elster, Terry Murphy, and Eli Singerman

Challenges in System on Chip Verification 52
*Noah Bamford, Rekha K Bangalore, Eric Chapman, Hector Chavez,
Rajeev Dasari, Yinfang Lin, and Edgar Jimenez*

SECTION 3: ARCHITECTURAL AND DESIGN ISSUES

Workload Slicing for Characterizing New Features in High
Performance Microprocessors 61
Hassan Al-Sukhni, David Lindberg, James Holt, and Michele Reese

Deep vs. Shallow, Kernel vs. Language – What is Better for Heterogeneous Modeling in SystemC? 68
Hiren D. Patel and Sandeep K. Shukla

Statistical Static Timing Analysis Considering the Impact of Power Supply Noise in VLSI Circuits..... 76
Hyun Sung Kim and D. M. H. Walker

SECTION 4: DESIGN ERROR DEBUG & DIAGNOSIS

| | |
|--|----|
| Debug Support for Scalable System-on-Chip | 83 |
| <i>Jianmin Zhang, Ming Yan, and Sikun Li</i> | |
| Abstraction and Refinement Techniques in Automated Design Debugging | 88 |
| <i>Sean Safarpour and Andreas Veneris</i> | |
| Diagnosing Silicon Failures Based on Functional Test Patterns | 94 |
| <i>Chia-Chih Yen, Ten Lin, Hermes Lin, Kai Yang, Tayung Liu, and Yu-Chin Hsu</i> | |
| AUTHOR INDEX | 99 |