

14th International Conference "Mixed Design of Integrated Circuits & Systems"

**Ciechocinek, Poland
21-23 June 2007**

Volume 1 of 2

IEEE Catalog Number:	07EX1721
ISBN:	83-922632-4-3

Table of Contents

Preface	3
Table of Content	7

General Invited Papers

Characterization at Cryogenic Temperatures of Piezostacks Dedicated to Fast Tuners for SRF Cavities	17
<i>M. FOUAIDY, G. MARTINET, N. HAMMOUDI, F. CHATELET, A. OLIVIER (IPNO, FRANCE)</i>	
Evolution of the Classical Functional Integration Towards a 3D Heterogeneous Functional Integration	23
<i>J.-L. SANCHEZ, A. BOURENNANE, M. BREIL, P. AUSTIN, M. BRUNET, J.P. LAUR (LAAS-CNRS and Univ. Toulouse, FRANCE)</i>	
Modelling of Thin Film Transistors for Circuit Simulation	35
<i>B. INIGUEZ (Univ. Rovira i Virgili, SPAIN), R. PICOS (Univ. Illes Balears, SPAIN), M. ESTRADA, A. CERDEIRA (CINVESTAV, MEXICO), T.A. YTTERDAL (Norwegian Univ. of Science and Techn., NORWAY), W. JACKSON (HP Labs, USA), A. KOUDYMOV, D. VEKSLER, M.S. SHUR (Rensselaer Polytechnic Inst., USA)</i>	
STARC's Semiconductor Design Technology Research Activities and the HiSIM2 Advanced MOSFET Model Project	41
<i>Y. FURUI (STARC, JAPAN), M. MIURA-MATTAUSCH, N. SADACHIKA, M. MIYAKE, T. EZAKI, H.J. MATTAUSCH (Hiroshima Univ., JAPAN), T. OHGURO, T. IIZUKA, R. INAGAKI, N. FUDANUKI (STARC, JAPAN)</i>	
Tradeoffs and Optimization in Analog CMOS Design	47
<i>D.M. BINKLEY (The Univ. of North Carolina at Charlotte, USA)</i>	

Compact Modelling Special Session

A Unified Carrier-based Model for Symmetric Double-gate and Surrounding-gate MOS Transistors	63
<i>J. HE, W. BIAN, Y. TAO, F. LIU, X. ZHANG (Peking Univ., CHINA), W. WU, T. WANG, M. CHAN (Hong Kong Univ. of Science & Techn., HONG KONG)</i>	
Development of MPW Service for Academies Based on ITE Proprietary CMOS Process	69
<i>D. OBRĘBSKI, K. KUCHARSKI, M. GRODNER, A. KOKOSZKA, A. MALINOWSKI, J. LESIŃSKI, D. TOMASZEWSKI, J. MALESIŃSKA (Institute of Electron Techn., POLAND)</i>	
EKV3 Parameter Extraction and Characterization of 90nm RF-CMOS Technology	74
<i>S. YOSHITOMI (Toshiba Corp. Semiconductor Company, JAPAN), A. BAZIGOS (National Tech. Univ. Athens, GREECE), M. BUCHER (Tech. Univ. Crete, GREECE)</i>	
Electrical Characteristics in n- and p-MOSFETs with Slightly Tilted Off-axis (110) Channel	80
<i>H.S. MOMOSE, S. YOSHITOMI, K. KOJIMA, T. OHGURO, Y. TOYOSHIMA (Toshiba Corp. Semiconductor Company, JAPAN), H. ISHIUCHI (Toshiba Corp. Research and Development Center, JAPAN)</i>	
Experiments and Modeling of Dynamic Floating Body Effects in 1T-DRAM Fully Depleted SOI Devices	84
<i>M. BAWEDIN (Univ. Catholique de Louvain, BELGIUM and INPG, FRANCE), S. CRISTOLOVEANU (INPG, FRANCE), V. DESSARD (CISSOID, BELGIUM), D. FLANDRE (Univ. Catholique de Louvain, BELGIUM)</i>	
Model Parameter Extraction for the High Voltage SOI-Process Using BSIMSOI3 Model and ICCAP	89
<i>J. PIECZYŃSKI (Fraunhofer Inst. for Microelectronic Circuits and Systems, GERMANY), T. GNEITING (AdMOS GmbH Advanced Modeling Solutions, GERMANY)</i>	
Structured Design Based on the Inversion Factor Parameter: Case Study of $\Delta\Sigma$ Modulator System	95
<i>D. STEFANOVIC (EPFL, SWITZERLAND), S. PESENTI (Marvell Semiconductor, SWITZERLAND), M. PASTRE, M. KAYAL (EPFL, SWITZERLAND)</i>	

CARE Project Special Session

A Novel Approach for Hardware Implementation of a Detuning Compensation Control System for SC Cavities	105
<i>K. PRZYGODA (Tech. Univ. Lodz, POLAND), R. PAPARELLA (Univ. degli Studi di Milano, ITALY)</i>	
In Situ Measurement of Neutron and Gamma Radiation Exposures During Intercontinental Flights Using Electronic Personal Dosimeter and Bubble Detectors	110
<i>B. MUKHERJEE (Deutsches Elektronen-Synchrotron, GERMANY), D. MAKOWSKI (Tech. Univ. Lodz, POLAND), V. MARES (GSF-National Research Centre, GERMANY), D. RYBKA (Warsaw Univ. of Techn., POLAND), S. SIMROCK (Deutsches Elektronen-Synchrotron, GERMANY)</i>	
Integral Interface - Universal Communication Interface for FPGA-based Projects	115
<i>A. PIOTROWSKI, S. TARNOWSKI, G. JABŁOŃSKI, A. NAPIERALSKI (Tech. Univ. Lodz, POLAND)</i>	
Low-latency Implementation of Coordinate Conversion in Virtex II Pro FPGA	120
<i>G. JABŁOŃSKI, K. PRZYGODA (Tech. Univ. Lodz, POLAND)</i>	
RadTest - Testing Board for the Software Implemented Hardware Fault Tolerance Research	124
<i>A. PIOTROWSKI, D. MAKOWSKI, S. TARNOWSKI, A. NAPIERALSKI (Tech. Univ. Lodz, POLAND)</i>	
Sinusoidal Signal Synthesis from Vector Values with Small Quantity of Samples	129
<i>S. TARNOWSKI, A. PIOTROWSKI, A. NAPIERALSKI (Tech. Univ. Lodz, POLAND)</i>	

Advanced Logic Synthesis with Application to FPGA-based Implementations

Programmable Hardware Implementation Based on Four Walsh Sequences	135
<i>B.J. FALKOWSKI (Nanyang Techn. Univ., SINGAPORE), T. SASAO (Kyushu Inst. of Techn., JAPAN), T. ŁUBA (Warsaw Univ. of Techn., POLAND)</i>	
Logic Synthesis Importance in FPGA-based Designing of Image and Signal Processing Systems	141
<i>P. TOMASZEWICZ, M. NOWICKA (Warsaw Univ. of Techn., POLAND), B.J. FALKOWSKI (Nanyang Techn. Univ., SINGAPORE), T. ŁUBA (Warsaw Univ. of Techn., POLAND)</i>	
Reconfigurable FPGA-based Hardware Accelerator for Embedded DSP	147
<i>G. RUBIN, M. OMIELJANOWICZ, A. PETROVSKY (Białystok Tech. Univ., POLAND)</i>	
Distributed Arithmetic Based Implementation of Fourier Transform Targeted at FPGA Architectures	152
<i>M. RAWSKI, M. WOJTYŃSKI, T. WOJCIECHOWSKI, P. MAJKOWSKI (Warsaw Univ. of Techn., POLAND)</i>	
Synthesis of Control Unit with Modified Microinstructions	157
<i>A. BARKALOV, L. TITARENKO, J. BIEGANOWSKI (Univ. Zielona Góra, POLAND)</i>	

CLEAN Workshop

Static Power Consumption in Nano-CMOS Circuits: Physics and Modelling	163
<i>W. KUŹMICH, E. PIWOWARSKA, A. PFITZNER, D. KASPROWICZ (Warsaw Univ. of Techn., POLAND)</i>	
System Level Optimization of Static Power Consumption in Nano-CMOS Circuits	169
<i>D. HELMS (OFFIS, GERMANY)</i>	
Static Power Reduction in Nano CMOS Circuits through an Adequate Circuit Synthesis	172
<i>L. JÓŹWIAK, D. GAWŁOWSKI, A. ŚLUSARCZYK, A. CHOJNACKI (Eindhoven Univ. of Techn., THE NETHERLANDS)</i>	

1 Design of Integrated Circuits and Microsystems

A 3.4 Gb/s Low Latency 1 bit Input Digital FIR-filter in 0.13 μ m CMOS	181
<i>H. FREDRIKSSON, C. SVENSSON, A. ALVANDPOUR (Linköping Univ., SWEDEN)</i>	

A Continuous MVL Gate Using Pseudo Floating-Gate	185
<i>O. MIRMOTAHARI, J. LOMSDALEN, Y. BERG (Univ. Oslo, NORWAY)</i>	
A Heuristic Approach to System-level Design Problems	189
<i>A. PUŁKA (Silesian Univ. of Techn., POLAND)</i>	
A Kick-back Reduced Comparator for a 4-6-bit 3-GS/s Flash ADC in a 90nm CMOS Process	195
<i>T. SUNDSTRÖM, A. ALVANDPOUR (Linköping Univ., SWEDEN)</i>	
A Low-noise Current Preamplifier in 120nm CMOS Technology	199
<i>H. UHRMANN, H. ZIMMERMANN (Tech. Univ. Wien, AUSTRIA)</i>	
A Low-power Strategy for Delta-Sigma Modulators	203
<i>S. PESENTI, P. CLEMENT (Marvell Semiconductor, SWITZERLAND), D. STEFANOVIC, M. KAYAL (EPFL, SWITZERLAND)</i>	
A Novel Fully-differential Gm-C Filter Structure for Communication Channel Equalizer	209
<i>P. ALIPARAST, A. KHOEI, K. HADIDI (Urmia Univ., IRAN)</i>	
A Simple and Accurate Track-and-Hold Circuit Using Operational Transconductance Amplifier	215
<i>J.-K. SEON, K.-H. NAM, S.-H. KANG, K.-S. BAE, J.-B. KIM (LG Industrial Systems, KOREA)</i>	
Active Suppression of Substrate Noise in CMOS Integrated Circuits	219
<i>G. BLAKIEWICZ (Gdansk Univ. of Techn., POLAND)</i>	
An Undersampling Digital Microphone Utilising Second Order Noise Shaping	225
<i>S. SOELL, B. PORR (Glasgow Univ., UK)</i>	
Analog, Continuous Time, Fully Parallel, Programmable Image Processor Based on Vector Gilbert Multiplier	231
<i>R. DŁUGOSZ (Univ. Neuchatel, SWITZERLAND, Univ. Alberta, CANADA and Poznan Univ. of Techn., POLAND)</i>	
Analysis of Basic Pausable Local Clock Signal Generator	237
<i>A. SOBCZYK, A. ŁUCZYK, W. PLESKACZ (Warsaw Univ. of Techn., POLAND)</i>	
Comparison of Two Pole-Zero Cancellation Circuits for Fast Charge Sensitive Amplifier in CMOS Technology	243
<i>P. GRYBOŚ, P. MAJ, R. SZCZYGIEL (AGH Univ. of Science and Techn., POLAND)</i>	
Compound Current Conveyor with Reduced Current Tracking Error	247
<i>E. ERGUN, M. ULUTAS (Ondokuz Mayıs Univ., TURKEY)</i>	
Current Mode Analog Kohonen's Neural Network	250
<i>T. TALAŚKA (Univ. of Techn. and Life Sciences, POLAND), R. DŁUGOSZ (Univ. Neuchatel, SWITZERLAND, Univ. Alberta, CANADA and Poznan Univ. of Techn., POLAND), R. WOJTYNA (Univ. of Techn. and Life Sciences, POLAND)</i>	
Current-mode LP CMOS Active Filter for Very Low Frequency Applications	256
<i>T. KULEJ (Tech. Univ. Częstochowa, POLAND)</i>	
Design of a Cascoded Operational Amplifier with High Gain	260
<i>B. LIPKA, U. KLEINE (Otto-von-Guericke Univ. Magdeburg, GERMANY)</i>	
Design of CMCU with EOLC and Encoding of Collections of Microoperations	262
<i>A. BARKALOV, M. KOŁOPIEŃCZYK, L. TITARENKO (Univ. Zielona Góra, POLAND)</i>	
Design of Operational Amplifier with Low Power Consumption in 0.35um Technology	266
<i>J. KOLCZYŃSKI (Tech. Univ. Lodz, POLAND)</i>	
Digital Implementation of a Programmable Reconfigurable Fuzzy Automaton for Control Applications	270
<i>A. WIELGUS, M. MACIĄG (Warsaw Univ. of Techn., POLAND)</i>	
FPGA Based Accelerator for Simulated Annealing with Greedy Perturbations	274
<i>M. ŁUKOWIAK (Rochester Inst. of Techn., USA), B. CODY (Kulicke & Soffa Industries, USA)</i>	
Hardware Support for Combined Interval and Floating Point Multiplication	278
<i>A. AMARICAI, M. VLADUTIU, L. PRODAN, M. UDRESCU, O. BONCALO (Politeh. Univ. of Timisoara, ROMANIA)</i>	

Hierarchical Asynchronous Multiplexer for Readout Front-end ASIC for Multi-element Detectors in Medical Imaging	283
<i>R. DŁUGOSZ (Univ. Neuchatel, SWITZERLAND, Univ. Alberta, CANADA and Poznan Univ. of Techn., POLAND), K. INIEWSKI (CMOS Emerging Techn. Inc., CANADA)</i>	
Implementation of Cholesky LL^T -decomposition Algorithm in FPGA-based Rational Fraction Parallel Processor	287
<i>O. MASLENNIKOW, P. RATUSZNIK (Tech. Univ. Koszalin, POLAND), A. SERGIENKO (Nat. Techn. Univ. of Ukraine, UKRAINE)</i>	
Improved Low-power Low-voltage CMOS Comparator for 4-bit Flash ADCs for UWB Applications	293
<i>J. OLIVEIRA, J. GOES, N. PAULINO (UNL Univ., PORTUGAL), J. FERNANDES (INESC-ID, PORTUGAL)</i>	
Integrated Thermo-electro-mechanical Modeling of 3D e-Cubes Structures	297
<i>G. JANCZYK, T. BIENIEK, P. JANUS, A. KOCIUBIŃSKI, P. GRABIEC, J. SZYNKA (Institute of Electron Techn., POLAND), S. REITZ, P. SCHNEIDER, E. KAULFRESH, J. WEBER (Fraunhofer Institute, GERMANY)</i>	
Log-domain Linear SVM Classifier	301
<i>L. FESTILA, R. GROZA, M. CIRLUGEA, A. FAZAKAS (Tech. Univ. Cluj-Napoca, ROMANIA)</i>	
Low Power High Speed Switched Current Comparator	305
<i>Y. SUN, Y. WANG, F. LAI (Harbin Inst. of Techn., CHINA)</i>	
On Hardware Implementation of FlexRay Bus Guardian Module	309
<i>P.M. SZECÓWKA, M.A. ŚWIDERSKI (Wrocław Univ. of Techn., POLAND)</i>	
Optimisation of Laser Scanner Parameters Using Neural Networks	313
<i>M. PODOLSKI (Warsaw Univ. of Techn., POLAND)</i>	
Performance Modelling and Optimisation of RF Circuits Using Support Vector Machines	317
<i>X. REN, T. KAZMIERSKI (Univ. Southampton, UK)</i>	
Pull Down Network Minimization, Based on Equivalent Functions Concept, in DCVS Circuit Design	322
<i>H. MOHTASHAMI, K. NAVI (Shahid Beheshti Univ., IRAN), A. MAHINI (Iran Univ. of Science and Techn., IRAN), M. SHARIFAN (Shahid Beheshti Univ., IRAN)</i>	
Realization of Tunable Periodical Differential Transmission Lines on Silicon	328
<i>S.E. EL RAI, A.H. PAWLIKIEWICZ (ATMEL Corp., USA), D. JÄGER (Univ. Duisburg-Essen, GERMANY), R. TEMPEL (ATMEL Corp., USA)</i>	
RF CMOS or SiGe BiCMOS for RF and Mixed Signal Circuit Design	333
<i>A.H. PAWLIKIEWICZ, S.E. EL RAI (ATMEL Corp., USA)</i>	
Some Practical Aspects of Integrated 2.4GHz Quadrature VCO Design	339
<i>E. KURJATA-PFITZNER, A. SZYMAŃSKI, J. LESIŃSKI (Institute of Electron Techn., POLAND)</i>	
Speed Enhancement and Linearity Analysis for a Rail-to-Rail Input Opamp in 120nm CMOS	344
<i>W.X. YAN, H. ZIMMERMANN (Tech. Univ. Wien, AUSTRIA)</i>	
Superscalar MOVE Architecture for Power-aware Computing	349
<i>A. ŁUCZYK (Warsaw Univ. of Techn., POLAND)</i>	

2 Thermal Issues in Microelectronics

Application of RC Equivalent Networks to Modelling of Nonlinear Thermal Phenomena	357
<i>M. KAMIŃSKI, M. JANICKI, A. NAPIERAŁSKI (Tech. Univ. Lodz, POLAND)</i>	
Convective Cooling Evaluation of Electronic Devices Using Lock-in Thermography	363
<i>T. ŚWIĄT CZAK, B. WIĘCEK, K. TOMALCZYK (Tech. Univ. Lodz, POLAND)</i>	
Correction to Thermal Impedance Measurements Made Under Non-equilibrium Conditions	369
<i>F. MASANA (Tech. Univ. Catalunya, SPAIN)</i>	
Device Level Electrothermal Analysis of Integrated Resistors	375
<i>B. VERMEERSCH, G. DE MEY (Ghent Univ., BELGIUM)</i>	

Effective Supervisors for Predictive Methods of Dynamic Power Management	381
<i>A. GOŁDA, A. KOS (AGH Univ. of Science and Techn., POLAND)</i>	
Optimal Placement of Electronic Devices in Forced Convective Cooling Conditions	387
<i>M. FELCZAK, B. WIĘCEK (Tech. Univ. Lodz, POLAND)</i>	
Parameters Identification of Embedded PTAT Temperature Sensors for CMOS Circuits	392
<i>A. GOŁDA, A. KOS (AGH Univ. of Science and Techn., POLAND)</i>	
Thermal Imaging of Actively Cooled High-power Laser Bars	396
<i>A. KOZŁOWSKA (Institute of Electron Techn., POLAND), M. ZIEGLER, J.W. TOMM (Max Born Inst., GERMANY), R.P. SARZAŁA, W. NAKWASKI (Tech. Univ. Lodz, POLAND)</i>	

3 Analysis and Modelling of ICs and Microsystems

Accuracy of Analytical Evaluation of Interconnection Capacitances in Crossing Buses	403
<i>A. JAROSZ (Institute of Electron Techn., POLAND), A. PFITZNER (Warsaw Univ. of Techn., POLAND)</i>	
Behavioural Modelling and Simulation of Dual Cascaded PLL Based Frequency Synthesizer	407
<i>A.A. TELBA (King Saud Univ., SAUDI ARABIA and Univ. of Bradford, UK), S. MANZOOR QASIM (King Saud Univ., SAUDI ARABIA), J.M. NORAS (Univ. of Bradford, UK), B. ALMASHARY, M.A. EL ELA (King Saud Univ., SAUDI ARABIA)</i>	
Compensation of Calculations Duration on Converters Output Voltage in Digitally Controlled Converters Based on Law of Conservation of Energy - Project "Bumblebee"	412
<i>J. KACZMAREK, A. MAZUREK (Tech. Univ. Koszalin, POLAND)</i>	
Current Distribution Modelling in Electroconductive Textiles	418
<i>J. BANASZCZYK, G. DE MEY, A. SCHWARZ, L. VAN LANGENHOVE (Ghent Univ., BELGIUM)</i>	
Hardware Fault Free Simulation for SoC	424
<i>V. HAHANOV, M. KAMINSKA, W. GHRIBI, A. HAHANOVA (Kharkov National Univ. of Radioel., UKRAINE)</i>	
Investigation of Substrate Noise Coupling and Isolation Characteristics for a 0.35um HV CMOS Technology	429
<i>W. PFLANZL, E. SEEBACHER (austriamicrosystems AG, AUSTRIA)</i>	
Mixed-mode Simulation and Analysis of Digital Single Event Transients in Fast CMOS ICs	433
<i>M. TUROWSKI, A. RAMAN (CFDRC, USA), G. JABŁOŃSKI (Tech. Univ. Lodz, POLAND)</i>	
Modeling and Co-simulation of Integrated Micro- and Nanosystems	439
<i>P. JANUS, T. BIENIEK, A. KOCIUBIŃSKI, P. GRABIEC (Institute of Electron Techn., POLAND), G. SCHRÖPFER (Coventor Sarl, FRANCE)</i>	
Modeling and the Simulator of Digital Circuits in Object-oriented Programming	444
<i>S. SENCZYNA (Silesian Univ. of Techn., POLAND)</i>	
Modeling Power Amplifier Nonlinearities with Artificial Neural Network	449
<i>J. POCHMARA (Poznan Univ. of Techn., POLAND)</i>	
Multi-tool Constraint Verification	454
<i>A. SCHÄFER (Univ. Siegen, GERMANY), J. FREUER (Univ. Oldenburg, GERMANY), K. HAHN (Univ. Siegen, GERMANY), W. NEBEL (Univ. Oldenburg and OFFIS, GERMANY), R. BRÜCK (Univ. Siegen, GERMANY)</i>	
Nonlinear Model of Electrokinetic Phenomena in VHDL-AMS	460
<i>K. ŚLUSARCZYK, A. NAPIERAŁSKI (Tech. Univ. Lodz, POLAND)</i>	
Parameter Extraction for Simplified RF NMOSFET Equivalent Circuit Using SPICE	464
<i>G. ANGELOV, M. HRISTOV, O. ANTONOVA, E. GADJEVA (Tech. Univ. Sofia, BULGARIA)</i>	
System-level Analysis of O-QPSK Transceiver for 2.4-GHz Band IEEE 802.15.4 ZigBee Standard	469
<i>A. EL OUALKADI, L. VANDENDORPE, D. FLANDRE (Univ. Catholique de Louvain, BELGIUM)</i>	

4 Microelectronics Technology and Packaging

- Fabrication of MOS-compatible Ion-sensitive Devices for Water Pollution Monitoring (WARMER) 477
*M. ZABOROWSKI, B. JAROSZEWICZ, D. TOMASZEWSKI, P. PROKARYN (Institute of Electron Techn., POLAND),
E. MALINOWSKA, E. GRYGOŁOWICZ-PAWLAK (Warsaw Univ. of Techn., POLAND), P. GRABIEC (Institute of
Electron Techn., POLAND)*
- Polysiloxane Thin Films Optimisation for Potassium Detection Using EIS Characterisation with
Microelectrode Structures 482
*B. TORBIÉRO, J. LAUNAY, A. BENYAHIA, A. MARTINEZ, P. TEMPLE-BOYER (LAAS-CNRS and Univ.
Toulouse, FRANCE)*

5 Testing and Reliability

- Convolution Blocks Based on Self-checking Operators 487
D. FRANCO, J.-F. NAVINER, L. NAVINER (GET/Telecom Paris, FRANCE)
- CPLD Based Development Board for Mixed Signal Chip Testing 492
*P. ŚNIATAŁA, J. PIERZCHLEWSKI, A. HANDKIEWICZ (Poznan Univ. of Techn., POLAND), B. NOWAKOWSKI (Atrem
Sp. z o.o., POLAND)*
- Crosstalk-insensitive Method for Testing of Delay Faults in Interconnects between Cores in SoCs 496
T. GARBOLINO, K. GUCWA, M. KOPEĆ, A. HŁAWICZKA (Silesian Univ. of Techn., POLAND)
- C-V Characterization of Nonlinear Capacitors Using CBCM Method 501
T. SUTORY, Z. KOLKA (Brno Univ. of Techn., CZECH REPUBLIC)
- Facet Heating Mechanisms in High Power Semiconductor Lasers Investigated by Spatially
Resolved Thermoreflectance 506
*D. PIERŚCIŃSKA, K. PIERŚCIŃSKI, A. KOZŁOWSKA (Institute of Electron Techn., POLAND), A. MALĄG (Inst. of
Electronic Materials Techn., POLAND), A. JASIK, M. BUGAJSKI (Institute of Electron Techn., POLAND)*
- Multi Background Memory Testing 511
S. YARMOLIK (Belarusian State Univ. of Inf. and Radioel., BELARUS), I. MROZEK (Bialystok Tech. Univ., POLAND)
- Novel Step-ramp Signal for Testing ADCs and DACs 517
Y.C. WEN (Cheng Kung Univ., TAIWAN)
- Optimal Excitation in Fault Diagnosis of Analog Electronic Circuits 523
Ł. CHRUSZCZYK, J. RUTKOWSKI, D. GRZETCHCA (Silesian Univ. of Techn., POLAND)
- Random Access Memory Faults Descriptions and Simulation Using VHDL 529
A. IVANIUK (Belarusian State Univ. of Inf. and Radioel., BELARUS)
- Self-adjusting Output Data Compression for RAM with Word Error Detection and Correction 535
*S. MUSIN, A. IVANIUK (Belarusian State Univ. of Inf. and Radioel., BELARUS), V. YARMOLIK (Tech. Univ.
Bialystok, POLAND)*
- Spectral Modification of the LFSR - Sequence for Test Patterns Generation Improvement 539
P. PORWIK, K. WRÓBEL (Univ. of Silesia, POLAND)
- The Influence of Defect Distribution Function Parameters on Test Patterns Generation 545
M. RAKOWSKI, W. PLESKACZ, P. BORKOWSKI (Warsaw Univ. of Techn., POLAND)

6 Power Electronics

- Application of Advanced Thermal Analysis Method for Investigation of Internal Package Structure 553
*J. BANASZCZYK (Ghent Univ., BELGIUM), M. JANICKI (Tech. Univ. Lodz, POLAND), B. VERMEERSCH, G. DE
MEY (Ghent Univ., BELGIUM), A. NAPIERAŁSKI (Tech. Univ. Lodz, POLAND)*

CMOS Dual-channel 0.5A Power Switch for Power Distribution via USB Port	559
<i>V. NAGY, V. STOPJAKOVÁ, J. BRENKUŠ, M. ŠIMLAŠTÍK, M. KONFAL (Slovak Univ. of Techn., SLOVAKIA)</i>	
Comparison of Classic DC/DC Converters with Converters Equipped with Analog-Digital Regulator Based on Law of Conservation of Energy (Bumblebee Type)	564
<i>J. KACZMAREK, A. MAZUREK (Tech. Univ. Koszalin, POLAND)</i>	
Configurable High Side Power Switch in Smart Power Technology	570
<i>P. DEL CROCE, J. HADZI VUKOVIC, B. MELDT, M. LADURNER (Infineon, AUSTRIA)</i>	
Design of an Integrated Self-switching Mode Device for Power Converters	574
<i>F. CAPY, A. BOURENNANE, M. BREIL (LAAS-CNRS, FRANCE), F. RICHARDEAU (LAPLACE, FRANCE), E. IMBERNON, J.-L. SANCHEZ, J.P. LAUR, P. AUSTIN (LAAS-CNRS, FRANCE)</i>	
Improving Measuring Procedures in DC-DC Converters	580
<i>M. CIRLUGEA, V. POPESCU, L. FESTILA, R. GROZA (Tech. Univ. Cluj-Napoca, ROMANIA)</i>	
New Concept of DC/DC Converters Digital Control Based on Law of Conservation of Energy - Project "Bumblebee"	586
<i>J. KACZMAREK, A. MAZUREK (Tech. Univ. Koszalin, POLAND)</i>	
Piezoelectric Transformer Efficiency Tests in a Digitally Controlled Converter Circuit	592
<i>K. TOMALCZYK, T. ŚWIĄT CZAK, B. WIĘCEK (Tech. Univ. Lodz, POLAND)</i>	
The Electrothermal Analysis of a Switched Mode Voltage Regulator	597
<i>K. GÓRECKI, J. ZARĘBSKI (Gdynia Maritime Univ., POLAND)</i>	

7 Signal Processing

An FPGA Implementation of the Distributed Arithmetic Based Quaternionic Multipliers for Paraunitary Filter Banks	605
<i>A. VERENIK (Belarusian State Univ. of Inf. and Radioel., BELARUS), M. PARFIENIUK, A. PETROVSKY (Białystok Tech. Univ., POLAND)</i>	
Application Specific VLIW Processors with Power-saving Mode via Variable Arithmetic Accuracy	611
<i>P. PAWŁOWSKI, A. DĄBROWSKI (Poznan Univ. of Techn., POLAND)</i>	
Aura Removal Algorithm for High-temperature Image Quantitative Analysis Systems	617
<i>A. FABIAŃSKA, D. SANKOWSKI (Tech. Univ. Lodz, POLAND)</i>	
Eyelids Localization Method Designed for Iris Recognition System	622
<i>W. SANKOWSKI, K. GRABOWSKI, M. NAPIERALSKA, M. ZUBERT (Tech. Univ. Lodz, POLAND)</i>	
Focus Assessment Issues in Iris Image Acquisition System	628
<i>K. GRABOWSKI, W. SANKOWSKI, M. ZUBERT, M. NAPIERALSKA (Tech. Univ. Lodz, POLAND)</i>	
Initial Version of FPGA-Based CRAINOT Function Generator	632
<i>G. VALTERS, P. MISANS (Riga Tech. Univ., LATVIA)</i>	
Low Input Impedance Current-mode Allpass and Notch Filter Employing Single Current Follower	638
<i>E. ERGUN, M. ULUTAS (Ondokuz Mayıs Univ., TURKEY)</i>	
Low Voltage Low Frequency Continuous Time CMOS Antialiasing Filters	641
<i>W. MACHOWSKI, J. JASIELSKI, S. KUTA (AGH Univ. of Science and Techn., POLAND)</i>	
New Features Extraction Method for People Recognition on the Basis of the Iris Pattern	645
<i>R. SZEWCZYK (Tech. Univ. Lodz, POLAND)</i>	
Wavelet Processing Implementation in Digital Hardware	651
<i>P.M. SZECÓWKA, M. KOWALSKI, K. KRYSZTOFORSKI, A.R. WOŁCZOWSKI (Wrocław Univ. of Techn., POLAND)</i>	

8 Embedded Systems

A Coloured Petri Net Based Solution for the Generalized Railway Crossing Problem	657
<i>M. PIOTROWICZ, K. ŚLUSARCZYK, A. NAPIERALSKI (Tech. Univ. Lodz, POLAND)</i>	

Hardware-Software Codesign of a Fingerprint Alignment Processor	661
<i>M. FONS, F. FONS, E. CANTÓ (Univ. Rovira i Virgili, SPAIN)</i>	
Knowledge-based Control of Reactive Systems with Multi-layer Architecture	667
<i>P. MATYASIK, G.J. NALEPA (AGH Univ. of Science and Techn., POLAND)</i>	
NnEP, Design Pattern for Neural-network-based Embedded Systems	673
<i>H. ESMAEILZADEH, M.R. JAMALI, P. SAEEDI, A. MOGHIMI, C. LUCAS, S.M. FAKHRAIE (Univ. Tehran, IRAN)</i>	
The Architecture of Communication Channel for Custom Computing Machine Node	679
<i>R. KAPELA (Poznan Univ. of Techn., POLAND), B. NOWAKOWSKI (Atrem Sp. z o.o., POLAND), A. RYBARCZYK (Poznan Univ. of Techn., POLAND)</i>	
Translator of Hierarchical State Machine from UML Statechart to the Event Processor Pattern	684
<i>P. ROMANIUK (Tech. Univ. Lodz, POLAND)</i>	
XCCS - Graphical Extension of CCS Language	688
<i>M. SZPYRKA (AGH Univ. of Science and Techn., POLAND), K. BALICKI (Rzeszów Univ., POLAND)</i>	

9 Information Technology

General Purpose Lightweight Content Management System	697
<i>M. JASKÓLSKI, B. SAKOWICZ, A. NAPIERALSKI (Tech. Univ. Lodz, POLAND)</i>	
JWay - Model-driven J2EE Application Framework	703
<i>B. SAKOWICZ, J. MURLEWSKI, A. LABUS, A. NAPIERALSKI (Tech. Univ. Lodz, POLAND)</i>	
Query Optimization in Grid Databases	707
<i>J. MURLEWSKI, T. KOWALSKI, R. ADAMUS, B. SAKOWICZ, A. NAPIERALSKI (Tech. Univ. Lodz, POLAND)</i>	