

# 2007 22<sup>nd</sup> IEEE Non-Volatile Semiconductor Memory Workshop

Proceedings

August 26<sup>th</sup> – 30<sup>th</sup>, 2007  
Monterey, California



## TABLE OF CONTENTS

---

<b>NVSMW Conference Schedule/Program</b>		<b>vi</b>
<b>Map of Hotel and Conference Facilities</b>		<b>viii</b>
<b>Session #1</b>	<hr/>	<b>1</b>
T. Siegel	"Non Volatile Memory in Automotive Application, Expectations, Best Practices"	Not Available for Publication
R. Schuetz	"HyperLink NAND Flash Architecture for Mass Storage Applications"	3
K. Prall	"Scaling Non-Volatile Memory Below 30nm"	5
P. Nicosia	"Test Strategies on Non Volatile Memories - Electrical Wafer Sort on NAND, NOR Flash and Phase Change Memories"	11
J.K. Kim	"Low Stress Program and Single Wordline Erase Schemes for NAND Flash Memory"	19
H. Pon	"A NAND Flash PC Platform Read Write Cache"	21
M. Mihara	"A 1.8V 4Mb Floating-Gate NOR Type B4-Flash Test Chip for 100MB/s Programming Speed"	23
<b>Session #2</b>	<hr/>	<b>25</b>
J.R. Power	"Improved Reliability of a High-k IPD Flash Cell through use of a Top-oxide"	27
S. Shukuri	"Floating Gate B4-Flash Memory Technology Utilizing Novel Programming Scheme- Highly Scalable, Efficient and Temperature Independent Programming -"	30
K.J. Han	"A Novel Flash-based FPGA Technology with Deep Trench Isolation"	32
J. Sarkar	"Protein-Mediated Assembly of Nanocrystal Floating Gate in a Vertical Flash Cell"	34
A. Niebel	<b>"Panel Discussion</b> - How to Overcome the Performance and Reliability Limitations of >2 bits/cell as we Continue Scaling the Technology"	
<b>Session #3</b>	<hr/>	<b>37</b>
D. Oh	"A New Self-Boosting Phenomenon by Source/Drain Depletion Cut-off in NAND Flash Memory"	39
L. Perniola	"In Depth Analysis of Channel Length, Fin Width (down to 10 nm) Impacts on Fowler-Nordheim Program/Erase Characteristics of Si-NC SOI FinFlash Memories"	42
C. Gerardi	"Highly manufacturable/low aspect ratio Si Nano Floating Gate FinFET memories: High Speed Performances and Improved Reliability"	44
L. Breuil	"Nitride Based FinFLASH Memory Device Using Multilevel Hot Carrier Program/Erase"	46
C.E. Huang	"A New CMOS Logic Anti-Fuse Cell with Programmable Contact"	48

## TABLE OF CONTENTS

M.H. Hsueh	"A Novel Self-aligned Si-wire Flash Memory Featuring Multi-bit/cell Operation, Fast Edge +FN Erase, and Over-erasure Immunity"	52
S. Kim	"Air-Gap Application and Simulation Results for Low Capacitance in 60nm NAND Flash Memory"	54
I. Karpov	"Mechanism of Threshold Switching in Chalcogenide Phase Change Memory Devices"	56
<b>Session #4</b>	<hr/>	59
Y.Y. Lin	"Nano-Crystalline Phase Change Memory with Composite Si-Sb-Te Film for better Data Retention and Lower Operation Current"	61
H. Tanizaki	"A 1Mb High-Density Toggle-MRAM with Symmetrical Read/Write Operations"	63
K. Kinoshita	"Reduction of Reset Current in NiO-ReRAM brought about by Ideal Current Limiter"	66
S. Karg	"Nanoscale Resistive Memory Device Using SrTiO <sub>3</sub> Films"	68
S. Jacob	"Investigation of Reliability Characteristics of Si Nanocrystal NOR Memory Arrays"	71
H. Choi	"Hybrid Charge Trap Memory Device with TaN Nanocrystals Formed by Phase Separation Methods"	73
C.M. Hong	"Reliability Study of Split Gate Silicon Nanocrystal Flash EEPROM"	75
J. Yater	"Optimization of 90nm Split Gate Nanocrystal Non-Volatile Memory"	77
<b>Session #5</b>	<hr/>	79
Y.W. Chang	"A New Interference Phenomenon in Sub-60nm Nitride-Based Flash Memory"	81
E.S. Choi	"Modeling and Characterization of Program / Erasure Speed and Retention of TiN-gate MANOS (Si-Oxide-SiN <sub>x</sub> -Al <sub>2</sub> O <sub>3</sub> -Metal Gate) Cells for NAND Flash Memory"	83
Y. Okuyama	"Determination of Lateral Charge Distributions of Split-gate SONOS Memories Using Experimental Devices with Nanometer-size Nitride Piece"	85
S.C. Lai	"MA BE-SONOS: A Bandgap Engineered SONOS Using Metal Gate and Al <sub>2</sub> O <sub>3</sub> Blocking Layer to Overcome Erase Saturation"	88
N. Takahashi	"Nitride Trapping Memory Technology to Realize Flash-Embedded SoC of 65nm and Beyond"	90
N. Akil	"New Punch-through Assisted Hot Holes Programming Mechanism for Reliable SONOS FLASH Memories with Thick Tunnel Oxide"	92
A. Furnémonta	"Physical Understanding of SANOS Disturbs and VARIOT Engineered Barrier as a Solution"	94
A. Furnémonta	"A Consistent Model for the SANOS Programming Operation"	96

## TABLE OF CONTENTS

<b>Session #6</b>		99
S.H. Lee	"Improved Bake Retention Characteristic of Recessed Charge Trap Flash (RCTF)"	101
S. Shim	"Low Voltage High Speed Programming/Erasing Charge Trapping Memory with Metal-Al <sub>2</sub> O <sub>3</sub> -Si <sub>3</sub> N <sub>4</sub> - Si Structure"	103
G. Kathawala	"Novel Application of Monte Carlo Simulations for Improved Understanding of Transient Programming in SONOS Devices"	106
J.S. Sim	"Self Aligned Trap-Shallow Trench Isolation Scheme for the Reliability of TANOS (TaN/AIO/SiN/Oxide/Si) NAND Flash Memory"	110
	Author Index	Follows page 112