

2007 International Symposium on Power Semiconductor Devices & IC's

**Jeju, Korea
27-31 May 2007**



IEEE Catalog Number:
ISBN 10:
ISBN 13:

CFP07ISP-PRT
1-4244-1095-9
978-1-4244-1095-8

TECHNICAL SESSIONS

Monday, May 28, 2007

Session 1 Plenary

Chairs

- Min-Koo Han (Seoul National University, Korea)
 Tat-Sing Paul Chow (Rensselaer Polytechnic Institute, USA)
- P1-1 Izak Bencuya (Executive Vice President)
 Fairchild Semiconductor, USA
- P1-2 Kaushik Rajashekara (Senior Technologist)
 Rolls Royce Corporation, UK
- P1-3 Soo Young Oh (Vice President and Director)
 IT Convergence & Component Laboratory, ETRI, Korea

Session 2 Si IGBTs - I

Chairs

- Yasukazu Seki (Fuji Electric Holdings, Japan)
 Stefan Linder (ABB, Switzerland)
- O2-1 **Long Term Stability and Drift Phenomena of different Trench IGBT Structures under Repetitive Switching Tests** 1
 T. Laska, F. Hille, F. Pfirsch, R. Jereb, and M. Bässler
 Infineon Technologies, Neubiberg, Germany
- O2-2 **Investigations on 6.5kV Trench IGBT and adapted EmCon Diode** 5
 J.G. Bauer¹, T. Duetemeyer², E. Falck¹, C. Schaeffer³, G. Schmidt³, and H. Schulze³
¹Infineon Technologies, Neubiberg, Germany
²Infineon Technologies, Warstein, Germany
³Infineon Technologies, Austria
- O2-3 **1200V IGBTs operating at 200°C? An investigation on the potentials and the design constraints** 9
 U. Schlapbach, M. Rahimo, C. von Arx, A. Mukhitdinov, and S. Linder
 ABB, Lenzburg, Switzerland

Session 3 Si IGBTs - II

Chairs

- Akio Nakagawa (Toshiba, Japan)
 Hsueh-Rong Chang (International Rectifier, USA)
- O3-1 **Development of the next generation 1200V trench-gate FS-IGBT featuring lower EMI noise and lower switching loss** 13
 Y. Onozawa¹, H. Nakano¹, M. Otsuki¹, K. Yoshikawa², T. Miyasaka¹, and Y. Seki³
¹Fuji Electric Device Technology, Japan
²Fuji Electric Advanced Technology, Japan
³Fuji Electric Holdings, Japan
- O3-2 **A 800 V Hybrid IGBT Having a High-Speed Internal Diode for Power-Supply Applications** 17
 S. Kaneko, H. Yamagiwa, T. Saji, T. Uno, and K. Sawada
 Matsushita Electric Industrial, Japan

-
- O3-3 **An Ultrafast and Latch-Up Free Lateral IGBT with Hole Diverter for Junction-Isolated Technologies** 21
 B. Bakeroot¹, J. Doutreloigne¹, P. Vanmeerbeek², and P. Moens²
¹Ghent University, ELIS-TFCG/IMEC, Belgium
²AMI Semiconductor BVBA, Belgium

Session 4 Super Junction Devices, Thyristors and Measurement Technology

Chairs

- Shankar Ekkanath Madathil (De Montfort University, UK)
 Chong-Man Yun (Fairchild Korea Semiconductor, Korea)
- O4-1 **Design concept of n-buffer layer (n-Bottom Assist Layer) for 600V-class Semi-Super Junction MOSFET** 25
 S. Ono, W. Saito, M. Takashita, S. Kurushima, K. Tokano, and M. Yamaguchi
 Toshiba Corporation Semiconductor, Japan
- O4-2 **The Corrugated P-Base IGCT – a New Benchmark for Large Area SOA Scaling** 29
 T. Wikström¹, T. Stiasny¹, M. Rahimo¹, D. Cottet², and P. Streit¹
¹ABB, Lenzburg, Switzerland
²ABB, Dättwil, Switzerland
- O4-3 **Depth-Resolved Temperature Measurements on Power Devices under Transient Conditions** 33
 X. Perpiñà^{1,2}, X. Jordà¹, M. Vellvehi¹, M. Mermet-Guyennet², J. Millán¹, and N. Mestres³
¹CNM-CSIC, Spain
²ALSTOM, France
³CMAB-CSIC, Spain
- O4-4 **200V Trench Filling Type Super Junction MOSFET with Orthogonal Gate Structure** 37
 T. Shibata¹, Y. Noda¹, S. Yamauchi¹, S. Nogami², T. Yamaoka², Y. Hattori³, and H. Yamaguchi¹
¹DENSO, Japan
²SUMCO, Japan
³Toyota Central R&D Labs., Japan

Tuesday, May 29, 2007

Session 5 Applications

Chairs

- Alex Q. Huang (North Carolina State University, USA)
 Z. John Shen (University of Central Florida, USA)
- O5-1 **ACTIVE CONTROL OF THE TRIGGERING CHARACTERISTICS OF NPN BJT, BSCR AND NLD MOS-SCR DEVICES** 41
 V.A. Vashchenko, D. Farrenkopf, and P. Hopper
 National Semiconductor, USA

O5-2	Demonstration of high frequency and 10A operation in 12V 1 chip DC/DC converter IC using bump technology	45
	K. Nakamura, K. Matsushita, T. Naka, Y. Ikeda, N. Yasuhara, K. Endo, F. Suzuki, M. Takahashi, M. Yamaguchi, and A. Nakagawa Toshiba Corporation Semiconductor, Japan	
O5-3	Low Parasitic Current 'Half ON' Operation of Battery Protection IC	49
	S. Matsunaga, M. Sawada, M. Sugimoto, and N. Fujishima Fuji Electric Advanced Technology, Japan	
O5-4	Compact Double-Side Liquid-Impingement-Cooled Integrated Power Electronic Module	53
	C.M. Johnson ¹ , C. Buttay ¹ , S.J. Rashid ² , F. Udrea ² , G.A.J. Amaratunga, ² P. Ireland ³ , and R.K. Malhan ⁴ ¹ University of Nottingham, UK ² University of Cambridge, UK ³ Oxford University, UK ⁴ DENSO, Japan	

Session 6 Low Voltage Si MOS

Chairs

	Philip Hower (Texas Instruments, USA)	
	Wai Tung Ng (University of Toronto, Canada)	
O6-1	Record-low on-Resistance for 0.35 μ m based integrated XtremOSTM Transistors	57
	P. Moens ¹ , F. Bauwens ¹ , B. Desoete ¹ , J. Baele ¹ , K. Vershinin ² , H. Ziad ² , E.M.S. Narayanan ² , and M. Tack ¹ ¹ AMI Semiconductor BVBA, Belgium ² De Montfort University, UK	
O6-2	Split-gate Resurf Stepped Oxide (RSO) MOSFETs for 25V applications with record low gate-to-drain charge	61
	P. Goarin ¹ , G.E.J. Koops ¹ , R. van Dalen ¹ , C.L. Cam ² , and J. Saby ³ ¹ NXP Semiconductors, Belgium ² NXP Semiconductors, France ³ INSA, France	
O6-3	Anomalous temperature behavior in LDMOS current sensing	65
	J. Lin ¹ , S. Pendharkar ² , P. Hower ¹ , J. Arch ² , T. Chatterjee ² , K. Chen ² , J. Devore ² , B. Hu ² , J. Trogolo ² , and Q. Wang ² ¹ Texas Instruments, NH, USA ² Texas Instruments, TX, USA	

Session 7 Integration Technology

Chairs

	Johnny. K. O. Sin (Hong Kong University of Science and Technology, China)	
	Oh-Kyong Kwon (Hanyang University, Korea)	
07-1	Trench-Isolated High-Voltage IC with Reduced Parasitic Bipolar Transistor Action	69
	T. Takahashi, T. Terashima, and J. Moritani Mitsubishi Electric, Japan	

07-2	BCD8 from 7V to 70V: a new 0.18μ m Technology Platform to Address the Evolution of Applications towards Smart Power ICs with High Logic Contents D. Riccardi, A. Causio, I. Filippi, A. Paleari, L.V.A. Pregolato, P. Galbiati, and C. Contiero STMicroelectronics, Italy	73
07-3	Ultra-flexible, layout-enabled field plates for HV transistor integration in SOI-based CMOS J. Šonský, and A. Heringa NXP Semiconductors, Belgium	77
07-4	Local buried oxide technology for HV transistors integrated in CMOS E. Saarnilehto, J. Šonský, P. Meunier-Beillard, and F. Neuilly NXP Semiconductors, Belgium	81

Session 8 Poster Papers

Chairs		
	Peter Moens (AMI Semiconductor BVBA, Belgium)	
	Yeom-Ik Choi (Ajou University, Korea)	
P8-1	8 kV Normally-off All-SiC Cascode Power Switch Using VJFETs E.J. Stewart ¹ , M.J. McCoy ¹ , T.R. McNutt ¹ , H.C. Hearne ¹ , A.P. Walker ¹ , S.D.V. Campen ¹ , G.M. Bates ¹ , S. Leslie ² , G.C. DeSalvo ¹ , and R.C. Clarke ¹ ¹ Northrop Grumman Science and Technology Center, USA ² Powerex, USA	85
P8-2	600V Reverse Conducting (RC-)IGBT for Drives Applications in Ultra-Thin Wafer Technology H. R�thing, F. Hille, F.-J. Niedernostheide, H.-J. Schulze, and B. Brunner Infineon Technologies, Neubiberg, Germany	89
P8-3	Buried Gate Static Induction Transistors in 4H-SiC (SiC-BGSITs) with Ultra Low On-Resistance Y. Tanaka ¹ , K. Yano ² , M. Okamoto ¹ , A. Takatsuka ¹ , K. Arai ¹ , and T. Yatsuo ¹ ¹ National Institute of Advanced Industrial Science and Technology, Japan ² Yamanashi University, Japan	93
P8-4	10kV 4H-SiC PiN Diodes Designed for Improved Switching Performance using Emitter Injection Control P.A. Losee ¹ , C. Li ¹ , Y. Wang ¹ , S.K. Sharma ¹ , T.P. Chow ¹ , I.B. Bhat ¹ , R.E. Stahlbush ² , and R.J. Gutmann ¹ ¹ Rensselaer Polytechnic Institute, USA. ² Naval Research Laboratory, USA.	97
P8-5	Optimisation of SuperJunction Bipolar Transistor for ultra-fast switching applications M. Antoniou ¹ , F. Udrea ¹ , and F. Bauer ² ¹ University of Cambridge, UK ² ABB, D�ttwil, Switzerland	101
P8-6	600V / 100A Broad-Buffer Diode M. Nemoto, and H. Nakazawa Fuji Electric Advanced Technology, Japan	105

P8-7	1200V Emcon4 freewheeling diode – a soft alternative F. Hille, M. Bässler, H.-J. Schulze, E. Falck, H.P. Felsl, A. Schieber, and A. Mauder Infineon Technologies, Neubiberg, Germany	109
P8-8	Investigation of Gate Oscillation of Power MOSFETs Induced by Avalanche Mode Operation S.-C. Lee, K.-H. Oh, H.-C. Jang, J.-G. Lee, S.-S. Kim, and C.-M. Yun Fairchild Semiconductor, Korea	113
P8-9	Discrete and Half Bridge Module using GaN HFETs for High Temperature Applications more than 200°C T. Nomura ¹ , M. Masuda ¹ , S. Yoshida ¹ , T. Yamate ² , Y. Sudo ² , and J. Takeda ² ¹ Furukawa Electric, Japan ² Schlumberger K.K., Japan	117
P8-10	Analysis of Operational Degradation of SiC BJT Characteristics Y. Gao ¹ , A. Q. Huang ¹ , Q. Zhang ² , S. Krishnaswami ² , and A. Agarwal ² ¹ North Carolina State University, USA ² Cree, USA	121
P8-11	Advanced Power SiP with Wireless Bonding for Voltage Regulators T. Hashimoto ¹ , T. Uno ² , Y. Satou ² , M. Shiraishi ¹ , T. Kawashima ¹ , and N. Matsuura ² ¹ Hitachi Research Laboratory, Hitachi, Japan ² Renesas Technology, Japan	125
P8-12	Hot-Carrier-Stress-Induced Degradation of 1 kV AlGaIn/GaN HEMTs by Employing SiO₂ Passivation M.-W. Ha ¹ , Y.-H. Choi ¹ , J.-H. Park ¹ , J.-Y. Lim ¹ , S.-S. Kim ² , C.-M. Yun ² , and M.-K. Han ¹ ¹ Seoul National University, Korea ² Fairchild Semiconductor, Korea	129
P8-13	Integrated Compact Modelling of a Planar-Gate Non-Punch-Through 3.3kV-1200A IGBT Module for Insightful Analysis and Realistic Interpretation of the Failure Mechanisms A. Castellazzi ¹ , M. Ciappa ¹ , W. Fichtner ¹ , J. Urresti-Ibañez ² , and M. Mermet-Guyennet ² ¹ ETH, Switzerland ² ALSTOM, France	133
P8-14	New Measurement Method of T_j of SiCGT and Its Application to a High Voltage Inverter Operating at greater than 300°C K. Asano, Y. Sugawara, A. Tanaka, Y. Miyanagi, S. Okada, S. Ogata, T. Izumi, and K. Nakayama Kansai Electric Power, Japan	137
P8-15	A diode structure with anode side buried p doped layers for damping of dynamic avalanche M. Chen ¹ , J. Lutz ¹ , H.P. Felsl ² , and H.-J. Schulze ² ¹ Chemnitz University of Technology, Germany ² Infineon Technologies, Munich, Germany	141

P8-16	A New Soft Self-Clamping Scheme for Improving the Self-Clamped Inductive Switching (SCIS) Capability of Automotive Ignition IGBT I.-H. Ji ¹ , Y.-H. Choi ¹ , K.-H. Cho ¹ , K.-H. Oh ² , S.-S. Kim ² , C.-M. Yun ² , and M.-K. Han ¹ ¹ Seoul National University, Korea ² Fairchild Semiconductor, Korea	145
P8-17	Dependence of Electrical Properties of Super Junction Diode on Voids within Trench-refill Region M. Kitada, S. Kunori, and T. Kurosaki Shindengen Electric, Japan	149
P8-18	Influence of the base contact on the electrical characteristics of SiC BJTs H.-S. Lee ¹ , M. Domeij ¹ , C.-M. Zetterling ¹ , M. Östling ¹ , B. Heinze ² , and J. Lutz ² ¹ KTH Royal Institute of Technology, Sweden ² Chemnitz University of Technology, Germany	153
P8-19	Induction heating system operation by soft switching GaN heterojunction field effect transistors Y. Niiyama, M. Masuda, N. Ikeda, and S. Yoshida Furukawa Electric, Japan	157
P8-20	RC-TCIGBT: A Reverse Conducting Trench Clustered IGBT D. Kumar, M. Sweet, K. Vershinin, L. Ngwendson, and E.M.S. Narayanan De Montfort University, UK	161
P8-21	Unified Approach in Electro-Thermal Modelling of IGBTs and Power PiN Diodes N. Jankovic ¹ , T. Ueta ² , K. Hamada ² , T. Nishijima ² , and P. Igie ³ ¹ University of Nis, Serbia ² Toyota Motor, Japan ³ University of Wales Swansea, UK	165
P8-22	Circuit Breaker and Safe Controlled Power Switch B. Rosensaft ¹ , U.R. Vemulapati ² , and D. Silber ² ¹ TU-Braunschweig, Germany ² University of Bremen, Germany	169
P8-23	THE INFLUENCE OF NBL LAYOUT AND LOCOS SPACE ON COMPONENT ESD AND SYSTEM LEVEL ESD FOR HV-LDMOS J.-H. Lee, S.H. Chen, Y.T. Tsai, D.B. Lee, F.H. Chen, W.C. Liu, C.M. Chung, S.L. Hsu, J.R. Shih, A.Y. Liang, and K. Wu Taiwan Semiconductor Manufacturing Company, Taiwan	173
P8-24	Superjunction Power LDMOS on Partial SOI Platform Yu Chen ¹ , K. D. Buddharaju ² , Y.C. Liang ¹ , G.S. Samudra ¹ , and H.H. Feng ² ¹ National University of Singapore, Singapore ² Institute of Microelectronics, Singapore	177
P8-25	A 70V UMOS Technology with Trenched LOCOS Process to Reduce Cgs H. Wang ¹ , O. Trescases ¹ , H.P.E. Xu ¹ , W.T. Ng ¹ , K. Fukumoto ² , A. Ishikawa ² , Y. Furukawa ² , H. Imai ² , T. Naito ² , N. Sato ² , K. Sakai ² , S. Tamura ² , and K. Takasuka ² ¹ University of Toronto, Canada ² Asahi Kasei Microsystems, Japan	181

P8-26	Engineering RESURF LDMOSFETs for Robust SOA, ESD Protection and Energy Capability	185
	R. Zhu, V. Khemka, and A. Bose Freescale Semiconductor, USA	
P8-27	Impact of Deep Sub-Micron Design Rules on Optimization of RESURF LDMOSFETs	189
	V. Khemka, R. Zhu, T. Khan, and A. Bose Freescale Semiconductor, USA	
P8-28	The Concept of a Regenerative Diode	193
	U.R. Vemulapati ¹ , D. Silber ¹ , and B. Rosensaft ² ¹ University of Bremen, Germany ² TU-Braunschweig, Germany	
P8-29	Advanced Floating Island and Thick Bottom Oxide Trench Gate MOSFET (FITMOS) with reduced RonA during AC operation by passive hole gate and improved BVdss RonA trade-off by elliptical floating island	197
	H. Takaya, K. Miyagi, and K. Hamada Toyota Motor, Japan	
P8-30	High Voltage LDMOS Transistors utilizing a Triple Well Architecture	201
	H. Puchner, S. Lee, L. Hinh, and J. Jang Cypress Semiconductor, USA	
P8-31	Sub-micron Cell Pitch 30 V N-channel UMOFET with Ultra Low On-resistance	205
	K. Kobayashi, A. Kaneko, Y. Murase, and H. Yamamoto NEC Electronics, Japan	
P8-32	First 15V complementary LDMOS transistors in thin SOI 65nm low power technology	209
	O. Bon ^{1,2} , O. Gonnard ¹ , F. Gianesello ¹ , C. Raynaud ^{1,3} , and F. Morancho ² ¹ STMicroelectronics, France ² Universite de Toulouse, France ³ CEA-LETI, France	
P8-33	A Multiple Deep Trench Isolation Structure with Voltage Divider Biasing	213
	B. Desoete, A. De Smet, and P. Moens AMI Semiconductor BVBA, Belgium	
P8-34	A Normally-off SiC-JFET inverter with low- voltage control and a high-speed drive circuit	217
	K. Ishikawa ¹ , H. Onose ² , Y. Onose ² , T. Ooyanagi ² , T. Someya ² , N. Yokoyama ² , and H. Hozouji ³ ¹ Advanced Research Laboratory, Hitachi, Japan ² Central Research Laboratory, Hitachi, Japan ³ Hitachi Research Laboratory, Hitachi, Japan	
P8-35	Reverse Conducting Double Gate Lateral Insulated Gate Bipolar Transistor in SOI Based Technology	221
	F. Udrea, U.N.K. Udugampola, T. Trajkovic, and G.A.J. Amaratunga Cambridge Semiconductor, UK	
P8-36	Configuration of JI-LIGBT for Over 100 kHz Switching	225
	T. Terashima, and J. Moritani Mitsubishi Electric, Japan	

P8-37	250V-Class Lateral SOI Devices for Driving HDTV PDPs	229
	H. Sumida, K. Maiguma, N. Shimizu, and H. Kobayashi Fuji Electric Device Technology, Japan	
P8-38	250V Integrable Silicon Lateral Trench Power MOSFETs with Superior Specific On-Resistance	233
	K.R. Varadarajan ¹ , T.P. Chow ¹ , J. Wang ¹ , R. Liu ² , and F. Gonzalez ² ¹ Rensselaer Polytechnic Institute, USA ² Supertex, USA	
P8-39	A18 – a novel 0.18μ m Smart Power SOC IC Technology for Automotive Applications	237
	T. Uhlig ¹ , A. Bemmann ¹ , C. Ellmers ¹ , F. F \ddot{u} rnhammer ¹ , M. Gro β ² , Y.H. Hu ³ , J. Liu ³ , R.-R. Ludwig ¹ , M. Reinhold ¹ , M. Stoisiek ² , E. Votintseva ⁴ , and M. Wittmaack ¹ ¹ ZMD Analog Mixed Signal Services, Germany ² Universitat Erlangen-Nurnberg, Germany ³ X-FAB, Malaysia ⁴ Qimonda, Germany	
P8-40	Vertical Power Dissipation Characteristics of Semiconductor Power Devices	241
	Y.S. Chung Freescale Semiconductor, USA	
P8-41	RESURFed Quasi Lateral IGBT Structure for High Current PICs	245
	E.M.S. Narayanan, T. Ramakrishna, and D.W. Green De Montfort University, UK	
P8-42	Analysis of the MOSFET Failure In a Junction-Isolated Power Integrated Circuit	249
	J. Jung ¹ , A.Q. Huang ¹ , and X. Li ² ¹ North Carolina State University, USA ² Texas Instruments, USA	
P8-43	Modeling and Analysis of Metal Interconnect Resistance of Power IC's	253
	Y. Chen, Y. Fu, X. Cheng, T.X. Wu, and Z.J. Shen University of Central Florida, USA	

Wednesday, May 30, 2007

Session 9 GaN and Diamond Devices

Chairs		
	Ichiro Omura (Toshiba, Japan)	
	Kwang-Hoon Oh (Fairchild Korea Semiconductor, Korea)	
O9-1	Normally-off AlGaIn/GaN Low-Density-Drain HEMTs (LDD-HEMT) with Enhanced Breakdown Voltage and Suppressed Current Collapse	257
	D. Song, Jie Liu, Z. Cheng, W.C.-W. Tang, K.M. Lau, and K.J. Chen Hong Kong University of Science and Technology, Hong Kong	
O9-2	1.8 kV AlGaIn/GaN HEMTs with High-k/Oxide/SiN MIS Structure	261
	S. Yagi ¹ , M. Shimizu ¹ , H. Okumura ¹ , H. Ohashi ¹ , K. Arai ¹ , Y. Yano ² , and N. Akutsu ² ¹ National Institute of Advanced Industrial Science and Technology, Japan ² Taiyo Nippon Sanso, Japan	

- O9-3 **Monolithic High-Voltage GaN MOSFET/Schottky Pair with Reverse Blocking Capability** 265
 W. Huang and T.P. Chow
 Rensselaer Polytechnic Institute, USA
- O9-4 **Diamond MISFETs fabricated on high quality polycrystalline CVD diamond** 269
 K. Hirama¹, H. Takayanagi¹, S. Yamauchi¹, Y. Jingu¹, H. Umezawa², and H. Kawarada¹
¹Waseda University, Japan
²National Institute of Advanced Industrial Science and Technology, Japan

Session 10 SiC Devices I

Chairs

- Jose Millán (CNM Barcelona, Spain)
 Eric J. Stewart (Northrop Grumman Advanced Technology Laboratory, USA)
- O10-1 **180kVA Three Phase SiCGT Inverter Utilizing Novel VF Degradation Reduction Phenomena for SiC Devices** 273
 Y. Sugawara, Y. Miyanagi, K. Nakayama, K. Asano, S. Ogata, S. Okada, T. Izumi, and A. Tanaka
 Kansai Electric Power, Japan
- O10-2 **20V-400A SiC Zener Diodes with Excellent Temperature Coefficient** 277
 R. Ishii^{1,2}, H. Tsuchida¹, K. Nakayama², and Y. Sugawara²
¹Central Research Institute of Electric Power Industry, Japan
²Kansai Electric Power, Japan
- O10-3 **New Improvement Results on 7.5 kV 4H-SiC p-IGBTs with Rdiff, on of 26 mΩ cm² at 25°C** 281
 Q. Zhang¹, C. Jonas¹, R. Callanan¹, J. Sumakeris¹, M. Das¹, A. Agarwal¹, J. Palmour¹, S.-H. Ryu², J. Wang³, and A.Q. Huang³
¹Cree, USA
²Wayne State University, USA
³North Carolina State University, USA

Session 11 SiC Devices II

Chairs

- Reinhard Herzer (Semikron, Germany)
 Florin Udrea (Cambridge University, UK)
- O11-1 **High temperature behaviour of 3.5 kV 4H-SiC JBS diodes** 285
 P. Brosselard¹, X. Jordà¹, M. Vellvehi¹, P. Godignon¹, J. Millán¹, J.P. Bergman², and B. Lambert³
¹CNM-CSIC, Spain
²Norstel AB, Sweden
³ESA/ESTEC, Netherlands
- O11-2 **Demonstration of motor drive with SiC normally-off IEMOSFET/SBD power converter** 289
 S. Harada, Y. Hayashi, K. Takao, A. Kinoshita, M. Kato, M. Okamoto, T. Kato, S. Nishizawa,
 T. Yatsuo, K. Fukuda, H. Ohashi, and K. Arai
 National Institute of Advanced Industrial Science and Technology, Japan

**O11-3 6kV 4H-SiC BJTs with Specific On-resistance Below the Unipolar
Limit using a Selectively Grown Base Contact Process**

293

S. Balachandran², C. Li³, P.A. Losee⁴, I.B. Bhat¹, and T.P. Chow¹

¹Rensselaer Polytechnic Institute, USA

²NXP Semiconductors, USA

³International Rectifier USA

⁴GE, USA