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11.3 High-Performance 45nm node CMOS Transistors Featuring Flash Lamp Annealing (FLA) , T. Sanuki, T. Iwamoto*, K. Ota**, T. Komoda, H. Yamazaki**, A. Eiho, K. Miyagi, K. Nakayama, O. Fuji, M. Togo*, K. Ohno**, H. Yoshimura, K. Yoshida, T. Ito, A. Mineji*, K. Yoshino, T. Itani, K. Matsuo, T. Saito, S. Mori, K. Nakazawa**, M. Nakazawa**, T. Shinyama**, K. Suguro, I. Mizushima, S. Iwasa, S. Muramatsu*, K. Nagaoka**, M. Ikeda*, M. Saito**, H. Naruse, Y. Enomoto**, T. Kitano*, M. Iwai, K. Imai*, N. Nagashima**, T. Kuwata*, F. Matsuoka, Toshiba Corporation, [^] NEC Electronics Corporation, ^{**} Sony Corporation	281	12.3 Doped In-Ge-Te Phase Change Memory Featuring Stable Operation and Good Data Retention , T. Morikawa, K. Kurotsuchi, M. Kinoshita, N. Matsuzaki, Y. Matsui, Y. Fujisaki, S. Hanzawa, A. Kotabe, M. Terao, H. Moriya, T. Iwasaki, M. Matsuoka*, F. Nitta*, M. Moniwa*, T. Koga*, N. Takaura, Hitachi Ltd., *Renesas Technology Corp.	307
10:20 a.m.		10:20 a.m.	
11.4 45nm High-k/Metal-Gate CMOS Technology for GPU/NPU Applications with Highest PFET Performance , H.T. Huang, Y.C. Liu, Y.T. Hou, R.C.-J. Chen, C.H. Lee, Y.S. Chao, P.F. Hsu, C.L. Chen, W.H. Guo, W.C. Yang, T.H. Perng, J.J. Shen, Y. Yasuda, K. Goto, C.C. Chen, K.T. Huang, H. Chuang, C.H. Diaz, M.S. Liang, TSMC	285	12.4 Statistical Analysis and Modeling of Programming and Retention in PCM Arrays , D. Mantegazza, D. Ielmini, E. Varesi*, A. Pirovano*, A.L. Lacaita, Politecnico di Milano, [^] STMicroelectronics	311
		10:45 a.m.	
		12.5 Evidence of the Thermo-Electric Thomson Effect and Influence on the Program Conditions and Cell Optimization in Phase-Change Memory Cells , D. Tio Castro, L. Goux*, G.A.M. Hurkx, K. Attenborough, R. Delhougne, J. Lisoni*, F.J. Jedema**, M.A.A. in't Zandt, R.A.M. Wolters, D.J. Gravesteijn, M.A. Verheijen**, M. Kaiser**, R.G.R. Weemaes, D.J. Wouters*, NXP-TSMC Research Center, [^] IMEC, ^{**} Philips Research Europe	315
		11:10 a.m.	
		12.6 A Novel Cross-Spacer Phase Change Memory with Ultra-Small Lithography Independent Contact Area , W.S. Chen, C.M. Lee, D.S. Chao, Y.C. Chen, F. Chen, C.W. Chen, P.H. Yen, M.J. Chen, W.H. Wang, T.C. Hsiao, J.T. Yeh, S.H. Chiou, M.Y. Liu*, T.C. Wang*, L.L. Chein**, C.M. Huang**, N.T. Shih [^] , L.S. Tu [^] , D. Huang [^] , T.H. Yu [^] , M.J. Kao, M.-J. Tsai, ITRI, [^] Powerchip Semiconductor Corp., ^{**} PrMOS Technologies, [^] Nanya Technology Corporation, ^{^^} Winbond Electronics Corp.	319
		11:35 a.m.	
		12.7 The Role of Interfaces in Damascene Phase-Change Memory , D.L. Kencke, I.V. Karpov, B.G. Johnson, S.J. Lee, D.C. Kau, S.J. Hudgens*, J.P. Reifenberg**, S.D. Savransky, J. Zhang, M.D. Giles, G. Spadini, Intel Corp., [^] Ovonyx Inc., ^{**} Stanford University	323

Session 13: Process Technology - Gate Stack Process I – Fundamental Aspects

Tuesday, December 11, 9:00 a.m.
Jefferson Room

9:05 a.m.

13.1 Tuning PMOS Mo(O,N) Metal Gates to NMOS by Addition of DyO Capping Layer, J. Petry, R. Singanamalla*, K. Xiong, C. Ravit, E. Simoens*, R. O'Connor*, A. Veloso*, C. Adelman*, S. Van Elshocht*, V. Paraschiv*, S. Brus*, J. Van Berkum**, S. Kubicek*, K. De Meyer*, S. Biesmans*, J.C. Hooker, NXP Semiconductors, *IMEC, KU Leuven, **Philips Research

9:30 a.m.

13.2 Very Low V_t [Ir-Hf]/HfLaO CMOS Using Novel Self-Aligned Low Temperature Shallow Junctions, C. F. Cheng, C. H. Wu*, N. C. Su*, S. J. Wang*, S. P. McAlister** and A. Chin, National Chiao-Tung University, *National Cheng Kung University, **National Research Council of Canada

9:55 a.m.

13.3 Mechanism of V_{th} roll-off with High Work function Metal Gate and Low Temperature Oxygen Incorporation to Achieve PMOS Band Edge Work function, S.C. Song, C. S. Park, J. Price*, C. Burham*, R. Choi, H.H. Tseng, H.C. Wen, K. Choi, B.H. Lee, and R. Jammy, SEMATECH, *University of Texas

10:20 a.m.

13.4 Comprehensive Study of V_{FB} Shift in High-k CMOS - Dipole Formation, Fermi-level Pinning and Oxygen Vacancy Effect -, Y. Kamimuta, K. Iwamoto, Y. Nunoshige*, A. Hirano, W. Mizubayashi*, Y. Watanabe, S. Migita*, A. Ogawa, H. Ota*, T. Nabatame, and A. Toriumi*, MIRAI-ASET, *MIRAI-ASRC

10:45 a.m.

13.5 Wide Controllability in Flatband Voltage by Tuning Crystalline Microstructures in Metal Gate Electrodes, K. Ohmori, T. Chikyow*, T. Hosoi**, H. Watanabe**, K. Nakajima*, T. Adachi*, A. Ishikawa*, Y. Sugita^, Y. Nara^, Y. Ohji^, K. Shiraishi***, K. Yamabe***, K. Yamada, Waseda University, *National Institute for Materials Science, **Osaka University, ^SELETE, ***University of Tsukuba

11:10 a.m.

13.6 Clarification of Additional Mobility Components associated with TaC and TiN Metal Gates in scaled HfSiON MOSFETs down to sub-1.0nm EOT, K. Tatsumura, M. Goto, S. Kawanaka, K. Nakajima, T. Schimizu, T. Ishihara, M. Koyama, Toshiba Corporation

11:35 a.m.

13.7 Impact of Flash Annealing on Performance and Reliability of High-k/Metal-Gate MOSFETs for Sub-45nm CMOS, P. Kalra, P. Majhi, D. Heh*, G. Bersuker*, C. Young*, N. Vora**, R. Harris***, P. Kirsch^, R. Choi*, M. Chang#, J. Lee#, H. Hwang#, H-H Tseng*, R. Jammy***, and T-J King Liu, University of California, Intel, *SEMATECH, **University of Texas at Austin, ***AMD, ^IBM, #GIST

Session 14: Emerging Technologies - Energy Harvesting Electron Devices

Tuesday, December 11, 9:00 a.m.
Lincoln Room

9:05 a.m.

14.1 Developments in Silicon Solar Cells (Invited), R. Swanson, SunPower Corp.

9:30 a.m.

14.2 Energy Harvesting - A Systems Perspective (Invited), J. Rabaey, F. Burghardt, D. Steingart, M. Seeman, P. Wright, Berkeley Wireless Research Center

9:55 a.m.

14.3 Energy Harvesting for Electronics with Thermoelectric Devices Using Nanoscale Materials (Invited), R. Venkatasubramanian, C. Watkins, D. Stokes, J. Posthill, C. Caylor, RTI International

10:20 a.m.

14.4 Nanogenerators and Nano-Piezotronics (Invited), Z.L. Wang, Georgia Institute of Technology

10:45 a.m.

14.5 Micro-engineered Devices for Motion Energy Harvesting, E. Yeatman, P. Mitcheson, A. Holmes, Imperial College London

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Session 15: Quantum, Power, and Compound Semiconductor Devices - Reliability and Characterizations of Power HEMTs

Tuesday, December 11, 9:00 a.m.
Military Room

9:05 a.m.

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15.1 A Review of Failure Modes and Mechanisms of GaN-Based HEMT's (Invited), E. Zanoni, G. Meneghesso, G. Verzellesi*, F. Danesin, M. Meneghini, F. Rampazzo, A. Tazzoli, F. Zanon, Universita di Padova, *Universita di Modena e Reggio Emilia

9:30 a.m.

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15.2 Gate Current Degradation Mechanisms of GaN High Electron Mobility Transistors, J. Joh, L. Xia, and J.A. del Alamo, Massachusetts Institute of Technology

9:55 a.m.

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15.3 Reliability of Enhancement-mode AlGaIn/GaN HEMTs Fabricated by Fluorine Plasma Treatment, C. Yi, R. Wang, W. Huang, W. C.-W. Tang, K.M. Lau, K.J. Chen, Hong Kong University of Science and Technology

10:20 a.m.

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15.4 Drain Corrosion in RF Power GaAs PHEMTs, A. Villanueva, J. del Alamo, T. Hisaka*, T. Ishida*, Massachusetts Institute of Technology, *Mitsubishi Electric Corporation

10:45 a.m.

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15.5 Remarkable Breakdown Voltage Enhancement in AlGaIn Channel HEMTs, T. Nanjo, M. Takeuchi*, M. Suita, Y. Abe, T. Oishi, Y. Tokuda and Y. Aoyagi**, Mitsubishi Electric Corporation, *RIKEN, **Tokyo Institute of Technology

11:10 a.m.

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15.6 Characterisation of AlGaIn/GaN HEMT Epitaxy and Devices on Composite Substrates, G. Meneghesso, C. Ongaro, E. Zanoni, C. Brylinski*, M.A. di Forte-Poisson*, V. Hoel**, J.C. de Jaeger**, R. Langer^, H. Lahreche^, P. Bove^, J. Thorpe#, Universita di Padova, *GIE ALCATEL-THALES, **IEMN/TIGER, ^PICOGIGA International, #United Monolithic Semiconductors GmbH

11:35 a.m.

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15.7 High-voltage Millimeter-Wave GaN HEMTs with 13.7 W/mm Power Density, Y.-F. Wu, M. Moore, A. Abrahamsen, M. Jacob-Mitos, P. Parikh, S. Heikman, and A. Burk*, Cree Santa Barbara Technology Center, *Cree Inc.

Session 16: Displays, Sensors, and MEMS - RF MEMS

Tuesday, December 11, 9:00 a.m.
Thoroughbred Room

9:05 a.m.

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16.1 Scalable 1.1 GHz Fundamental Mode Piezo-Resistive Silicon MEMS Resonator, J.T.M. van Beek, G.J.A.M. Verheijden, G.E.J. Koops, K.L. Phan, C. van der Avoort, J. van Wingerden, D. Ernur Badaroglu, J.J.M. Bontemps*, NXP-TSMC Research Center, *Technical University

3:35 p.m.			
19.4 Multi-probe Two-Dimensional Mapping of Off-State Degradation in DeNMOS Transistors: How and Why Interfacial Damage Predicts Gate Dielectric Breakdown , D. Varghese, H. Kufluoglu, V. Reddy*, H. Shichijo*, D. Mosher*, S. Krishnan*, M.A. Alam, Purdue University, *Texas Instruments			
4:00 p.m.			
19.5 Designing Reliable Systems with Unreliable Devices Challenges and Opportunities (Invited) , L. Benini, Universita di Bologna			
4:25 p.m.			
19.6 Copper Wiring Encapsulation with Ultra-thin Barriers to Enhance Wiring and Dielectric Reliabilities for 32-nm Nodes and Beyond , H. Kudo, M. Haneda, H. Ochimizu, A. Tsukune, S. Okano, N. Ohtsuka, M. Sunayama, H. Sakai*, T. Suzuki, H. Kitada, S. Amari*, T. Tabira, H. Matsuyama*, N. Shimizu*, T. Futatsugi, and T. Sugii, Fujitsu Laboratories Ltd., *Fujitsu Limited			
Session 20: Process Technology - Gate Stack Process II – Metal Gate/High K Integration Tuesday, December 11, 2:15 p.m. Jefferson Ballroom			
2:20			
20.1 Feasible Integration Scheme for Dual Work Function FUSI/HfSiON Gate Stacks with Selective Metal Pile-up to nMOSFET , Y. Tsuchiya, M. Yoshiki, A. Kaneko, S. Numiya, T. Saito, K. Nakajima, T. Aoyama, J. Koga, A. Nishiyama, M. Koyama, Toshiba Corp.	519		
2:45 p.m.			
20.2 Gate-First Processed FUSI/HfO₂/HfSiO_x/Si MOSFETs with EOT=0.5 nm -Interfacial Layer Formation by Cycle-by-Cycle Deposition and Annealing- , M. Takahashi, A. Ogawa, A. Hirano, Y. Kamimuta, Y. Watanabe, K. Iwamoto, S. Migita*, N. Yasuda, H. Ota*, T. Nabatame and A. Toriumi*, MIRAI-ASET, *MIRAI-ASRC	523		
3:10 p.m.			
20.3 Single Metal/Dual High-k Gate Stack with Low V_{th} and Precise Gate Profile Control for Highly Manufacturable Aggressively Scaled CMOSFETs , N. Mise, T. Morooka, T. Eimori, S. Kamiyama, K. Murayama*, M. Sato, T. Ono, T. Eimori, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies Inc., *Assoc. of Super-Advanced Electronics Technologies & Hitachi Kenki FineTech Co.	527		
3:35 p.m.			
20.4 Practical Dual-Metal-Gate Dual-High-k CMOS Integration Technology for hp 32 nm LSTP Utilizing Process-Friendly TiAlN Metal Gate , M. Kadoshima, T. Matsuki, M. Sato, T. Aminaka, E. Kurosawa, A. Ohta*, H. Yoshinaga*, S. Miyazaki*, K. Shiraishi**, Y. Yamabe**, K. Yamada^, T. Aoyama, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies Inc., *Hiroshima University, **University of Tsukuba, ^Waseda University	531		
4:00 p.m.			
20.5 A Dy₂O₃-capped HfO₂ Dielectric and TaC_x-based Metals Enabling Low-V_t Single-Metal-Single-Dielectric Gate Stack , V.S. Chang, L.-Å. Ragnarsson, G. Pourtois, R. O'Connor, C. Adelman, S. Van Elshocht, A. Delabie, J. Swerts, N. Van der Heyden, T. Conard, H.-J. Cho, A. Akheyar, R. Mitsuhashi, T. Witters, B.J. O'Sullivan, L. Pantisano, E. Rohr, P. Lehnen, S. Kubicek, T. Schram, S. De Gendt, P. P. Absil, and S. Biesemans, IMEC	535		
4:25 p.m.			
20.6 Band Edge Gate First HfSiON/Metal Gate n-MOSFETs using ALD-La₂O₃ Cap Layers Scalable to EOT=0.68 nm for hp 32nm Bulk Devices with High Performance and Reliability , S. Kamiyama, T. Miura, E. Kurosawa, M. Kitajima, M. Ootuka, T. Aoyama, and Y. Nara, SELETE	539		
4:50 p.m.			
20.7 Aggressively Scaled High-k Gate Dielectric with Excellent Performance and High Temperature Stability for 32nm and Beyond , P. Sivasubramani, P. D. Kirsch, J. Huang, C. Park, Y. N. Tan, D. Gilmer, C. Young, K. Freeman, M. Hussain, D. Lysaght, R. Harris**, S.C. Song, D. Heh, R. Choi, P. Majhi^, G. Bersuker, B.H. Lee, H.-H. Tseng, J.S. Jur#, D.J. Lichtenwalner#, A.I. Kingon#, and R. Jammy*, SEMATECH, *IBM, **AMD, ^Intel, #North Carolina State University	505		543
Session 21: Modeling and Simulation - Development and Applications of Compact Models for Advanced Circuits Tuesday, December 11, 2:15 p.m. Lincoln Room	509		
2:20 p.m.			
21.1 A Unified Compact Model of the Gate Oxide Reliability for Complete Circuit Level Analysis , C-H Lee, G-Y Yang, J-K Park, Y-K Park, B-S Yoo, H-W Kim, D. Park, M-H Yoo, Samsung Electronics Co., Ltd.	513		549
2:45 p.m.			
21.2 A Predictive Analytical Model of 3D MIM Capacitors for RC IC , N. Segura, S. Cremer, D. Gloria, L. Ciampolini, E. Picolet and M. Minondo, STMicroelectronics	517		553
3:10 p.m.			
21.3 Physically-Based Unified Compact Model for Low-Field Carrier Mobility in MOSFETs with Different Gate Stacks and Biaxial/Uniaxial Stress Conditions , S. Reggiani, L. Silvestri, A. Cacciatori*, E. Gnani, A. Gnudi, G. Baccarani, University of Bologna, *University of Brescia	519		557
3:35 p.m.			
21.4 A New Model for 1/f Noise in High-k MOSFETs , T. Morshed, S.P. Devireddy, M.S. Rahman, Z. Celik-Butler, H.-H. Tseng*, A. Zlotnicka**, A. Shanware^, K. Green^, J.J. Chambers^, M.R. Visokay^, M.A. Quevedo-Lopez^ and L. Colombo^, University of Texas, *Sematech, **Freescale Semiconductor, ^Texas Instruments	523		561
4:00 p.m.			
21.5 A Multi-Gate MOSFET Compact Model Featuring Independent-Gate Operation , D.D. Lu, M.V. Dunga, C.-H. Lin, A.M. Niknejad and C. Hu, University of California	527		565
4:25 p.m.			
21.6 High Performance CMOS Variability in the 65nm Regime and Beyond (Invited) , S. Nassif, K. Bernstein, D. Frank, A. Gattiker, W. Haensch, B. Ji, E. Nowak, D. Pearson, N. Rohrer, IBM	531		569
4:50 p.m.			
21.7 Rapid Circuit-based Optimization of Low Operational Power CMOS Devices , P. Christie, A. Nackaerts**, T. Hoffmann**, A. Kumar*, NXP-TSMC Research Center, *IMEC, **NXP Semiconductors	535		573
Session 22: Displays, Sensors, and MEMS - TFTs, Displays and Memories Tuesday, December 11, 2:15 p.m. Military Room	539		
2:20 p.m.			
22.1 ZnO Thin Film Transistor Ring Oscillators with sub 75 nsec Propagation Delay , J. Sun, D. Mourey, D. Zhao, S. Park, S. Nelson*, D. Levy*, D. Freeman*, P. Cowdery-Corvan*, L. Tutt*, T. Jackson, Penn State University, *Eastman Kodak	543		579
2:45 p.m.			
22.2 New Approach for Passivation of Ga₂O₃-In₂O₃-ZnO Thin Film Transistors , S.I. Kim, C.J. Kim, J.C. Park, I. Song, D.H. Kang, H. Lim, S.W. Kim, E. Lee, J.C. Lee and Y. Park, Samsung Advanced Institute of Technology	547		583

3:10 p.m.			
22.3 High Performance Transparent Thin Film Transistors Based on Indium Gallium Zinc Oxide as the Channel Material , A. Suresh, P. Wellenius and J. Muth, North Carolina State University	587	23.7 90 nm Self-Aligned Enhancement-Mode InGaAs HEMT for Logic Applications , N. Waldron, D-H Kim and J. A. del Alamo, Massachusetts Institute of Technology	633
3:35 p.m.		5:15 p.m.	
22.4 Sub-Micron CMOS / MOS-Bipolar Hybrid TFTs for System Displays , G. Kawachi, T. Okada, S. Tsuboi, M. Mitani, Advanced LCD Technologies Development Center Co., Ltd.	591	23.8 High Performance Submicron Inversion-Type Enhancement-Mode InGaAs MOSFETs with ALD Al₂O₃, HfO₂ and HfAlO as Gate Dielectrics , Y. Xuan, Y.Q. Wu, T. Shen, T. Yang and P.D. Ye, Purdue University	637
4:00 p.m.		Session 24: 2007 IEDM Special Evening Session Tuesday, December 11, 8:00 p.m. International Ballroom Center	
22.5 New In-Situ Process of Top Gate Nanocrystalline Silicon Thin Film Transistors Fabricated at 180°C for the Suppression of Leakage Current , J-H Park, S-M Han, Y-H Choi, S.-J. Kim, M-K Han, Seoul National University	595	Device/Circuit Interactions in Highly-Scaled CMOS: Challenges and Potential Solutions	641
4:25 p.m.		Session 25: 2007 IEDM Evening Panel Discussion Tuesday, December 11, 8:00 p.m. International Ballroom East	
22.6 Uniform High Current Field Emission of Electrons from Si and CNF FEAs Individually Controlled by Si Pillar Ungated FETs , L. Velasquez-Garcia, B. Adeoti, Y. Niu, and A.I. Akinwande, Massachusetts Insitute of Technology	599	Looking Beyond Silicon - A Pipe Dream or the Inevitable Next Step?	647
4:50 p.m.		Session 26: Quantum, Power, and Compound Semiconductor Devices - Ultra High Speed SiGe and InP-Based HBTs Wednesday, December 12, 9:00 a.m. International Ballroom West	
22.7 Compact Nano-Electro-Mechanical Non-Volatile Memory (NEMory) for 3D Integration , W.Y. Choi, H. Kam, D. Lee, J. Lai and T-J King Liu, University of California	603	9:05 a.m.	
Session 23: Quantum, Power, and Compound Semiconductor Devices - III-V FETs for Microwave, Millimeter Wave and Digital Applications Tuesday, December 11, 2:15 p.m. Thoroughbred Room		26.1 SiGe BiCMOS Technology with 3.0 ps Gate Delay , H. Ruecker, B. Heinemann, R. Barth, J. Bauer, K. Blum, D. Bolze, J. Drews, G. Fischer, A. Fox, O. Fursenko, T. Grabolla, U. Haak, W. Hoepfner, D. Knoll, K. Koepke, B. Kuck, A. Mai, S. Marschmeyer, T. Morgenstern, H. H. Richter, P. Schley, D. Schmidt, K. Schulz, B. Tillack, G. Weidner, W. Winkler, D. Wolansky, H.E. Wulf, Y. Yamamoto, IHP	651
2:20 p.m.		9:30 a.m.	
23.1 Sub 50 nm InP HEMT Device with Fmax Greater than 1 THz , R. Lai, X.B. Mei, W.R. Deal, W. Yoshida, Y.M. Kim, P.H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier*, L. Samoska*, A. Fung*, Northrop Grumman Space Technology and *Jet Propulsion Laboratory	609	26.2 A Novel Fully Self-Aligned SiGe:C HBT Architecture Featuring a Single-Step Epitaxial Collector-Base Process , J.J.T.M. Donkers, M.C.J.C.M. Kramer, S. Van Huylbroeck*, L.J. Choi*, P. Meunier-Beillard, A. Sibaja-Hernandez*, G. Boccardi, W. van Noort, G.A.M. Hurkx, T. Vanhoucke, F. Vleugels*, G. Winderickx*, E. Kunnen*, S. Peeters*, D. Baute*, B. De Vos*, T. Vandeweyer*, R. Loo*, R. Venegas*, R. Pijper, F.C. Voogt**, S. Decoutere*, E.A. Hijzen, NXP-TSMC Research Center, *IMEC, **NXP Semiconductors	655
2:45 p.m.		9:55 a.m.	
23.2 610GHz In_{0.52}AlAs/In_{0.75}GaAs Metamorphic HEMTs with an Ultra-Short 15-nm-Gate , S-J Yeon, M. Park, J.H. Choi*, K. Seo, Seoul National University, *Korea Advanced Nanofab Center	613	26.3 Electrically pumped Ge Laser at room temperature , T-H. Cheng, P-S. Kuo, C.T. Lee, M.H. Liao, T.A. Hung, C.W. Liu, National Taiwan University	659
3:10 p.m.		10:20 a.m.	
23.3 0.1 μm In_{0.2}Al_{0.8}Sb-InAs HEMT Low Noise Amplifiers for Ultralow-Power Applications , Y.C. Chou, M.D. Lange, B.R. Bennett*, J.B. Boos*, J.M. Yang, N.A Papanicolaou*, C.H. Lin, L.J. Lee, P.S. Nam, A.L Gutierrez, D.S. Farkas, R.S. Tsai, M. Wojtowicz, T.P. Chin, A.K. Oki, Northrop Grumman Corporation, *Naval Research Laboratory	617	26.4 Type-II GaAsSb/InP DHBTs With Record f_T = 670 GHz and Simultaneous f_T, f_{MAX} > 400 GHz , W. Snodgrass, B-R Wu, K.Y. Cheng, and M. Feng, University of Illinois at Urbana-Champaign	663
3:35 p.m.		10:45 a.m.	
23.4 High Mobility III-V MOSFETs for RF and Digital Applications (Invited) , M. Passlack, P. Zurcher, K. Rajagopalan, R. Droopad, J. Abrokwhah, M. Tutt, Y-B Park, E. Johnson, O. Hartin, A. Zlotnicka, P. Fejes, R. Hill*, D. Moran*, X. Li*, H. Zhou*, D. Macintyre*, S. Thoms*, A. Asenov*, K. Kalna* and I. Thayne*, Freescale Semiconduct, *University of Glasgow	621	26.5 600 GHz InP/GaAsSb/InP DHBTs Grown by MOCVD with a Ga(As,Sb) Graded-Base and f_T X BV_{CEO} > 2.5 THz-V at Room Temperature , H.G. Liu, O. Ostinelli, Y. Zeng, C.R. Bolognesi, Swiss Federal Institute of Technology	667
4:00 p.m.		11:10 p.m.	
23.5 Heterogeneous Integration of Enhancement Mode In_{0.7}Ga_{0.3}As Quantum Well Transistor on Silicon Substrate using Thin (≤2um) Composite Buffer Architecture for High-Speed and Low-Voltage (0.5V) Logic Applications , M. K. Hudait, G. Dewey, S. Datta, J. M. Fastenau*, J. Kavalieros, W. K. Liu*, D. Lubyshev*, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit, R. Chau, Intel Corp., *IQE Inc.	625	26.6 High-Speed InP HBT Technology for Advanced Mixed-Signal and Digital Applications , C. Monier, D. Scott, M. D'Amore, B. Chan, L. Dang, A. Cavus, E. Kaneshiro, P. Nam, K. Sato, N. Cohen, S. Lin, K. Luo, J. Wang, B. Oyama, and A. G. Gutierrez, Northrop-Grumman Space Technology	671
4:25 p.m.			
23.6 Logic Performance of 40 nm InAs HEMTs , D-H Kim and J. del Alamo, Massachusetts Institute of Technology	629		

Session 27: Process Technology - Advanced Process and Integration Technology

Wednesday, December 12, 9:00 a.m.
International Ballroom Center

9:05 a.m.

27.1 Embedded Flash on 90nm Logic Technology and Beyond for FPGAs (Invited), H. Kojima, T. Ema, T. Anezaki, J. Ariyoshi, H. Ogawa, K. Yoshizawa, S. Mehta*, S. Fong*, S. Logie*, R. Smoak*, D. Rutledge*, Fujitsu Ltd. And *Lattice Semiconductor Corp.

9:30 a.m.

27.2 Gatestacks for Scalable High-Performance FinFETs, G. Vellianitis, M.J.H. van Dal, L. Witters*, G. Curatola, G. Doornbos, N. Collaert*, C. Jonville, C. Torregiani*, L.-S. Lai**, J. Petry, B.J. Pawlak, R. Duffy, M. Demand*, S. Beckx*, S. Mertens*, A. Delabie*, T. Vandeweyer*, C. Delvaux*, F. Leys*, A. Hikavy*, R. Rooyackers*, M. Kaiser**, R.J.R. Weemaes**, F. Voogt^, H. Roberts^, D. Donnet^, S. Biesemans*, M. Jurczak*, R.J.P. Lander, NXP-TSMC Research Center, *IMEC, **Philips, ***TSMC, ^NXP Semiconductors

9:55 a.m.

27.3 Route to Low Parasitic Resistance in MuGFETs with Silicon-Carbon Source/Drain: Integration of Novel Low Barrier Ni(M)Si:C Metal Silicides and Pulsed Laser Annealing, R.T-P Lee, A.T-Y Koh, F-Y Liu, W-W Fang, T-Y. Liow, K-M. Tan, P-C. Lim*, A.E-J. Lim, M. Zhu, K-M. Hoe^, C-H. Tung^, G-Q. Lo*, X. Wang**, D.K-Y. Low**, G.S. Samudra, D-Z. Chi*, Y-C. Yeo, National University of Singapore, *Institute of Materials Research and Engineering, ^Institute of Microelectronics, **Singapore Institute of Manufacturing Technology

10:20 a.m.

27.4 Si/SiGe Epitaxy: a Ubiquitous Process for Advanced Electronics (Invited), D. Dutartre, N. Loubet, F. Brossard, B. Vandelle, P. Chevalier, A. Chantre, S. Monfray, C. Fenouillet-Beranger*, A. Pouydebasque, T. Skotnicki, STMicroelectronics, *CEA LETI-MINATEC

10:45 a.m.

27.5 Localized SOI Technology: An Innovative Low Cost Self-Aligned Process for Ultra Thin Si-film on Thin BOX Integration for Low Power Applications, S. Monfray, M. Samson, D. Dutartre, T. Ernst*, E. Rouhouze, D. Renaud*, B. Guillaumot, D. Chanemougame, G. Rabille, S. Borel*, JP. Colonna*, C. Arvet, N. Loubet, Y. Campidelli, JM. Hartmann*, L. Vandroux*, D. Bensahel, A. Toffoli*, F. Allain*, A. Margin, L. Clement**, A. Quiroga, S. Deleonibus*, T. Skotnicki, STMicroelectronics, *CEA LETI MINATEC, **NXP Semiconductor

11:10 a.m.

27.6 Proof of Ge-Interfacing Concepts for Metal/High-k/Ge CMOS -Ge-intimate Material Selection and Interface Conscious Process Flow-, T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita and A. Toriumi, The University of Tokyo

Session 28: CMOS Devices - Physics and Technologies of Mobility Enhancement

Wednesday, December 12, 9:00 a.m.
International Ballroom East

9:05 a.m.

28.1 Extension of Universal Mobility Curve to Multi-Gate MOSFETs, H. Yoshimoto, N. Sugii, D. Hisamoto, S-I Saito, R. Tsuchiya and S. Kimura, Hitachi, Ltd.

9:30 a.m.

28.2 More-than-Universal Mobility in Double-Gate SOI p-FETs with Sub-10-nm Body Thickness -Role of Light-Hole Band and Compatibility with Uniaxial Stress Engineering-, S. Kobayashi, M. Saitoh, K. Uchida, Toshiba Corp.

9:55 a.m.

28.3 Physical Understanding of Fundamental Properties of Si (110) pMOSFETs - Inversion-Layer Capacitance, Mobility Universality, and Uniaxial Strain Effects-, M. Saitoh, S. Kobayashi, K. Uchida, Toshiba Corp.

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10:20 a.m.

28.4 Mobility Enhancement in Uniaxially Strained (110) oriented Ultra-Thin Body Single- and Double-Gate MOSFETs with SOI Thickness of less than 4 nm, K. Shimizu and T. Hiramoto, University of Tokyo

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10:45 a.m.

28.5 Examination of Additive Mobility Enhancements for Uniaxial Stress Combined with Biaxially Strained Si, Biaxially Strained SiGe and Ge Channel MOSFETs, O. Weber, T. Irisawa*, T. Numata*, M. Harada*, N. Taoka**, Y. Yamashita*, T. Yamamoto*, N. Sugiyama*, M. Takenaka and S. Takagi, The University of Tokyo, *MIRAI_ASET, **MIRAI-AIST

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11:10 a.m.

28.6 Interface-Engineered Ge (100) and (111), N- and P-FETs with High Mobility, D. Kuzum, A.J. Pethe, T. Krishnamohan, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, Stanford University

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11:35 a.m.

28.7 High Performance PMOSFETs Using Si/Si_xGe_x/Si Quantum Wells with High-k/Metal Gate Stacks and Additive Uniaxial Strain for 22 nm Technology and Beyond, S. Suthram, P. Majhi, G. Sun^, P. Kalra*, H.R. Harris, K.J. Choi^, D. Heh, J. Oh, D. Kelly, R. Choi, B.J. Cho**, M.M. Hussain, C. Smith, S. Banerjee, W. Tsai, S.E. Thompson^, H.H. Tseng, R. Jammy, SEMATECH, *University of California, **National University of Singapore, ^Jusung Engineering, ^^University of Florida

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Session 29: Modeling and Simulation - Nanotubes, Nanowires and Nanoribbons

Wednesday, December 12, 9:00 a.m.
Georgetown Ballroom

9:05 a.m.

29.1 Three-dimensional Modeling of Gate Leakage in Si Nanowire Transistors, M. Luisier, A. Schenk, W. Fichtner, ETH Zurich

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9:30 a.m.

29.2 Band Structure Effects on the Current-Voltage Characteristics of SNW-FETs, E. Gnani, A. Gnudi, S. Reggiani, M. Rudan, G. Baccarani, University of Bologna

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9:55 a.m.

29.3 1-D and 2-D Devices Performance Comparison including Parasitic Gate Capacitance and Screening Effect, L. Wei, J. Deng, H.-S.P. Wong, Stanford University

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10:20 a.m.

29.4 Exciton Generation in Suspended Carbon Nanotube FETs: A Computational Study, S.O. Koswatta, V. Perebeinos*, M.S. Lundstrom, Ph. Avouris*, Purdue University, *IBM Research Division

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10:45 a.m.

29.5 A Comprehensive Atomic Study of Carbon Nanotube Schottky Diode Using First Principles Approach, P. Bai, K.T. Lam, E. Li, and K.K-F. Chang, Institute of High Performance Computing

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11:10 a.m.

29.6 Analytical Model of Carbon Nanotube Electrostatics: Density of States, Effective Mass, Carrier Density, and Quantum Capacitance, D. Akinwande, Y. Nishi, H.-S.P. Wong, Stanford University

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11:35 a.m.			
29.7 Performance Comparison of Graphene Nanoribbon Schottky Barrier and MOSFETs , G. Fiori, Y. Yoon*, S. Hong*, G. Iannaccone, J. Guo*, University de Pisa, *University of Florida	757		
12:00 p.m.			
29.8 Simulation Investigation of Double-Gate CNR-MOSFETs with a Fully Self-Consistent NEGF and TB Method , X. Guan, M. Zhang, Q. Liu, and Z. Yu, Tsinghua University	761		
Session 30: Solid State and Nanoelectronic Devices - Emerging Resistive RAM and New Function on Silicon Wednesday, December 12, 9:00 a.m. Jefferson Room			
9:05 a.m.			
30.1 Low Power and High Speed Switching of Ti-doped NiO ReRAM under the Unipolar Voltage Source of less than 3V , K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Iizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, and Y. Sugiyama, Fujitsu Laboratories	767		
9:30 a.m.			
30.2 2-stack 1D-1R Cross-point Structure with Oxide Diodes as Switch Elements for High Density Resistance RAM Applications , M.J. Lee, Y. Park, B.S. Kang, S.E. Ahn, C.B. Lee, K.H. Kim, W. Xianyu, G. Stefanovich, J.H. Lee, S.J. Chung, Y.H. Kim, C.S. Lee, J.B. Park, I.G. Baek* and I.K. Yoo, Samsung Advanced Institute of Technology, *Samsung Electronics, Co., Ltd.	771		
9:55 a.m.			
30.3 Conductive-Filament Switching Analysis and Self-Accelerated Thermal Dissolution Model for Reset in NiO-Based RRAM , U. Russo, D. Ielmini, C. Cagli, A. Lacaíta, S. Spiga*, C. Wiemer*, M. Perego*, M. Fanciulli*, Politecnico di Milano, *CNR-INFN	775		
10:20 a.m.			
30.4 Fast Switching and Long Retention Fe-O ReRAM and its Switching Mechanism , S. Muraoka, K. Osano, Y. Kanzawa, S. Mitani, S. Fujii, K. Katayama, Y. Katoh, Z. Wei, T. Mikawa, K. Arita, Y. Kawashima, R. Azuma, K. Kawai, K. Shimakawa, A. Odagawa, T. Takagi, Matsushita Electric Industrial Co., Ltd.	779		
10:45 a.m.			
30.5 A Novel Resistance Memory with High Scalability and Nanosecond Switching , K. Aratani, K. Ohba, T. Mizuguchi, S. Yasuda, T. Shiimoto, T. Tsushima, T. Sone, K. Endo, A. Kouchiyama, S. Sasaki, A. Maesaka, N. Yamada, and H. Narisawa, Sony Corporation	783		
11:10 a.m.			
30.6 Silicon Photonics Approach for Nanotechnology Era (Invited) , K. Ohashi, K. Nishi, T. Shimizu, M. Nakada, J. Fujikata, J. Ushida, K. Nose, A. Gomyo, T. Ishi, M. Mizuno, M. Kinoshita, N. Suzuki, D. Okamoto, H. Yukawa, T. Tsuchizawa*, T. Watanabe*, K. Yamada*, S. Itabasi*, J. Akedo**, MIRAI-Selete, *NTT, **AIST	787		
11:35 a.m.			
30.7 Single-Electron Circuit for Stochastic Data Processing Using nano-MOSFETs , K. Nishiguchi, A. Fujiwara, NTT Corporation	791		
Session 31: CMOS and Interconnect Reliability - Negative Bias Temperature Instability Wednesday, December 12, 9:00 a.m. Lincoln Room			
9:05 a.m.			
31.1 New Characterization and Modeling Approach for NBTI Degradation from Transistor to Product Level , V. Huard, C. Parthasarathy, N. Rallet, C. Guerin, M. Mammase, D. Barge, C. Ouvrard*, STMicroelectronics, *NXP Semiconductors	797		
9:30 a.m.			
31.2 Simultaneous Extraction of Recoverable and Permanent Components Contributing to Bias-Temperature Instability , T. Grasser, B. Kaczer*, P. Hehenberger, W. Goes, R. O'Connor*, H. Reisinger**, W. Gustin**, and C. Schluender**, TU Wien, *IMEC, **Infineon Technologies	801		
9:55 a.m.			
31.3 Theory and Practice of On-the-fly and Ultra-fast V_T Measurements for NBTI Degradation: Challenges and Opportunities , A.E. Islam, E. N. Kumar*, H. Das*, S. Purawat*, V. Maheta*, H. Aono**, E. Murakami**, S. Mahapatra*, M.A. Alam, Purdue University, *IIT Bombay, **Renesas Technologies	805		
10:20 a.m.			
31.4 Material Dependence of NBTI Physical Mechanism in Silicon Oxynitride (SiON) p-MOSFETs: A Comprehensive Study by Ultra-Fast On-The-Fly (UF-OTF) I_{DLIN} Technique , E.N. Kumar, V.D. Maheta, S. Purawat, A. E. Islam*, C. Olsen**, K. Ahmed**, M. A. Alam* and S. Mahapatra, IIT Bombay, *Purdue University, **Applied Materials	809		
10:45 a.m.			
31.5 On-The-Fly Interface Trap Measurement and Its Impact on the Understanding of NBTI Mechanism for p-MOSFETs with SiON Gate Dielectric , W.J. Liu, Z.Y. Liu, D. Huang, C.C. Liao*, L.F. Zhang*, Z.H. Gan*, W. Wong*, C. Shen**, and M-F. Li, Fudan University, *Semiconductor Manufacturing International Corp., **National University of Singapore	813		
11:10 a.m.			
31.6 Real V_{th} Instability of pMOSFETs Under Practical Operation Conditions , J.F. Zhang, Z. Ji, M.H. Chang, B. Kaczer*, and G. Groeseneken*, Liverpool John Moores University, *IMEC	817		
11:35 a.m.			
31.7 New Observations on the Hot Carrier and NBTI Reliability of Silicon Nanowire Transistors , R. Wang, R. Huang, D-W Kim*, Y. He, Z. Wang, G. Jia, D. Park*, Y. Wang, Peking University, *Samsung Electronics Co.	821		
12:00 p.m.			
31.8 Impact of TiN Metal Gate on NBTI Assessed by Interface States and Fast Transient Effects Characterization , M. Rafik, X. Garros*, G. Ribes, G. Ghibaudo*, C. Hobbs [^] , A. Zauner****, M. Muller***, V. Huard, C.Ouvrard***, STMicroelectronics, *CEA-LETI, **IMEP-LAHC, ***NXP, [^] Freescale	825		
Session 32: Displays, Sensors, and MEMS - Chemical and Biological Sensors, and Microsystems Wednesday, December 12, 9:00 a.m. Thoroughbred Room			
9:05 a.m.			
32.1 Three Technologies for a Smart Miniaturized Gas-Sensor: SOI CMOS, Micromachining and CNTs - Challenges and Performance , F. Udrea, S. Maeng**, J.W. Gardner*, J. Park**, M.S. Haque, S.Z. Ali, Y. Choi**, P.K. Guha, S.M.C. Vieira, H.Y. Kim**, S.Y. Lee**, S. H. Kim**, K.C. Kim**, S.E. Moon**, W.I. Milne, University of Cambridge, *University of Warwick, **Electronics and Telecommunications Research Institute	831		

9:30 a.m.			
32.2 AlGaIn/GaN Heterostructure Field Effect Transistors for High Temperature Hydrogen Sensing with Enhanced Sensitivity , J. Song and W. Lu, The Ohio State University	835	33.6 Impact of Self-Heating Effect on Hot Carrier Degradation in High-Voltage LDMOS , C.C. Cheng, J.F. Lin, T. Wang, T.H. Hsieh*, J.T. Tzeng*, Y.C. Jong*, R.S. Liou*, S.C. Pan*, and S.L. Hsu*, National Chiao-Tung University, *TSMC	881
9:55 a.m.			
32.3 Improved Liquid Phase Chromatography Separation Using Sub-micron Micromachining Technology , D. Sabuncuoglu Tezcan, A. Verbist, W. De Malsche*, J. Vangelooven*, H. Eghballi*, D. Clicq*, G. Desmet* and P. De Moor, IMEC, *Vrije Universiteit Brussel	839	Session 34: CMOS Devices - Advanced Device Structures Wednesday, December 12, 1:30 p.m. International Ballroom Center	
10:20 a.m.		1:35 p.m.	
32.4 A Micro Ionizer for Portable Mass Spectrometers using Double-gated Isolated Vertically Aligned Carbon Nanofiber Arrays , L.-Y. Chen, L.F. Velasquez-Garcia, X. Wang*, and K. Teo*, and A.I. Akinwande, Massachusetts Institute of Technology, *University of Cambridge	843	34.1 Observation of Mobility Enhancement in Strained Si and SiGe tri-gate MOSFETs with Multi-nanowire Channels Trimmed by Hydrogen Thermal Etching , T. Tezuka, E. Toyoda*, S. Nakaharai, T. Irisawa, N. Hirashita, Y. Moriyama, N. Sugiyama, N. Taoka**, Y. Yamashita**, O. Kiso**, M. Harada, T. Yamamoto, S. Takagi**, MIRA-ASET, *Covalent Materials Corp., **MIRAI-AIST	887
10:45 a.m.		2:00 p.m.	
32.5 Optoelectronic Tweezers for Manipulation of Cells and Nanowires (Invited) , M.C. Wu, University of California	847	34.2 Investigation of Nanowire Size Dependency on TSNWFET , S.D. Suk, M. Li, Y-Y Yeoh, K. Yeo, K.H. Cho, I.K. Ku, H. Cho, WJ Jang, D-W Kim, D. Park, and W-S Lee, Samsung Electronics	891
11:10 a.m.		2:25 p.m.	
32.6 Integrated ZnO Surface Acoustic Wave Microfluidic and Biosensor System , D.S. Lee*, S. Maeng*, Y.Q. Fu, X.Y. Du, S.C. Tan, J.K. Luo, A.J. Flewitt, S.H. Kim*, N. M. Park*, H. C. Yoon**, W.I. Milne, S.Y. Oh*, University of Cambridge, *Electronics and Telecommunications Research Institute (ETRI), **Ajou University,	851	34.3 New Self-Aligned Silicon Nanowire Transistors on Bulk Substrate Fabricated by Epi-Free Compatible CMOS Technology: Process Integration, Experimental Characterization of Carrier Transport and Low Frequency Noise , Y. Tian, R. Huang, Y. Wang, J. Zhuge, R. Wang, J. Liu, X. Zhang, Y. Wang, Peking University	895
11:35 a.m.		2:50 p.m.	
32.7 Electrical Measurement of Adhesion and Viability of Living Cells with a Silicon Chip , L. Bandiera, M.Borgo, G. Cellere*, A.De Toni*, L. Santoni, M. Dal Maschio*, S. Girardi*, L. Lorenzelli**, and A. Paccagnella*, Biosilab, *Universita di Padova, **FBK-irst	855	34.4 Experimental Investigation on Superior PMOS Performance of Uniaxial Strained Silicon Nanowire Channel By Embedded SiGe <110> Source/Drain , M. Li, K.H. Yeo, Y-Y Yeoh, S.D. Suk, K.H. Cho, D-W Kim, D Park, and W-S Lee, Samsung Electronics Co., Ltd.	899
Session 33: Quantum, Power, and Compound Semiconductor Devices - High Voltage Power Devices Wednesday, December 12, 1:30 p.m. International Ballroom West		3:15 p.m.	
1:35 p.m.		34.5 A Novel Body Effect Reduction Technique to Recessed Channel Transistor Featuring Partially Insulating Layer Under Source and Drain: Application to Sub-50nm DRAM Cell , J-M Park, S-O Sohn, J-S Park, S.-Y. Han, J-B Lee, W. Kim, C.-H. Jeon, S.-D. Kim, Y.-P. Kim, Y.-S. Lee, S. Yamada, W. Yang, D. Park, W.-S. Lee, Samsung Electronics Co.	903
33.1 8300V Blocking Voltage AlGaIn/GaN Power HFET with Thick Poly-AlN Passivation , Y. Uemoto, D. Shibata, M. Yanagihara, H. Ishida, H. Matsuo, S. Nagai*, N. Batta*, M. Li*, T. Ueda, T. Tanaka, D. Ueda, Matsushita Electric-Panasonic, *Panasonic Technologies	861	3:40 p.m.	
2:00 p.m.		34.6 Ultra-Low Leakage Silicon-on-Insulator Technology for 65 nm Node and Beyond , J. Cai, A. Majumdar, D. Dobuzinsky*, T.H. Ning, S. Koester, and W. Haensch, IBM Research, *IBM SRDC	907
33.2 650V 3.1mQcm² GaN-based Monolithic Bidirectional Switch Using Normally-off Gate Injection Transistor , T. Morita, M. Yanagihara, H. Ishida, M. Hikita, K. Kaibara, H. Matsuo, Y. Uemoto, T. Ueda, T. Tanaka, D. Ueda, Matsushita Electric - Panasonic	865	Session 35: Solid State and Nanoelectronic Devices - Nanoscale Flash and DRAM Technologies Wednesday, December 12, 1:30 p.m. International Ballroom East	
2:25 p.m.		1:35 p.m.	
33.3 Current Collapseless High-Voltage GaN-HEMT and its 50-W Boost Converter Operation , W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, Y. Saito, I. Omura and M. Yamaguchi, Toshiba Corporation	869	35.1 A High-Speed BE-SONOS NAND Flash Utilizing the Field-Enhancement Effect of FinFET , T-H Hsu, H-T Lue, E-K. Lai, J-Y Hsieh, S-Y Wang, L-W Yang, Y-C King*, T. Yang, K-C Chen, K-Y Hsieh, R. Liu, and C-Y Lu, Macronix International Co., Ltd., *National Tsing-Hua University	913
2:50 p.m.		2:00 p.m.	
33.4 High-Performance p-channel Diamond MOSFETs with Alumina Gate Insulator , K. Hiram, H. Takayanagi, S. Yamauchi, Y. Jingu, H. Umezawa*, H. Kawarada, Waseda University, *AIST	873	35.2 Highly Scalable Vertical Double Gate NOR Flash Memory , H. Cho, P. Kapur, P. Kalavade* and K.C. Saraswat, Stanford University, *Intel	917
3:15 p.m.			
33.5 Stress-Induced Mobility Enhancement for Integrated Power Transistors , P. Moens, J. Roig, F. Clemente*, I. De Wolf*, B. Desoete, F. Bauwens, M. Tack, AMI Semiconductor Belgium, *IMEC	877		

2:25 p.m.	35.3 Advantages of the FinFET Architecture in SONOS and Nanocrystal Memory Devices , S. Lombardo, C. Gerardi*, L. Breuil**, C. Jahan***, L. Perniola***, G. Cina*, D. Corso, E. Tripiciano*, V. Ancarani*, G. Iannaccone [^] , G. Iacono*, C. Bongiorno, J. Razafindramora***, C. Garozzo, P. Barbera, E. Nowak***, R. Puglisi, G. A. Costa*, C. Coccorese*, M. Vecchio*, E. Rimini, J. Van Houdt**, B. De Salvo***, M. Melanotte*, CNR-IMN, *STMicroelectronics, **IMEC, ***CEA-LETI, [^] University of Pisa	4:05 p.m.	36.7 Novel doping technology for a 1nm NiSi/Si junction with dipoles comforting Schottky (DCS) barrier , T. Yamauchi, Y. Nishi, Y. Tsuchiya, A. Kinoshita, J. Koga, K. Kato, Toshiba Corp.	963
2:50 p.m.	35.4 New Generation of Z-RAM , S. Okhonin, M. Nagoga, E. Carman, R. Beffa, E. Faraoni, Innovative Silicon	4:05 p.m.	36.7 Novel doping technology for a 1nm NiSi/Si junction with dipoles comforting Schottky (DCS) barrier , T. Yamauchi, Y. Nishi, Y. Tsuchiya, A. Kinoshita, J. Koga, K. Kato, Toshiba Corp.	963
3:15 p.m.	35.5 A Unified-RAM (URAM) Cell Multi-Functioning Capacitorless DRAM and NVM , J-W Han, S-W Ryu, C. Kim, S-H Kim, M. Im, S-J Choi, J.S. Kim*, K.H. Kim*, G.S. Lee*, J.S. Oh*, M.H. Song*, Y.C. Park*, J.W. Kim*, and Y-K Choi, KAIST, *National Nanofab Center	5:00 p.m.	37.1 32 nm node Ultralow-k(k=2.1)/Cu Damascene Multilevel Interconnect using High-Porosity (50 %) High-Modulus (9 GPa) Self-Assembled Porous Silica , S. Chikaki, K. Kinoshita, T. Nakayama*, K. Kohmura**, H. Tanaka**, M. Hirakawa*, E. Soda, Y. Seino***, N. Hata***, T. Kikkawa***, and S. Saito, Selete, *ULVAC, Inc., **Mitsui Chemicals, Inc., ***AIST	969
3:40 p.m.	35.6 Extremely Low-voltage and High-speed Operation Bulk Thyristor-SRAM/DRAM (BT-RAM) Cell with Triple Selective Epitaxy Layers (TEL) , T. Sugizaki, M. Nakamura, M. Yanagita, M. Shinohara, T. Ikuta, T. Ohchi, K. Kugimiya, S. Kanda, K. Yagami and T. Oda, Sony Corporation	5:00 p.m.	37.2 Cost-effective and High Performance Cu Interconnects ($k_{eff}=2.75$) with Continuous SiOCH Stack Incorporating a Low-k Barrier Cap (k=3.1) , M. Ueki, H. Yamamoto, F. Ito, J. Kawahara, M. Tada, T. Takeuchi, S. Saito, N. Furutake, T. Onodera, Y. Hayashi, NEC Corporation	973
	Session 36: Modeling and Simulation - Simulation of Processes and Advanced Memories Wednesday, December 12, 1:30 p.m. Georgetown Ballroom	5:00 p.m.	37.3 Bulk and Interface Band Diagrams of Advanced Intermetal Dielectrics , C. Guedj, E. Martinez, C. Licitra, G. Imbert*, J.P. Barnes, D. Lafond, A. Toffoli, LETI-MINATEC, *STMicroelectronics	977
1:35 p.m.	36.1 Physical Interpretation, Modeling and Impact on Phase Change Memory (PCM) Reliability of Resistance Drift Due to Chalcogenide Structural Relaxation , D. Ielmini, S. Lavizzari, D. Sharma and A. L. Lacaita, Politecnico di Milano	5:00 p.m.	37.4 FR-4 and CMOS: Enabling Technologies for Consumer Volume Millimeterwave Applications (Invited) , J. Laskar, S. Pinel, D. Dawn, S. Sarkar, P. Sen, B. Perunama, D. Yeh, Georgia Institute of Technology	981
2:00 p.m.	36.2 Physical Model for NAND operation in SOI and Body-Tied Nanocrystal FinFLASH memories , L. Perniola, E. Nowak, G. Iannaccone*, P. Scheiblin, C. Jahan, G. Pananakakis**, J. Razafindramora, B. De Salvo, S. Deleonibus, G. Reimbold, F. Boulanger, CEA-LETI-MINATEC, *Universita di Pisa, **IMEP/INPG Grenoble	5:15 p.m.	37.5 New Three-Dimensional Integration Technology Based on Reconfigured Wafer-on-Wafer Bonding Technique , T. Fukushima, H. Kikuchi, Y. Yamada, T. Konno, J. Liang, K. Sasaki, K. Inamura, T. Tanaka, and M. Koyanagi, Tohoku University	985
2:25 p.m.	36.3 Development of A 3D Simulator for Metal Nanocrystal (NC) Flash Memories under NAND Operation , A. Nainani, S. Palit, P. K. Singh, U. Ganguly, N. Krishna*, J. Vasi and S. Mahapatra, IIT Bombay, *Applied Materials	5:40	37.6 Highly Reliable Thin MIM Capacitor on Metal (CoM) Structure with Vertical Scalability for Analog/RF Applications , N. Inoue, I. Kume, J. Kawahara, N. Furutake, T. Toda*, K. Matsui*, M. Furumiya*, T. Iwaki*, S. Shida*, Y. Hayashi, NEC Corp., *NEC Electronics Corp.	989
2:50 p.m.	36.4 Current Capabilities Future Prospects of Atomistic Process Simulation (Invited) , M. Jaraiz, P. Castrillo, R. Pinacho, and J.E. Rubio, University of Valladolid	5:40	37.7 Mass Productive Worthy MIM Capacitor On Gate poly silicon(MIM-COG) Structure using HfO₂/HfO_xC_yN_z/HfO₂ Dielectric for Analog/RF/Mixed Signal Application , J-M Park, M-W Song W-H Kim, P-K Park, Y-K Jung, J-Y Kim, S-J Won, J-H Lee, N-I Lee, H-K Kang, Samsung Electronics Co., Ltd.	993
3:15 p.m.	36.5 Analysis of As, P Diffusion and Defect Evolution during Sub-millisecond Non-melt Laser Annealing based on an Atomistic Kinetic Monte Carlo Approach , T. Noda, W. Vandervorst*, S. Felch**, V. Parihar**, A. Cuperus**, R. McIntosh**, C. Vrancken*, E. Rosseel*, H. Bender*, B. Van Daele*, M. Niwa, H. Umimoto, R. Schreutelkamp**, P.P. Absil*, M. Jurczak*, K. De Meyer*, S. Biesemans*, T. Y. Hoffmann*, Matsushita Electric Industrial Co., Ltd, *IMEC, **Applied Materials	5:40	37.8 Toward Next High Performances MIM Generation: Up to 30fF/μm² with 3D Architecture and High-k Materials , S. Jeannot, A. Bajolet, J.-P. Manceau, S. Cremer, E. Deloffre, J.P. Oddou, C. Perrot, D. Benoit, C. Richard, P. Bouillon, S. Bruyere, STMicroelectronics	997
3:40 p.m.	36.6 Experimental and Theoretical Analysis of Dopant Diffusion and C Evolution in High-C Si:C Epi Layers: Optimization of Si:C Source and Drain Formed by Post-Epi Implant and Activation Anneal , Y. Cho, N. Zographos*, S. Thirupapuliyyur, and V. Moroz**, Applied Materials, *Synopsys Switzerland LLC, **Synopsys, Inc.		Session 38: Displays, Sensors, and MEMS - Imagers and Optical Detectors Wednesday, December 12, 1:30 p.m. Lincoln Room	
	Session 36: Modeling and Simulation - Simulation of Processes and Advanced Memories Wednesday, December 12, 1:30 p.m. Georgetown Ballroom	1:35 p.m.	38.1 A 0.5μm Pixel Frame-Transfer CCD Image Sensor in 110nm CMOS , K. Fife, A. El Gamal, H.-S.P. Wong, Stanford University	1003

2:00 p.m.

38.2 Development of a Production-Ready, Back-Illuminated CMOS Image Sensor with Small Pixels, T. Joy, S. Pyo*, S. Park*, C. Choi, C. Palsule, H. Han*, C. Feng, S. Lee*, J. McKee, P. Altice, C. Hong, C. Boemler, J. Hyncek, M. Louie, J. Lee*, D. Kim*, H. Haddad, B. Pain*, Magnachip Semiconductor America, *Magnachip Corp., **Jet Propulsion Lab

2:25 p.m.

38.3 Two-Transistor Active Pixel Sensor for High Resolution Large Area Digital X-ray Imaging, F. Taghibakhsh, K.S. Karim, Simon Fraser University

2:50 p.m.

38.4 Fully Implantable Retinal Prosthesis Chip with Photodetector and Stimulus Current Generator, T. Tanaka, K. Sato, K. Komiya, T. Kobayashi, T. Watanabe, T. Fukushima, H. Tomita, H. Kurino, M. Tamai, and M. Koyanagi, Tohoku University

3:15 p.m.

38.5 3 D Real-time CCD Imager Based on Background-Level-Subtraction Scheme, Y. Hashimoto, F. Kurihara, F. Tsunesada, K. Imai, Y. Takada, K. Taniguchi*, Matsushita Electric Works, Ltd., *Osaka University

3:40 p.m.

38.6 Potentiality of Silicon Optical Modulator Based on Free-Carrier Absorption, T. Tabei, T. Hirata, K. Kajikawa, H. Sunami, Hiroshima University

LATE NEWS

Session 6: Process Technology - Advanced Junctions, Silicides and Novel Stress Engineering

Monday, December 10, 1:30 p.m.

Jefferson Room

4:30 p.m.

6.8 Extendibility of NiPt Silicide Contacts for CMOS Technology Demonstrated to the 22-nm Node, K. Ohuchi, C. Lavoie*, C. Murray*, C. D'Emic*, I. Lauer*, J.O. Chu*, B. Yang**, P. Besser**, L. Gignac*, J. Bruley*, G.U. Singco*, F. Pagette*, A.W. Topol*, M.J. Rooks*, J.J. Bucchignano*, V. Narayanan*, M. Khare*, M. Takayanagi, K. Ishimaru, D.-G. Park*, G. Shahidi*, P. Solomon*, Toshiba America Electronic Components Inc., *IBM Corporation, **AMD

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Session 11: CMOS Devices - High Performance Devices

Tuesday, December 11, 9:00 a.m.

International Ballroom East

11:35 a.m.

11.7 (110) Channel, SiON Gate-Dielectric PMOS with Record High I_{on} =1 mA/ μ m Through Channel Stress and Source Drain External Resistance (R_{ext}) Engineering, B. Yang, A. Waite, H. Yin*, J. Yu*, L. Black, D. Chidambarrao*, A. Domenicucci*, X. Wang*, S.H. Ku*, Y. Wang*, H.V. Meer, B. Kim*, H. Nayfeh*, S.D. Kim*, K. Tabakman*, R. Pal, K. Nummy*, B. Grene*, P. Fisher, J. Liu*, Q. Liang*, J. Holt*, S. Nrasimha*, Z. Luo*, H. Utomo*, X. Chen*, D. Park*, C.Y. Sung*, R. Wachnik*, G. Freeman*, D. Schepis*, E. Maciejewski*, M. Khare*, E. Leobandung*, S. Luning, P. Agnello*, AMD, *IBM Systems and Technology Group

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11:50 a.m.

11.8 45nm SOI CMOS Technology with 3X Hole Mobility Enhancement and Asymmetric Transistor for High Performance CPU Application, S.K.H. Fung, H.C. Lo, C.F. Cheng, W.Y. Lu, K.C. Wu, K.H. Chen, D. H. Lee, Y.H. Liu, I.L. Wu, C.T. Li, C.H. Wu, F.L. Hisao, T. L. Chen, W.Y. Lien, C.H. Huang, P.W. Wang, Y.H. Chiu, L.T. Lin, K.Y. Chen, H.J. Tao, H.C. Tuan, Y.J. Mii, Y.C. Sun, TSMC

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Session 26: Quantum, Power, and Compound Semiconductor Devices - Ultra High Speed SiGe and InP-Based HBTs

Wednesday, December 12, 9:00 a.m.

International Ballroom West

11:35 a.m.

26.7 Ferrite-Partially-Filled On-Chip RF Inductor Fabricated Using Low-Temperature Nano-Powder-Mixed-Photoresist Filling Technique for Standard CMOS, C. Yang, F. Liu, T.-L. Ren, L.-T. Liu, G. Chen*, X.-K. Guan*, A. Wang**, Z.-X. Yue, Tsinghua University, *Illinois Institute of Technology, **University of California

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Session 34: CMOS Devices - Advanced Device Structures

Wednesday, December 12, 1:30 p.m.

International Ballroom Center

4:05 p.m.

34.7 High Performance 60nm Gate Length Germanium p-MOSFETs with Ni Germanide Metal Source/Drain, Y. Yamashita, M. Harada, N. Taoka*, K. Ikeda, K. Suzuki, O. Kiso*, N. Sugiyama, S.-I. Takagi*, MIRAI-ASET, *MIRAI-AIST

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