Surface Mount Technology Association

Pan Pacific Microelectronics Symposium and Tabletop Exhibition 2008

January 22-24, 2008 Kauai, Hawaii

Printed from e-media with permission by:

Curran Associates, Inc. 57 Morehouse Lane Red Hook, NY 12571 www.proceedings.com

ISBN: 978-1-60560-117-5

Some format issues inherent in the e-media version may also appear in this print version.

Copyright and Disclaimer

Pan Pacific Microelectronics Symposium and Tabletop Exhibition

INTERNATIONAL TECHNICAL EXCHANGE

ISBN: 978-1-60560-117-5

Reproduction rights for any of the technical papers included in these Proceedings are retained by the authors and/or their employers. Permission to reprint must be obtained from them and credit must be given to the "Pan Pacific Microelectronics Symposium" and these proceedings as the source.

The opinions expressed in these papers are those of the authors and are not necessarily those of SMTA. All papers are printed as submitted by the authors.

Additional copies of the Proceedings may be obtained by calling SMTA at (952) 920-7682, or by visiting the Bookstore at SMTA.org and placing your order securely on-line.

TABLE OF CONTENTS

Session TA1 Package on Package	
Process and Assembly Methods for Increased Yield of Package on Package Devices	1
Surface Mount Assembly Challenges for High Density PoP (Package-on-Package) Utilizing SoP (Solder-on-Pad) Technology	5
Joanna K. Wildhart, Panasonic Factory Solutions Company of America; Moody Dreiza, Amkor Technology Inc	•
Session TA2: Area Array	
μPILR™ Package Platform – A Higher Density Package-on-Package Innovation for Next Generation Electronics	14
Vern Solberg, Tessera, Inc.	
BGA Coplanarity Reduction During the Ball Attach Process Rick Lathrop, Hereaus Contact Materials Division	21
Session TP1: Stacked Die and TSV	
Market Drivers and Cost Analysis for 3D TSV Eric Mounier, Ph.D., Jérôme Baron, and Jean-Christophe Eloy, <i>Yole Development</i>	28
Cost Effective Copper TSV Interconnect Integration Paul Siblerud, Semitool, Inc.	32
Improvements to Through Silicon Vias or TSVs Phil Marcoux, TPL Group	34
Session TP2: Solderability	
Effects of Storage Environments on the Solderability of Nickel-Palladium-Gold Finish with Pb-Based a Pb-Free Solders	
Edwin Lopez, Paul Vianco, Samuel Lucero, and Carly George, Sandia National Laboratories	
Effect of Process Variations on Solder Joint Reliability for Nickel-Based Surface Finishes	50
Impact of Soldering Atmosphere on Solder Joint Formation Ursula Marquez de Tino and Denis Barbini, Vitronics Soltec; Wesley Enroth, Flextronics	57
Session TP1: Stacked Die and TSV (Continued)	
Technologies for 3D Heterogeneous Integration M. Juergen Wolf, Peter Ramm, and Herbert Reichl, Fraunhofer IZM	67
Precision Wafer to Wafer Packaging Using Eutectic Metal Bonding	74

	Advanced DRAM Si and Packaging Technology Status and Future Directions	. 80
	Update on the Evaluation of Stacked Die Packages Using Acoustic Micro Imaging	. 86
Ses	sion TP3: High Density Substrate Advances	
	HDI Via Architecture Effect on SiP Design Flexibility and Constraints Happy Holden, Mentor Graphics	. 91
	Sub-10µm Line/Space Technology on Organic Substrates for Next Generation System on Package (SoP) and Flip-Chip Packaging Venky Sundaram, Fuhan Liu, Hunter Chan, Mahadevan Iyer, and Rao Tummala, Georgia Institute of Technolog Hugh Roberts, Atotech USA Inc.	. 97
	Packaging Substrate Technologies Trend in Japan Henry H. Utsunomiya, Interconnection Technologies, Inc.	103
	Defect Structure and Failure Mechanism of PTH Electrodeposits	110
Key	note Presentation 1:	
	The Science and Engineering Workforce and National Security Robert A. Kavetsky, Energetics Technology Center; Davinder K. Anand, Ph.D., University of Maryland; Michael Marshall, Department of Navy (Retired)	115
Ses	sion WA1: Mechanical Integrity of Assemblies	
	Strength of Lead-Free BGA Spheres in High Speed Loading	127
	Experimental Approach to Analyze Failure Site Condition in Final Testing of BGA Package	134
	Development of Algorithm and Calculation Tool for Visco-Elastic Package Warpage	142
Ses	sion WA2: Degenerative Solder Effects	
	The Influence of the PWB Fabrication Electrodeposition Process on Copper Erosion During Wave Soldering	148
	Analyzing and Predicting Electrochemical Migration Failures on Field Failure Returns	169
	Effect of Thickness of Under-Bump-Metallization on the Electromigration Lifetime of Flip-Chip Solder Joints S.W. Liang and Chih Chen, National Chiao Tung University	176
_		
Ses	sion WA2: Degenerative Solder Effects (Continued)	
	Methodology to Characterize Pad Cratering Under BGA Pads in Printed Circuit Boards	182

Reflowing Treatments	180
C.C. Wei, P.C. Liu, and Chih Chen, <i>National Chiao Tung University;</i> Jeffrey C.B. Lee, <i>Integrated Service Technology,</i> P.C. Chen, <i>Advanced Semiconductor Engineering</i>	
Session WA3: Advanced Low I/O Packages	
Novel Wafer Level Packages Using Anisotropic Conductive Adhesives (ACPs) and NCPs for Flip-Ch	in
Assembly on Organic Substrates	
Kyung-Wook Paik, Il Kim, Ho-Young Son, and Chang-Kyu Chang, Korea Advanced Institute of Science and Technology	
Novel Leadframe-Based Package Provides Performance Boost for Hard Disk Drive Data Transfer Performance	201
Tim Olson, Amkor Technology; Bill Rugg, Seagate Technology	201
Session WP1: System/Subsystem Packaging	
A Novel Nano SMT Approach for WLSOP	205
P. Markondeya Raj, Gopal Jha, Gaurav Mehrotra, Janagama Goud, Mahadevan Iyer, and Rao Tummala, <i>Georgia Institute of Technology</i>	
Solderless Assembly and Interconnection of Electronic Packages	211
Development Status of an OCCAM Electronic Assembly Method	219
Edward S. Binkley, Ph. D. and Richard F. Otte, <i>PROMEX Industries Inc.</i>	
Embedded Passives – Uniformity and Reliability	226
Session WP2: Manufacturing Systems and Strategies	
Managing Electronics Manufacturing Business in China	233
Lean Manufacturing – Its Impact on Supply Chain	239
Apply MES Into PCBA Manufacturing Shop Floor Foundation of Advanced Production Model	243
Session WP3: System/Subsystem Reliability	
Electrostatic Discharge (ESD) and the Technology Roadmap to 2020 Hartmut Berndt, B.E.STAT European ESD Competence Centre	249
Life-Test Statistics for Small Sample Sizes Tom Clifford, Industry Consultant (formerly Lockheed-Martin)	257
Data Analysis Approach for System Reliability, Diagnostics and Prognostics Michael Pecht and Sachin Kumar, CALCE, University of Maryland	264
Session WP4: Solder Assembly Challenges	
A Study of Hand Soldering Tip Life on Lead-Free Alloys	273
Juthathip Fangkangwanwong, Jareerat Jintana, Jarinee Ketui, and Teng Hoon Ng, Celestica Thailand	

A Study of 0201's and Tombstoning in Lead-Free Systems	279
New Methods for Evaluating the Cleanliness Beneath Low Standoff Devices	288
Session THA1: Sensors and Sensor Networks	
Membrane Type Pressure Sensitive Sensor	293
Shape Analysis and Efficiency of Arrays of Microstrip Patch Antennas for Wireless Sensor Networks A. Gandelli, D. Monopoli, A. Pirisi, and R.E. Zich, <i>Politecnico di Milano</i>	298
Vibration Sensor for Wireless Condition Monitoring Maaike M.V. Taklo, Thor Bakke, Andreas Vogl, and Dag T. Wang, SINTEF ICT; Frank Niklaus, KTH-Royal Institute of Technology, Lennart Balgård, Automation Technologies Corporate Research	305
Session THA2: Reliability Enhancement	
Electrical and Thermal Interface Materials Rob Emery and Tanawan Chaowasakoo, Celestica Inc.	311
Thermal Management of Disk Drives Using Silicone-Free Thermal Interface Materials Bill Rugg, Seagate Technology; Radesh Jewram and Sanjay Misra, The Bergquist Company	319
Full Metal TIMs Ross Berntson, Indium Corporation	322
	326
Design and Optimization of a Multilayer Shield of Dielectric D. Monopoli, M. Mussetta, A. Gandelli, and R. Zich, <i>Politecnico di Milano</i>	320
	320
D. Monopoli, M. Mussetta, A. Gandelli, and R. Zich, <i>Politecnico di Milano</i>	