

2007 International Conference on Field-Programmable Technology

**Kitakyusyu, Japan
12-14 December 2007**



IEEE Catalog Number:
ISBN 10:
ISBN 13:

CFP07528-PRT
1-4244-1471-7
978-1-4244-1471-0

TABLE OF CONTENTS

Message from the General Chair	iii
Message from the Technical Program Chairs	v
Organizing Committee	vi
Technical Program Committee	vii
Additional Reviewers	ix
Keynote	x
Invited Talk	xi
Author Index	385

Session 1: Tools I

Memory Footprint Reduction For FPGA Routing Algorithms	1
<i>Scott Chin and Steve Wilton</i>	
SOC implementation of wave-pipelined circuits	9
<i>Seetharaman Gopalakrishnan and Venkataramani Balasubramanian</i>	
Self-characterization of Combinatorial Circuit Delays in FPGAs	17
<i>Justin S. J. Wong, Pete Sedcole and Peter Y. K. Cheung</i>	

Session 2: Applications I

FPGA Cluster Computing in the ETA Radio Telescope	25
<i>Cameron Patterson, Brian Martin, Steve Ellingson, John Simonetti and Sean Cutchin</i>	
FPGA-based Accelerator Design for RankBoost in Web Search Engines	33
<i>Ning-Yi XU, Xiong-Fei CAI, Rui GAO, Lei ZHANG and Feng-Hsiung HSU</i>	
Asymmetric Multi-Processor Architecture for Reconfigurable System-on-Chip and Operating System Abstractions	41
<i>Xin Xie, John Williams and Neil Bergmann</i>	
Design and Implementation of an FPGA Architecture for High-Speed Network Feature Extraction	49
<i>Sailesh Pati, Ramanathan Narayanan, Gokhan Memik, Alok Choudhary and Joseph Zambreno</i>	

Session 3: Architecture

Architecting Hard Crossbars on FPGAs and Increasing their Area-Efficiency with Shadow Clusters	57
<i>Peter Jamieson and Jonathan Rose</i>	
A Method and FPGA Architecture for Real-Time Polymorphic Reconfiguration	65
<i>Jason Paul, Samuel Stone, Yong Kim and Robert Bennington</i>	

Reconfigurable Functional Units for Scientific Superscalar Processors	73
<i>Jonathan Evans, Kyle Rupnow and Katherine Compton</i>	

A COARSE GRAINED RECONFIGURABLE ARCHITECTURE FOR VARIABLE BLOCK SIZE MOTION ESTIMATION	81
<i>Ruchika Verma and Ali Akoglu</i>	

Session 4: Tools II

Instrumented Multi-Stage Word-Length Optimization	89
<i>William Osborne, Jose Coutinho, Ray Cheung, Wayne Luk and Oskar Mencer</i>	
A Domain Specific Language for Reconfigurable Path-based Monte Carlo Simulations . .	97
<i>David Barrie Thomas and Wayne Luk</i>	
Fused-Arithmetic Unit Generation for Reconfigurable Devices using Common Subgraph Extraction	105
<i>Alastair Smith, George Constantinides and Peter Cheung</i>	
Unifying FPGA Hardware Development	113
<i>Jacob Alexis Bower, Wei Ning Cho and Wayne Luk</i>	

Session 5: Applications II

Applying Cuckoo Hashing for FPGA-based Pattern Matching in NIDS/NIPS	121
<i>Tran Ngoc Thinh, Surin Kittitornkun and Shigenori Tomiyama</i>	
HIGH PERFORMANCE HARDWARE IMPLEMENTATION OF SPIKEPROP LEARNING: POTENTIAL AND TRADEOFFS	129
<i>Marco Aurelio Nuno-Maganda, Miguel Arias-Estrada and Cesar Torres-Huitzil</i>	
The Image Forest Transform Architecture	137
<i>F.A. Nabio Augusto Cappabianco, Guido Ara Nzjo and Alexandre Falc Nco</i>	
A HIGHLY PARALLEL FPGA BASED IEEE-754 COMPLIANT DOUBLE-PRECISION BINARY FLOATING-POINT MULTIPLICATION ALGORITHM	145
<i>Sandeep Venishetti and Ali Akoglu</i>	

Session 6: Memory & IP Protection

TAS-MRAM based Non-volatile FPGA logic circuit	153
<i>Weisheng ZHAO, Eric BELHAIRE, Bernard DIENY, Guillaume PRENAT and Claude CHAPPERT</i>	
Bitstream Decompression for High Speed FPGA Configuration from Slow Memories . . .	161
<i>Dirk Koch, Christian Beckhoff and Juergen Teich</i>	
Dynamic Intellectual Property Protection for Reconfigurable Devices	169
<i>Tim G.A. Nlneysu, Bodo M. Nvller and Christof Paar</i>	

Session 7: Applications III

Hardware/Software Co-design of a General-Purpose Computation Platform in Particle Physics	177
<i>Ming Liu, Wolfgang Kuehn, Zhonghai Lu, Axel Jantsch, Shuo Yang, Tiago Perez and Zhenan Liu</i>	
Efficient and High-Throughput Implementations of AES-GCM on FPGAs	185
<i>Gang Zhou, Harald Michalik and Lasloz Hinsenkamp</i>	
A Framework for Implementing a Network-Based Stochastic Biochemical Simulator on an FPGA	193
<i>Masato Yoshimi, Yuri Nishikawa, Toshinori Kojima, Yasunori Osana, Akira Funahashi,</i>	

An Approach for Applying Large Filters on Large Images using FPGA	201
<i>Shingo Kawada and Tsutomu Maruyama</i>	

Session 8: Tools III

Run-Time Management of Reconfigurable Hardware Tasks using Embedded Linux . . .	209
<i>Krzysztof Kościuszkiewicz, Fearghal Morgan and Krzysztof Kępa</i>	
Implementations of Reconfigurable Logic Arrays on FPGAs	217
<i>Tsutomu Sasao and Hiroki Nakahara</i>	
Net Length Based Routability Driven Packing	225
<i>Audip Pandit and Ali Akoglu</i>	

Poster Session I

FPGA-based Streaming Computation for Lattice Boltzmann Method	233
<i>Kentaro Sano, Oliver Pell, Wayne Luk and Satoru Yamamoto</i>	
Reconfigurable Hardware Module Sequencer - A Tradeoff Between Networked and Data Flow Architectures	237
<i>Kai-Jung Shih, Chin-Chieh Hung, and Pao-Ann Hsiung</i>	
An Embedded Reconfigurable Logic Core based on Variable Grain Logic Cell Architecture	241
<i>Yoshiaki Satou, Motoki Amagasaki, Hiroshi Miura, Kazunori Matsuyama, Ryoichi Yamaguchi, Masahiro Iida and Toshinori Sueyoshi</i>	
Improving bounds for FPGA Logic Minimization	245
<i>Tim Todman, Haohan Fu, Oskar Mencer and Wayne Luk</i>	
Floating-Point Matrix Multiplication in a Polymorphic Processor	249
<i>Georgi K. Kuzmanov and Wouter M. van Oijen</i>	
A Secure Digital Content Delivery System Based on Partially Reconfigurable Hardware . .	253
<i>Yohei Hori, Hiroyuki Yokoyama, Hirofumi Sakane and Kenji Toda</i>	
Productivity Of High-Level Languages On Reconfigurable Computers: An HPC Perspective .	257
<i>Esam El-Araby, Preetham Nosum and Tarek El-Ghazawi</i>	
A Systolic Algorithm for the Quadratic Assignment Problem and its FPGA Implementation . .	261
<i>Yoshihiro Kimura, Shin'ichi Wakabayashi and Shinobu Nagayama</i>	
Reconfiguration performance analysis of a dynamic optically reconfigurable gate array architecture	265
<i>Daisaku Seto and Minoru Watanabe</i>	

Poster Session II

Efficient Mesh of Tree Interconnect for FPGA Architecture	269
<i>ZIED MARRAKCHI, HAYDER MRABET, CHRISTIAN MASSON and HABIB MEHREZ</i>	
Overwrite Configuration Technique in Multicast Configuration Scheme for Dynamically Reconfigurable Processor Arrays	273
<i>Satoshi Tsutsumi, Vasutan Tunbunheng, Yohei Hasegawa, Adepu Parimala, Takuro Nakamura, Takashi Nishimura and Hideharu Amano</i>	
AN FPGA Based Traveling-Wave Fault Location System	277
<i>David P Coggins, David W P Thomas, Barrie R Hayes-Gill and Yiqun Zhu</i>	
NICFlex: A Functional Verification Accelerator for An RTL NIC Design	281
<i>Xianyang Jiang, Xiaomin Li, Yue Tian and Kai Wang</i>	

Power Configurable Block Array Connected in Series as First Prototype Flex Power FPGA Chip	285
<i>Masakazu Hioki, Takashi Kawanami, Yohei Matsumoto, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa and Hanpei Koike</i>	
Optimal Buffering of FPGA Interconnect for Expected Delay optimization	289
<i>Yi-Ru He and Wai-Kei Mak</i>	
FPGA-Based 3-D engine for high-speed 3-D measurement based on light section method .	293
<i>Yachide Yusuke, Makoto Ikeda and Kunihiro Asada</i>	
A 62.5 ns holographic reconfiguration for an optically differential reconfigurable	297
gate array	
<i>Mao Nakajima and Minoru Watanabe</i>	
Recursive Variable Expansion: A Loop Transformation for Reconfigurable Systems	301
<i>Zubair Nawaz, Ozana Silvia Dragomir, Thomas Marconi, Elena Moscu Panainte, Koen Bertels and Stamatis Vassiliadis</i>	

Poster Session III

A Rapid Prototyping of Real-Time Pattern Generator for Step-and-Scan Lithography Using Digital Micromirror Device	305
<i>Naoto Miyamoto, Masahiko Shimakage, Tatsuo Morimoto, Kazuya Kadota, Shigetoshi Sugawa and Tadahiro Ohmi</i>	
High Performance Software-Hardware Network Intrusion Detection System	309
<i>Ryan Proudfoot, Kenneth B. Kent, Eric Aubanel, and Nan Chen</i>	
A Domain-Specific Dynamically Reconfigurable Hardware Platform for Wireless Sensor Networks	313
<i>Heiko Hinkelmann, Peter Zipf and Manfred Glesner</i>	
FPGA implementation of a statically reconfigurable Java environment for embedded systems	317
<i>Shinsuke Nino, Takayuki Mori, YoungHun Ko, Yuichiro Shibata and Kiyoshi Oguri</i>	
A Dynamically Reconfigurable Architecture Combining Pixel-Level SIMD and Operation-Pipeline Modes for High Frame Rate Visual Processing	321
<i>Nao Iwata, Shingo Kagami and Koichi Hashimoto</i>	
A BALANCED VECTOR-QUANTIZATION PROCESSOR ELIMINATING REDUNDANT CALCULATION FOR REAL-TIME MOTION PICTURE COMPRESSION	325
<i>Masahiro Konda, Takahiro Nakayama, Naoto Miyamoto and Tadahiro Ohmi</i>	
Real-time Segmentation of Color Images based on K-Means Clustering on FPGA	329
<i>Takashi Saegusa and Tsutomu Maruyama</i>	
A PORTABLE MEMORY ACCESS FRAMEWORK FOR HIGH-PERFORMANCE RECONFIGURABLE COMPUTERS	333
<i>Miaoqing Huang, Ivan Gonzalez and Tarek El-Ghazawi</i>	
The Spiral Search: A Linear Complexity Algorithm for the Generation of Convex Multiple Input Multiple Output Instruction-Set Extensions	337
<i>Carlo Galuzzi, Koen Bertels and Stamatis Vassiliadis</i>	
A Case for Soft Vector Processors in FPGAs	341
<i>Jason Yu and Guy Lemieux</i>	
A Portable Co-Verification System Which Generates Transactor and Testbench Automatically	345
<i>Takahito Nakajima, Shigeru Namiki, Shuhei Kinoshita and Naohiko Shimizu</i>	