

Proceedings of the

IEEE 2008

INTERNATIONAL

INTERCONNECT TECHNOLOGY

CONFERENCE

Hyatt Regency Hotel
Burlingame, CA

June 2-4, 2008

The IITC is sponsored by the IEEE Electron Devices Society, whose goal is to provide a forum for professionals in semiconductor processing, academia and equipment development to present and discuss exciting new science and technology; and Semiconductor International is the media sponsor.

SESSION 1: PLENARY SESSION

Co-Chairs: Gary W. Ray, *Intel Corp.*
Kuniko Kikuta, *NEC Electronics Corp.*
Ivo Raaijmakers, *ASM International nv*

- | | | |
|-----|---|---|
| 1.1 | Keynote Presentation: Zero Defects – Reliability for Automotive Electronics , Dr. Valentin von Tils, Vice President, ASIC Platform Development, Robert Bosch GmbH, Reutlingen, Germany | 1 |
|-----|---|---|

SESSION 2: 3-D SILICON

Co-chairs: Mike Shapiro, *IBM*
and Young-Chang Joo, *Seoul National University*

- | | | |
|-----|---|----|
| 2.1 | INVITED: Through-Silicon Via Technologies for Extreme Miniaturized 3D Integrated Wireless Sensor Systems (e-CUBES) , P. Ramm and A. Klumpp, Fraunhofer Institute for Reliability and Microintegration, Dresden, Germany | 7 |
| 2.2 | INVITED: Three-Dimensional Integration Technology Using Self-Assembly Technique and Super Chip Integration , M. Koyanagi, T. Fukushima and T. Tanaka, Tohoku University, Sendai, Japan | 10 |
| 2.3 | A 3D-IC Technology with Integrated Microchannel Cooling , D. Sekar, C. King, B. Dang*, T. Spencer, H. Thacker**, P. Joseph, M. Bakir, and J. Meindl, Georgia Institute of Technology, Atlanta, GA, *IBM Research and **Nanonexus, Inc. | 13 |
| 2.4 | Extraction of the Appropriate Material Property for Realistic Modeling of Through-Silicon-Vias using μ-Raman Spectroscopy , C. Okoro, Y. Yang, B. Vandeveld, B. Swinnen, D. Vandepitte*, B. Verlinden*, and I. De Wolf, IMEC, Leuven, Belgium and *Katholieke Universiteit, Leuven, Belgium | 16 |
| 2.5 | Resistance to Electromigration of Purely Intermetallic Micro-Bump Interconnections for 3D-Device Stacking , R. Labie, W. Ruythooren, K. Baert, E. Beyne, and B. Swinnen, IMEC, Leuven, Belgium | 19 |

SESSION 3: POSTER I

- | | | |
|-----|--|----|
| 3.1 | High Performance Cu Containing Ru or RuN_x for Barrierless Metallization , J.P. Chu and C.H. Lin*, National Taiwan University of Science and Technology, Taipei, Taiwan and *Chin-Min Institute of Technology, Tou-Fen, Taiwan | 25 |
| 3.2 | Development and Optimization of Porous pSiCOH Interconnect Dielectrics for 45 nm and Beyond , A. Grill, S. Gates, C. Dimitrakopoulos, V. Pagel, S. Cohen, Y. Ostrovski, E. Liniger, E. Simonyi, D. Restaino* S. Sankaran*, S. Reiter**, A. Demos**, K.S. Yim**, V. Nguyen**, J. Rocha**, and D. Ho**, IBM – TJ Watson Research Center, Yorktown Heights, NY, *IBM Semiconductor Research & Development Center, Hopewell Junction, NY and **Applied Materials, Santa Clara, CA | 28 |

3.3	Mechanistic Study of CO₂ Plasma Damage to OSG Low k Dielectrics, H. Shi, J. Bao, H. Huang, B. Chao, S. Smith, Y. Sun, P.S. Ho, A. Li*, M. Armacost*, and D. Kyser*, University of Texas, Austin, TX and *Applied Materials, Sunnyvale, CA	31
3.4	A Self-Aligned Air Gap Interconnect Process, H-W. Chen, S-P. Jeng, H-Y. Tsai, Y-W. Liu, CH. Yu and YC. Sun, Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan	34
3.5	Production Worthy 3D Interconnect Technology, H.J. Tu, W.J. Wu, J.C. Hu, K.F Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan. Yang, H.B. Chang, W.C. Chiou, and C.H. Yu, Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan	37
3.6	3D IC Process Integration Challenges and Solutions, K. Powell, S. Burgess, T. Wilby, R. Hundman, and J. Callahan*, Aviza Technology, Newport, UK and *Cubic Wafer, Merrimack, NH	40
3.7	Current-carrying Capacity of Carbon Nanofiber Interconnects, H. Kitsuki, T. Saito, T. Yamada, D. Fabris, J.R. Jameson, P. Wilhite, M. Suzuki, and C.Y. Yang, Santa Clara University, Santa Clara, CA	43
3.8	3D Die-to-wafer Cu/Sn Microconnects formed simultaneously with an Adhesive Dielectric Bond using Thermal Compression Bonding, S. Pozder, A. Jain, R. Chatterjee, Z. Huang, R.E. Jones, E. Acosta, B. Marlin*, G. Hillmann**, M. Sobczak [^] , G. Kreindl ^{^^} , S. Kanagavel [^] , H. Kostner**, and S. Pargfrieder ^{^^} , Freescale Semiconductor, Inc., Austin, TX, *Freescale Semiconductor, Inc., Chandler, AZ, **Datacon Technology GmbH, Radfeld, Austria, [^] Cookson Electronics Semiconductor Products, Suwanee, GA and ^{^^} EV Group, Scharding, Austria	46
3.9	Voltage Ramp and Time-Dependent Dielectric Breakdown in Ultra-Narrow Cu/SiO₂ Interconnects, H. Park, H.-B. Lee, H.-K. Jung, Z.-S. Choi, J.-Y. Bae, J.-W. Hong, K.-I. Choi, B.-L. Park, E.-J. Lee, J.-W. Kim, J.-M. Lee, G.-H. Choi, and J.-T. Moon, Samsung Electronics Co., Ltd., Korea	49
3.10	Key Factors to Sustain the Extension of a MHM-based Integration Scheme to Medium and High Porosity PECVD Low-k Materials, Y. Travaly, J. Van Aelst, V. Truffert, P. Verdonck, T. Dupont, E. Camerotto, O. Richard, H. Bender, C. Kroes, D. De Roest*, G. Vereecke, M. Claes, Q.T. Le, E. Kesters, M. Van Cauwenberghe*, J. Beynet*, S. Kaneko**, H. Struyf, M. Baklanov, K. Matsushita**, N. Kobayashi**, H. Sprey*, and G. Beyer, IMEC, Leuven, Belgium, *ASM Belgium, Leuven, Belgium, **ASM Japan, Tokyo, Japan	52
3.11	Highly Reliable Low Resistance Cu Contact using Novel CVD Ru/TiN/Ti Stacked Liner, M. Kitamura, K. Nomura, H. Matsumori, T. Watanabe, H. Matsuyama, J.H. Wada, T. Usui, and M. Hasunuma, Toshiba Corporation, Tokyo, Japan	55

- | | | |
|------|--|----|
| 3.12 | Analytical Study of Leakage Characteristics Change during Multilevel Interconnect Process using Porogen-type Porous SiOC (k=2.4)/Cu System , N. Ohashi, J. Nakahira, E. Soda, K. Tomioka, S. Chikaki, N. Oda, S. Kondo, and S. Saito, Semiconductor Leading Edge Technologies, Inc., Ibaraki, Japan | 58 |
| 3.13 | Copper Direct Bonding for 3D Integration , P. Gueguen, L. Di Cioccio, M. Rivoire*, D. Scevola, M. Zussy, Charvet, L. Bally, D. Lafond, and L. Clavelier, CEA Leti – MINATEC, Grenoble, France and * STMicronics, Crolles, France | 61 |

SESSION 4: MATERIALS AND PROCESSING I

Co-chairs: Ivo Raijmakers, *ASM International*
and Kuniko Kikuta, *NEC Electronics*

- | | | |
|-----|--|----|
| 4.1 | INVITED: Process Control and Physical Failure Analysis for Sub-100nm Cu/Low-k Structures , E. Zschech, R. Huebner, P. Potapov, I. Zienert, M. A. Meyer, D. Chumakov, H. Geisler, M. Hecker, H-J. Engelmann, and E. Langer, AMD Saxony LLC and Co., KG, Dresden, Germany | 67 |
| 4.2 | INVITED: Lithography Options and Challenges for Sub-45nm Node Interconnect Layers , M. Maenhoudt, IMEC, Leuven, Belgium | 70 |
| 4.3 | Structure-Designable Formation-Method of Super Low-k SiOC Film (k=2.2) by Neutral-Beam-Enhanced-CVD , S. Yasuhara, J. Chung, K. Tajima*, H. Yano*, S. Kadomura*, M. Yoshimaru*, N. Matsunaga*, T. Kuybota, H. Ohtake, and S. Samukawa, Tohoku University, Sendai, Japan and *Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan | 73 |
| 4.4 | Micro Beam IR Characterization of Narrow Width (-100 nm) Low-k Spaces Between Cu Lines with Valence EELS Evaluation , S. Ogawa, H. Seki*, Y. Otsuka*, S. Nakao, Y. Takigawa, and H. Hashimoto*, Semiconductor Leading Edge Technologies, Inc., Ibaraki, Japan and *Toray Research Center, Shiga, Japan | 76 |
| 4.5 | On the Elements of High Throughput Cu-CMP Slurries Compatible with Low Step Heights , T. Kanki, T. Shirasu*, S. Takesako*, M. Sakamoto*, A.A. Asneil*, N. Idani*, T. Kimura, T. Nakamura, and M. Miyajima*, Fujitsu Laboratories Ltd., Tokyo, Japan and *Fujitsu Ltd., Mie and Tokyo, Japan | 79 |
| 4.6 | Hybrid e-CMP/CMP Process with Non-Contact Electrode Pad , S. Kondo, D. Abe*, T. Enomoto*, S. Tominaga*, K. Yamada, and S. Saito, Semiconductor Leading Edge Technologies, Inc. Ibaraki, Japan and *Roki Techno Co., Ltd., Tokyo, Japan | 82 |

SESSION 5: MATERIALS AND PROCESSING II

Co-chairs: Michael Armacost, *Applied Materials*
and Vincent Arnal, *STMicroelectronics*

- 5.1 **INVITED: Post-Etch Cleaning for Porous Low-k Integration: Impact of HF Wet Etch on "Pore-Sealing and "k recovery"**, L. Broussous, W. Puyrenier, D. Rebiscoul*, V. Rouessac**, and A. Ayrat**, STMicroelectronics, Crolles, France, *LETI/CEA, Grenoble, France and **Institut European des Membranes, Montpellier, France 87
- 5.2 **INVITED: Progress, Opportunities and Challenges in Modeling of Plasma Etching**, Y. Yang, M. Wang and M.J. Kushner, Iowa State University, Ames, IA 90
- 5.3 **Enhancing Yield and Reliability by Applying Dry Organic Acid Vapor Cleaning to Copper Contact Via-Bottom for 32-nm Nodes and Beyond**, H. Kudo, K. Ishikawa, M. Nakaishi*, A. Tsukune, S. Ozaki, Y. Nakata, S. Akiyama*, Y. Mizushima, M. Hayashi, A.A. Akbar*, T. Kouno, H. Iwata, Y. Iba, T. Ohba**, T. Futatsugi, T. Nakamura, and T. Sugii, Fujitsu Laboratories, Ltd. and *Fujitsu Ltd., Akiruno, Japan and **University of Tokyo, Tokyo, Japan 93
- 5.4 **ALD Growth of a Mixed-Phase Novel Barrier for Seedless Copper Electroplating Applications**, S. Kumar, H.L. Xin*, P. Ercius*, D.A. Muller* and E. Eisenbraun, and The University at Albany-SUNY, Albany, NY and * Cornell University, Ithaca, NY 96
- 5.5 **Effects of Ru-Ta Alloy Barrier on Cu Filling and Reliability for Cu Interconnects**, K. Mori, K. Ohmori, N. Torazawa*, S. Hirao*, S. Kaneyama*, H. Korogi*, K. Maekawa, S. Fukui, K. Tomita, M. Inoue, H. Chibahara, Y. Imai, N. Suzumura, K. Asai, and M. Kojima, Renesas Technology Corp., Hyogo, Japan and *Matsushita Electric Industrial Co., Ltd., Kyoto, Japan 99
- 5.6 **Amorphous Ru / Polycrystalline Ru Highly Reliable Stacked Layer Barrier Technology**, S. Ogawa, N. Tarumi, M. Abe, M. Shiohara, H. Imamura, and S. Kondo, Semiconductor Leading Edge Technologies, Inc., Ibaraki, Japan 102
- 5.7 **INVITED: CMOS Compatibility of Carbon Nanotubes**, W.I. Milne, X. Wang, Y. Zhang, S. Haque, S.M. Kim, F. Udrea, J. Robertson, and K.B.K. Teo, Cambridge University, Cambridge, UK 105

SESSION 6: RELIABILITY I

Co-chairs: Tomoji Nakamura, *Fujitsu Labs.*
and Maureen Brongo, *Skyworks Solutions*

- 6.1 **INVITED: Low-k Dielectric Reliability: Impact of Test Structure Choice, Copper and Integrated Dielectric Quality**. Zs. Tokei, Y.-L. Li, I. Ciofi, K. Croes, and G.P. Beyer, IMEC, Leuven, Belgium 111

6.2	Blech Effect and Lifetime Projection for Cu/Low-K Interconnects , C. Christiansen, B. Li and J. Gill*, IBM Systems & Technology Group, Essex Junction, VT and *Hopewell Junction, NY	114
6.3	Further Enhancement of Electro-migration Resistance by Combination of Self-aligned Barrier and Copper Wiring Encapsulation Techniques for 32-nm Nodes and Beyond , H. Kudo, M. Haneda, T. Tabira, M. Sunayama, N. Ohtsuke, N. Shimizu, H. Ochimizu, T. Tsukune, T. Suzuki, H. Kitada, S. Amari*, H. Matsuyama*, T. Owada*, H. Watantani*, T. Futatsugi, T. Nakamura, and T. Sugii, Fujitsu Laboratories, Ltd. and *Fujitsu Ltd., Akiruno, Japan	117

SESSION 7: POSTER II

7.1	Integration Aspects of CoWP Capping Layers for Electromigration Enhancement , A. Preusse, R. Seidel, O. Aubel, M. Nopper, B. Freudenberg, M. Schaller, M. Fecher, T. Letz, C. Bartsch, A. Ott, M. Friedemann, F. Feustel, M.A. Meyer, and P. Limbecker, AMD, Dresden, Germany	123
7.2	Investigation of the Impact of CoWP Self-aligned Barrier Deposition on the Porous SiOC Properties after a Direct CMP Process , S. Gall, S. Olivier, M. Assous, M. Bernard, P.H. Hasumesser, C. Jayet, S. Maitrejean, K. Hamioud*, V. Arnal*, and G. Passemard*, CEA-LETI-MINATEC, Grenoble, France and *STMicroelectronics, Crolles, France	126
7.3	Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers using Deep Trench Isolation , K. Minoglou, K. De Munck, D.S. Texcan, T. Borgers, W. Ruythooren, J. Bogaerts*, I.F. Veltroni** I. Zayer [^] , R. Meynart [^] , J-L. Bezy [^] , C. Van Hoof, and P. De Moor, IMEC, Leuven, Belgium, *CMOSIS, Antwerp, Belgium, **Galileo Avionica, Florence, Italy, and [^] ESA-ESTEC, Noordwijk, The Netherlands	129
7.4	Interconnect for Out-of-Plane MEMS Assembly , A.A.A. Aarts, H.P. Neves, R.P. Puers*, and C. Van Hoof, IMEC, Leuven, Belgium and *KULeuven, Leuven, Belgium	132
7.5	Impact of Process Induced Stresses and Chip-Packaging Interaction on Reliability of Air-gap Interconnects , X. Zhang, S-K. Ryu, R. Huang, P.S. Ho, J. K. Liu*, and D. Toma*, The University of Texas, Austin, TX and *Tokyo Electron US Holdings, Austin, TX	135
7.6	Measurements and Circuit Model of Carbon Nanofibers at Microwave Frequencies , R. R. Madriz, J.R. Jameson, S. Krishnan, K. Gleason, Z. Sun, and C.Y. Yang, Santa Clara University, Santa Clara, CA	138
7.7	Resistivity Size Effect in Encapsulated Cu Thin Films , T. Sun, B. Yao, A. Warren, V. Kumar*, K. Barmak*, and K.R. Coffee, University of Central Florida, Orlando, FL and *Carnegie Mellon University, Pittsburgh, PA	141

7.8	Benchmarking of Metal-to-Carbon Nanotube Side Contact Resistance, Z. Liu, L. Ci, N. Bajwa, Ajayan, and J-Q. Lu, Rensselaer Polytechnic Institute, Troy, NY	144
7.9	Integration of Low Resistive CVD-W Interconnects for sub-50nm FEOL Application, C-H. Kim, I-C. Rho, K-B. Rouh, K-Y. Lim, Y-S. Kim, J-C. Ku, Y-S. Sohn, H-S. Kang, and H-J. Kim*, Hynix Semiconductor, Inc., Kyoungki- do, Korea and *Seoul National University, Seoul, Korea	147
7.10	Investigation of Interconnect Design on Chip Package Interaction and Mechanical Reliability of Cu/Low-k Multi-Layer Interconnects in Flip Chip Package, C.J. Uchibori, X. Zhang, P.S. Ho*, and T. Nakamura**, Fujitsu Labs., America, Sunnyvale, CA, *University of Texas, Austin, TX and **Fujitsu Labs., Ltd., Kanagawa, Japan	150
7.11	Realization of Via Interconnects based on Carbon Nanotubes, J.C. Coiffic, M. Fayolle, H. Le Poche, S. Maitrejean, and S. Olivier, CEA-LETI- MINATEC, Grenoble, France and *CEA-LITEN, Grenoble, France	153
7.12	Plasma Enhanced Atomic Layer Deposition of Ru-Ta Composite Film as a Seed Layer for CVD Cu Filling, D. Jeoung, H. Inoue, and H. Shinriki, ASM Japan, Tokyo, Japan	156
7.13	An Evaluation of Electrografted Copper Seed Layers for Enhanced Metallization of Deep TSV Structures, S. Ledain, C. Bunel, P. Mangaigalli*, A. Carles*, N. Frederich**, E. Delbos**, L. Omnes**, and A. Etchberry^, NXP Semiconductors, Colombelles, France, *Alchimer S.A., Massy, France, **OM Broup, Saint Fromond, France, and ^University de Versailles, Versailles, France	159

SESSION 8: RELIABILITY II

Co-chairs: Scott List, SRC
and Shinichi Ogawa, SELETE

8.1	Copper Line Resistance Control and Reliability Improvement by Surface Nitridation of Ti barrier Metal, A. Sakata, S. Kato, Y. Yano, H. Toyoda, T. Kawanoue, M. Hatano, J. Wada, N. Yamada, T. Oki, H. Yamaguchi, N. Nakamura, K. Higashi, M. Yamada, T. Fujimake, and M. Hasunuma, Toshiba Corp., Yokohama, Japan	165
8.2	TDDDB Kinetics and their Relationship with the E- and $\sqrt{E}$-models, K-Y. Yiang, H.W. Yao and A. Marathe, Advanced Micro Devices, Inc. Sunnyvale, CA	168
8.3	Quantitative Roadmap for Optimizing CMP of Ultra-Low-k Dielectrics, T-S. Kim, T. Konno*, T. Yamanaka*, and R.H. Dauskardt, Stanford University, Stanford, CA and *JSR Micro, Inc., Sunnyvale, CA	171
8.4	Impact of LER and Misaligned Vias on the Electric Field in Nanometer- Scale Wires, M. Stucchi and Z. Tokei, IMEC, Leuven, Belgium	174

- 8.5 **Limitation of Low-k Reliability due to Dielectric Breakdown at Vias**, S.-C. Lee, A.S. Oates and K.M. Chang*, Taiwan Semiconductor Manufacturing Co., Hsinchu, Taiwan, ROC and *National Chiao Tung University, Hsinchu, Taiwan, ROC 177

SESSION 9: SYSTEM-ON-CHIP

Co-chairs: Hector Sanchez, *Freescale Semiconductor*
and Gary Ray, *Intel Corporation*

- 9.1 **INVITED: Performance Benchmarking for Graphene Nanoribbon, Carbon Nanotube, and Cu Interconnects**, A. Naeemi and J.D. Meindl, Georgia Institute of Technology, Atlanta, GA 183
- 9.2 **Crosstalk Analysis Method of 3-D Solenoid On-chip Inductors for High-speed CMOS SoCs**, K. Hijoka, A. Tanabe, Y. Amamiya, and Y. Hayashi, NEC Corp., Kanagawa, Japan 186

SESSION 10: PROCESS INTEGRATION I

Co-chairs: Didier Louis, *CEA-LETI*
and Toshiaki Hasegawa, *Sony Corp.*

- 10.1 **INVITED: A Multi-level Cu/Low-K/Airgap BEOL Technology**, S. Nitta, D. Edelstein, S. Ponoth*, L. Clevenger**, X. Liu, and T. Standaert**, IBM T.J. Watson Research Center, Yorktown Heights, NY, *IBM Research at Albany Nanotech, Albany, NY and **IBM Systems and Technology Group, Hopewell Junction, NY 191
- 10.2 **Cost-effective Air-gap Interconnects by All-in-One Post-Removing Process**, N. Nakamura, N. Matsunaga, T. Kaminatsui, K. Watanabe, and H. Shibata, Toshiba Corp., Yokohama, Japan 193
- 10.3 **300 mm Multi Level Air Gap Integration for Edge Interconnect Technologies and Specific High Performance Applications**, R. Gras, F. Gaillard*, D. Bouchu*, A. Farcy, E. Petiprez, B. Icard*, J.C. Le-Denmat, L. Pain*, J. Bustos, P.H. Hausmesser*, P. Brun*, G. Imbert, L. Clement, C. Brorwiak, M. Rivoire, E. Euvrad*, V. Arnal, S. Olivier*, S. Moreau*, M. Mellier, T. Chevolleau**, G. Passemard, and J. Torres, STMicroelectronics, Crolles, France, *CEA-LETI-MINATEC, Grenoble, France and **CNRS-LTM, Grenoble, France 196
- 10.4 **Self Aligned CuGeN Process for 32/22nm Nodes and Beyond**, C.S. Liu, H.C. Chen, T.I. Bao, J. VanOlmen*, K. Croes*, E. VanBesien*, M. Pantouvaki*, C. Zhao*, E. Sleenckx*, G. Beyer*, and C.H. Yu, Taiwan Semiconductor Manufacturing Co., Hsinchu, Taiwan and *IMEC, Leuven, Belgium 199
- 10.5 **Ti-based Barrier for Cu Interconnect Applications**, W. Wu, H.-J. Wu, G. Dixit, R. Shaviv, M. Gao, T. Mountsier, G. Harm, A. Dulkan, N. Fuchigami, S.K. Kailasam, E. Klawuhn, and R.H. Havemann, Novellus Systems, Inc., San Jose, CA 202

- 10.6 Highly-Reliable Low-Resistance Cu Interconnects with PVD-Ru/Ti Barrier Metal toward Automotive LSIs**, M. Tagami, N. Furutake, S. Saito, and Y. Hayashi, NEC Corp., Kanagawa, Japan **205**
- 10.7 Robust BEOL Process Integration with Ultra Low-k (k=2.0) Dielectric and Self-Formed MnO_x Barrier Technology for 32 nm-node and Beyond**, T. Watanabe, Y. Hayashi, H. Tomizawa, T. Usui, A. Gawase, M. Shimada, K. Watanabe, and H. Shibata, Toshiba Corp., Yokohoma, Japan **208**

SESSION 11: PROCESS INTEGRATION II

Co-chairs: Shin-Puu Jeng, *TSMC*
and J.D. Luttmer, *University of North Texas*

- 11.1 INVITED: High Volume Manufacturing Issues for On-Die Interconnects at the 45nm Process Node**, P. Moon, Intel LTD (Logic Technology Development) Hillsboro, Oregon **213**
- 11.2 Low-K Interconnect Stack with Thick Metal 9 Redistribution Layer and Cu Die Bump for 45nm High Volume Manufacturing**, D. Ingerly, S. Agraharam, D. Becher, V. Chikarmane, K. Fischer, R. Grover, M. Goodner, S. Haight, J. He, T. Ibrahim, S. Joshi, H. Kotheri, K. Lee, Y. Lin, C. Litteken, H. Liu, E. Mays, P. Moon, T. Mule, S. Nolen, N. Patel, S. Pradhan, J. Robinson, P. Ramanarayanan, S. Sattiraju, T. Schroeder, S. Williams, and P. Yashar, Intel Corp., Hillsboro, OR **216**
- 11.3 INVITED: Phase Change Memory**, M.J. Breitwisch, IBM T.J. Watson Research Center, Yorktown Heights, NY **219**
- 11.4 Quantitative Analysis of Correlation between Insulator Surface Copper Contamination and TDDb Lifetime based on Actual Measurement**, D. Oshida, T. Takewaki, M. Iguchi, T. Taiji, T. Morita, Y. Tsuchiya, H. Tsuchiya, S. Yokogawa, H. Kunishima, H. Aizawa, and N. Okada, NEC Electronics Corp., Kanagawa, Japan **222**
- 11.5 Low-Temperature Plasma-Oxidation Process for Reliable Tantalum-Oxide (TaO) Decoupling Capacitors**, I. Kume, N. Inoue, T. Toda*, M. Furumiya*, T. Takeuchi, F. Ito, T. Iwaki*, S. Shida*, and Y. Hayashi, NEC Corp. and *NEC Electronics, Kanagawa, Japan **225**

SESSION 12: NOVEL MATERIALS AND PROCESSES

Co-chairs: Dorel Toma, *Tokyo Electron US Holdings*
and Johann Bartha, *Technical University Dresden*

- 12.1 INVITED: Germanium on Silicon Modulators and Nanometallic-Enhanced Detectors for Optical Interconnects**, D.A.B. Miller, Stanford University, Stanford, CA **231**
- 12.2 Sub-ps Delay Through Multi-Wall Carbon Nanotube Local Interconnects in a CMOS Integrated Circuit**, G.F. Close, S. Yasuda*, B. Paul**, S. Fujita*, and H-S. P. Wong, Stanford, CA, *Toshiba Corp., Kawasaki, Japan and **Toshiba America Research, San Jose, CA **234**

- 12.3 Robustness of CNT Via Interconnect Fabricated by Low Temperature Process over a High-Density Current**, A. Kawabata, S. Sato, T. Nozue, T. Huakshima, M. Norimatsu, M. Mishima, T. Murakama, D. Kondo, K. Asano, M. Ohfuti, H. Kawarada*, T. Sakai, M. Nihei, and Y. Awano, MIRAI-Selete, Atsugi, Japan and *Waseda University, Tokyo, Japan

237