

**Proceedings**

**2008 IEEE International Conference**

**on**

**Integrated Circuit Design and Technology**

**Minatec Grenoble, France**  
**June 2<sup>nd</sup> – June 4<sup>th</sup>, 2008**

**Sponsored by:**



# Table of Content

## Session A     Advanced Transistor Structure, Architecture and Process

|                                                                                                                                                                                                                                                                                                                                                                                                          |    |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Invited Paper: Silicon-On-Nothing (SON) Applications for Low Power Technologies<br><i>S.Monfray, F.Boeuf, P.Coronel, G.Bidal, S.Denorme, T.Skotnicki;<br/>STMicroelectronics, France</i>                                                                                                                                                                                                                 | 1  |
| Evaluation of Ultra Thin Body Si-On-ONO (UTB SOONO) Transistors Using Ultra Thin Spacer Technology<br><i>Hyun Jun Bae, Sung Hwan Kim, Sung In Hong, Yong Lack Choi, Ho Ju Song, Chang Woo Oh, Dong-Won Kim, Donggun Park*, KyungSeok Oh, Won-Seong Lee;<br/>Advanced Technology Development Team 1, DPA Team*, R&amp;D Center, Samsung Electronics Co., Korea</i>                                        | 5  |
| New Charge Trapping Phenomena in Recessed-Channel-Array-Transistor (RCAT) after Fowler-Nordheim Stress<br><i>Sung-Young Lee, Se Geun Park, Samjin Hwang, Jaeun Jeon, Wonshik Lee;<br/>DRAM QA, Samsung Electronics Co., Korea</i>                                                                                                                                                                        | 9  |
| Use of the p-floating shielding layer for improving electric field concentration of the recessed gate<br><i>Sang Jun Hwang*, Seung Woo Yu*, Jae In Lee*, Ey-Goo Kang+, Man Young Sung*;<br/>*Department of Electrical Engineering, Korea University, Anam-Dong, Seongbuk-Gu, Seoul 136-701, Korea, +Department of Information Technology, Far East University, Uemsung-gun, Chung-buk 369-851, Korea</i> | 13 |

## Session B1     RF & AMS

|                                                                                                                                                                                                                                                |    |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Invited Paper: CMOS SOI technology for WPAN. Application to 60Ghz LNAs<br><i>A. Siligaris*, C. Mounet*, B. Reig*, P. Vincent*, A. Michel+;<br/>*CEA-LETI, +ANSOFT, France</i>                                                                  | 17 |
| A 0.5 V Area-Efficient Transformer Folded-Cascode Low-Noise Amplifier in 90 nm CMOS<br><i>Takao Kihara, Hae-Ju Park, Isao Takobe, Fumiaki Yamashita, Toshimasa Matsuoka, Kenji Taniguchi;<br/>Osaka University, Japan</i>                      | 21 |
| A Low Power Multi-band Selector DLL with Wide-Locking Range<br><i>Ko-Chi Kuo, Yi-Hsi Hsu;<br/>National Sun Yat-sen University, Taiwan</i>                                                                                                      | 25 |
| Design of a Current Steering CMOS D/A Converter with an Adaptive Control Switch and a Novel Layout Technique<br><i>Junho Moon, Sanghoon Hwang, Daeyoon Kim, Heewon Kang, Seungjin Yeo, Doobock Lee, Minkyu Song; Dongguk University, Korea</i> | 29 |

## Session B2 Low Power

### Invited Paper: 3D-Structured On-Chip Buck Converter for Distributed Power Supply System in SiPs 33

*Makoto Takamiya<sup>\*,+</sup>, Kohei Onizuka<sup>+</sup>, Takayasu Sakurai<sup>+</sup>;*

*<sup>\*</sup>VLSI Design and Education Center, University of Tokyo, Japan*

*<sup>+</sup>Institute of Industrial Science, University of Tokyo, Japan*

### Invited Paper: A Localized Power Control Mixing Hopping and Super Cut-Off Techniques within a GALS NoC 37

*Edith Beigné, Fabien Clermidy, Sylvain Miermont, Yvain Thonnart, Alexandre Valentian, Pascal Vivet; CEA-LETI, MINATEC, France*

### Improvement of Power Supply Rejection Ratio of LDO Deteriorated by Reducing Power Consumption 43

*Socheat Heng, Cong-Kha Pham;*

*Department of Electronic Engineering, the University of Electro-Communications, Tokyo, JAPAN*

### An Innovative sub-32nm SRAM Current Sense Amplifier in Double-Gate CMOS Insensitive to Process Variations and Transistor Mismatch 47

*Adam Makosiej<sup>\*</sup>, Piotr Nasalski<sup>\*</sup>, Bastien Giraud<sup>+</sup>, Andrei Vladimirescu<sup>+,#</sup>, Amara Amara<sup>+</sup>;*

*<sup>\*</sup>Technical University of Lodz, Poland,*

*<sup>+</sup>ISEP, France,*

*<sup>#</sup>Berkeley Wireless Research Center, USA*

### SRAM Memory Cell Leakage Reduction Design Techniques in 65nm Low Power PD-SOI CMOS 51

*Olivier Thomas<sup>\*</sup>, Marc Belleville<sup>\*</sup>, Richard Ferrant<sup>+</sup>;*

*<sup>\*</sup>CEA, France– Minatec, Grenoble, France*

*<sup>+</sup>STMicroelectronics Crolles, France*

### Which is the Best Dual-Port SRAM in 45-nm Process Technology? – 8T, 10T Single End, and 10T Differential – 55

*Hiroki Noguchi<sup>\*</sup>, Shunsuke Okumura<sup>\*</sup>, Yusuke Iguchi<sup>\*</sup>, Hidehiro Fujiwara<sup>\*</sup>, Yasuhiro Morita<sup>\*</sup>, Koji Nii<sup>\*,+</sup>, Hiroshi Kawaguchi<sup>\*</sup>, Masahiko Yoshimoto<sup>\*</sup>;*

*<sup>\*</sup>Kobe University, Japan*

*<sup>+</sup>Renesas Technology Corporation, Japan*

## Session C1 Advanced Transistor Structure, Architecture and Process

### Invited Paper: Low-voltage 6T FinFET SRAM cell with high SNM using HfSiON/TiN gate stack, fin widths down to 10nm and 30nm gate length 59

*N. Collaert<sup>\*</sup>, K. von Arnim<sup>+</sup>, R. Rooyackers<sup>\*</sup>, T. Vandeweyer<sup>\*</sup>, A. Mercha<sup>\*</sup>, B. Parvais<sup>\*</sup>, L. Witters<sup>\*</sup>, A. Nackaerts<sup>†</sup>, E. Altamirano Sanchez<sup>\*</sup>, M. Demand<sup>\*</sup>, A. Hikavy<sup>\*</sup>, S. Demuyne<sup>\*</sup>, K. Devriendt<sup>\*</sup>, F. Bauer<sup>+</sup>, I. Ferain<sup>\*,#</sup>, A. Veloso<sup>\*</sup>, K. De Meyer<sup>\*,#</sup>, S. Biesemans<sup>\*</sup>, M. Jurczak<sup>\*</sup>;*

*<sup>\*</sup>IMEC, Belgium*

*<sup>+</sup>Infineon Technologies, Germany.*

*<sup>#</sup>K. U. Leuven, Belgium*

*<sup>†</sup>NXP-TSMC Research Center, Heverlee, Belgium*

### Independent-Gate Four-Terminal FinFET SRAM for Drastic Leakage Current Reduction 63

*Kazuhiko Endo, Shin-ichi O'uchi, Yuki Ishikawa, Yongxun Liu, Takashi Matsukawa, Kunihiro Sakamoto, Meishoku Masahara, Junichi Tsukada, Kenichi Ishii, Eiichi Suzuki;*

*National Institute of AIST, Japan*

|                                                           |    |
|-----------------------------------------------------------|----|
| A Study of LBO Effects in a 40 nm SA-MSCFET               | 67 |
| <i>Jyi-Tsong Lin, Yi-Chuen Eng &amp; Shiang-Shi Kang;</i> |    |
| <i>National Sun Yat-Sen University, Taiwan</i>            |    |

|                                                                                                                                                                   |    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| A New Edge Termination Technique to Improve Voltage Blocking Capability and Reliability of Field Limiting Ring for Power Devices                                  | 71 |
| <i>Yo Han Kim<sup>*</sup>, Han Sin Lee<sup>*</sup>, Sin su Kyung<sup>*</sup>, Young Mok Kim<sup>*</sup>, Ey Goo Kang<sup>+</sup>, Man Young Sung<sup>*</sup>;</i> |    |
| <i>Korea University, Korea</i>                                                                                                                                    |    |
| <i><sup>+</sup>Far East University, Korea</i>                                                                                                                     |    |

|                                                                                              |    |
|----------------------------------------------------------------------------------------------|----|
| An SOI-based Self-aligned Quasi-SOI MOSFET with $\Pi$ -shaped Semiconductor Conductive Layer | 75 |
| <i>Yi-Chuen Eng, Jyi-Tsong Lin, Shiang-Shi Kang;</i>                                         |    |
| <i>National Sun Yat-Sen University, Taiwan</i>                                               |    |

## **Session C2 Reliability**

|                                                                                           |    |
|-------------------------------------------------------------------------------------------|----|
| Invited Paper: Reliability of Advanced Embedded Non-Volatile Memories: The 2T-FNFN Device | 79 |
| <i>Guoqiao Tao;</i>                                                                       |    |
| <i>NXP, The Netherlands</i>                                                               |    |

|                                                    |    |
|----------------------------------------------------|----|
| Invited Paper: SOI Chip Design and Charging Damage | 83 |
| <i>Terence B. Hook;</i>                            |    |
| <i>IBM, USA</i>                                    |    |

|                                                                                                                         |    |
|-------------------------------------------------------------------------------------------------------------------------|----|
| Invited Paper: TDDDB and BTI Reliabilities of High-k Stacked Gate Dielectrics - Impact of Initial Traps in High-k Layer | 87 |
| <i>Kenji Okada<sup>*</sup>, Hiroyuki Ota<sup>+</sup>, Toshihide Nabatame<sup>+</sup>, Akira Toriumi<sup>++</sup>;</i>   |    |
| <i><sup>*</sup>Matsushita Electric Industrial Co., Ltd.</i>                                                             |    |
| <i><sup>+</sup>MIRAI-ASET, Japan</i>                                                                                    |    |
| <i><sup>++</sup>The University of Tokyo, Japan.</i>                                                                     |    |

|                                                                                                                                                  |    |
|--------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Invited Paper: Reliability Issues for Nano-scale CMOS Dielectrics: - From Transistors to Product Reliability - From SiON to High-K dielectrics - | 91 |
| <i>G. Ribes, M. Rafik, D. Roy, J.M. Roux;</i>                                                                                                    |    |
| <i>ST microelectronics, France</i>                                                                                                               |    |

|                                                                                                                      |    |
|----------------------------------------------------------------------------------------------------------------------|----|
| Threshold Voltage Shift Instability Induced by Plasma Charging Damage in MOSFETs with High-k Dielectric              | 97 |
| <i>K. Eriguchi<sup>*</sup>, M. Kamei<sup>*</sup>, K. Okada<sup>+</sup>, H. Ohta<sup>*</sup>, K. Ono<sup>*</sup>;</i> |    |
| <i><sup>*</sup>Kyoto University, Japan</i>                                                                           |    |
| <i><sup>+</sup>MIRAI-ASET, Japan</i>                                                                                 |    |

|                                                                                                                        |     |
|------------------------------------------------------------------------------------------------------------------------|-----|
| Analysis of Si Substrate Damage Induced by Inductively Coupled Plasma Reactor with Various Superposed Bias Frequencies | 101 |
| <i>Y. Nakakubo, A. Matsuda, M. Kamei, H. Ohta, K. Eriguchi, K. Ono;</i>                                                |     |
| <i>Kyoto University, Japan</i>                                                                                         |     |

## Session D1 RF & AMS

- Low-Power High Precision Integrated Nanostructure with Superior-Order Curvature-Corrected Logarithmic Core 105  
*Cosmin Popa;*  
*UPB, Romania*
- Metal Gate Effects on a 32nm Metal Gate Resistor 109  
*Thuy Dao, Ik\_Sung Lim, Larry Connell, Dina H. Triyoso, Youngbog Park & Charlie Mackenzie;*  
*Freescale Semiconductor, USA*
- Design of a 6-bit 1GSPS Fully Folded CMOS A/D Converter For Ultra Wide Band (UWB) Applications 113  
*Doobock Lee, Seungjin Yeo, Heewon Kang, Daeyoon Kim, Junho Moon, Minkyu Song;*  
*Dongguk University, Korea*
- An Integrated Class D Audio Amplifier based on Sliding Mode Control 117  
*Remy Cellier, Gael Pillonnet, Nacer Abouchi, Monique Chiollaz;*  
*CPE Lyon/INL, France*
- Comparative analysis of two operational amplifier topologies for a 40MS/s 12-bit pipelined ADC in 0.35 $\mu$ m CMOS 121  
*Jose-Angel Diaz-Madrid\*, Harald Neubauer\*, Gines Domenech-Asensi+, Ramon Ruiz+;*  
*\*Fraunhofer IIS ICD-A, Germany*  
*+Universidad Politecnica de Cartagena, Spain*

## Session D2 System Level Technology Assessment & Low Power

- Invited Paper: Virtual Design for Technology Exploration - a process design integration methodology for a fabless entity - 125  
*Christopher Chun, Jose Corleto, Matt Nowak, Riko Radojcic;*  
*Qualcomm, USA*
- Invited Paper: Technology development driven by design 131  
*Axel Nackaerts;*  
*NXP Semiconductor Belgium NV, Belgium*
- A low power 12-bit and 30-MS/s pipeline analog to digital converter in 0.35 $\mu$ m CMOS 135  
*Fatah Rarbi\*, Daniel Dzahini+;*  
*\*PSI Electronics company*  
*+LPSC - IN2P3, Université Joseph Fourier,INPG, France*
- Sleep Circuit for SRAM Core with Improved Noise Margin 139  
*Piyush Jain, Jitendra Dasani, Ashish Kumar;*  
*STMicroelectronics Pvt Ltd.Greater Noida, India*
- Low Power Clocking strategies in Deep Submicron Technologies 143  
*M. Samy Hosny\*, Yuejian Wu+;*  
*\*SiliconPro Inc, Canada*  
*+Nortel Networks, Canada*
- Energy Delay Optimization Methodology for Current-Mode Signaling for On-Chip Interconnects 147  
*Astria Nur Irfansyah\*, Saeid Nooshabadi+, Torsten Lehmann\*;*  
*\*University of New South Wales, Australia,*  
*+Gwangju Institute of Science and Technology, Korea*

## Session E DFM/DFT/DFY/DFR

- Invited Paper: Overview of DFT Features of the Sun Microsystems Niagara2 CMP/CMT SPARC Chip 151  
*Tom Ziaja, Murali Gala;*  
*Sun Microsystems, USA,*
- Invited Paper: Energy-Efficient and Metastability-Immune Timing-Error Detection and Recovery Circuits for Dynamic Variation Tolerance 155  
*Keith A. Bowman, James W. Tschanz, Nam Sung Kim, Janice C. Lee, Chris B. Wilkerson, Shih-Lien L. Lu, Tanay Karnik, Vivek K. De;*  
*Intel, Hillsboro, OR, USA*
- Process Variability-Induced Timing Failures — A Challenge in Nanometer CMOS Low-Power Design 159  
*Xiaonan Zhang, Xiaoliang Bai;*  
*Qualcomm, USA*
- Ring Oscillator Circuit Structures for Measurement of Isolated NBTI/PBTI Effects 163  
*Jae-Joon Kim\*, Rahul Rao\*, Saibal Mukhopadhyay\*, Ching-Te Chuang#;*  
*\*IBM, Yorktown Heights, USA,*  
*+Georgia Institute of Technology, USA,*  
*#National Chiao-Tung University, Taiwan*
- A Comparative Study of Variability Impact on Static Flip-Flop Timing Characteristics 167  
*B. Rebaud\*, M. Belleville\*, C. Bernard\*, M. Robert+, P. Maurine+, N. Azemard+;*  
*\*CEA-LETI MINATEC, France,*  
*+LIRMM - CNRS - Université Montpellier II, France*
- Analyzing the Effect of Process Variation to Reduce Parametric Yield Loss 171  
*H. Ramakrishnan, S. S. Shedabale, G. Russell, A. Yakovlev;*  
*Newcastle University, UK*

## Session F Advanced Memory Devices

- Invited Paper: Low-Voltage Limitations and Challenges of Nano-Scale CMOS LSIs -A Personal View of Memory Designer- 177  
*Kiyoo Itoh;*  
*Fellow Hitachi, Japan*
- Invited Paper: New writing mechanism for reliable SONOS embedded memories with thick tunnel oxide 181  
*Michiel van Duuren, Nader Akil, Mohamed Boutchich, Dušan S. Golubović;*  
*NXP-TSMC Research Center, Belgium*
- Invited Paper: Read and Write Circuit Assist Techniques for Improving Vccmin of Dense 6T SRAM Cell 185  
*Muhammad M. Khellah, Ali Keshavarzi, Dinesh Somasekhar, Tanay Karnik, Vivek De;*  
*Circuits Research Lab, Intel Corp, USA*
- Invited Paper: The Future of Flash Memory: is Floating Gate Technology Doomed to Lose The Race? 189  
*Dirk Wellekens, Jan Van Houdt;*  
*IMEC, Belgium*

|                                                                                                                                                                                                           |     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| SONOS Memories with Embedded Silicon Nanocrystals in Nitride by In-situ Deposition Method                                                                                                                 | 195 |
| <i>Yi-Hong Wu<sup>*</sup>, Tsung-Yu Chiang<sup>+</sup>, Sheng-Hsien Liu<sup>*</sup>, Wen-Luh Yang<sup>*</sup>, Tien-Sheng Chao<sup>+</sup>, Fun-Tat Chin<sup>*</sup>;</i>                                 |     |
| <i><sup>*</sup>Feng Chia University, Taichung, Taiwan</i>                                                                                                                                                 |     |
| <i><sup>+</sup>National Chiao Tung University, Hsinchu, Taiwan</i>                                                                                                                                        |     |
| Temperature-Based Phase Change Memory Model for Pulsing Scheme Assessment                                                                                                                                 | 199 |
| <i>Yi-Bo Liao, Jun-Tin Lin, Meng-Hsueh Chiang;</i>                                                                                                                                                        |     |
| <i>National Ilan University, Taiwan</i>                                                                                                                                                                   |     |
| Ultra-high Bandwidth Memory with 3D-stacked Emerging Memory Cells                                                                                                                                         | 203 |
| <i>Keiko Abe<sup>*</sup>, Mihir P. Tendulkar<sup>+</sup>, John R. Jameson<sup>#</sup>, Peter B. Griffin<sup>+</sup>, Kumiko Nomura<sup>*</sup>, Shinobu Fujita<sup>*</sup>, Yoshio Nishi<sup>+</sup>;</i> |     |
| <i><sup>*</sup>Toshiba Corporation, Japan</i>                                                                                                                                                             |     |
| <i><sup>+</sup>Stanford University, USA</i>                                                                                                                                                               |     |
| <i><sup>#</sup>Santa Clara University</i>                                                                                                                                                                 |     |

## Session G      Advanced Materials

|                                                                                                                                                                                                                                                |     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Invited Paper: Transconductance Enhancement of Si Nanowire Transistors By Oxide-Induced Strain                                                                                                                                                 | 207 |
| <i>A. Seike<sup>*</sup>, T. Tange<sup>*</sup>, I. Sano<sup>*</sup>, Y. Sugiura<sup>*</sup>, I. Tsuchida<sup>*</sup>, H. Ohta<sup>*</sup>, T. Watanabe<sup>*</sup>, D. Kosemura<sup>+</sup>, A. Ogura<sup>+</sup>, I. Ohdomari<sup>*</sup>;</i> |     |
| <i><sup>*</sup>Waseda University, Japan</i>                                                                                                                                                                                                    |     |
| <i><sup>+</sup>Meiji University, Japan</i>                                                                                                                                                                                                     |     |
| A new analytical model for predicting SWCNT band-gap from geometrical properties                                                                                                                                                               | 211 |
| <i>Karim El Shabrawy, Koushik Maharatna, Darren M Bagnall, Bashir M Al-Hashimi;</i>                                                                                                                                                            |     |
| <i>ECS Southampton University, UK</i>                                                                                                                                                                                                          |     |
| FPGA design based Implementation of ICA algorithm for real time Blind Signal Separation                                                                                                                                                        | 215 |
| <i>M. Ounas<sup>*</sup>, R. Touhami<sup>*</sup>, S. Chitroub<sup>*</sup>, M.C.E. Yagoub<sup>+</sup>;</i>                                                                                                                                       |     |
| <i><sup>*</sup>USTHB University, Algeria</i>                                                                                                                                                                                                   |     |
| <i><sup>+</sup>School of Information Technology and Engineering, Canada</i>                                                                                                                                                                    |     |
| Probabilistic Modeling of Nanoscale Adder                                                                                                                                                                                                      | 219 |
| <i>Xiaojun Lu<sup>*</sup>, Jianping Li<sup>*</sup>, Guowu Yang<sup>*</sup>, Xiaoyu Song<sup>+</sup>;</i>                                                                                                                                       |     |
| <i><sup>*</sup>University of Electronic Science and Technology, China</i>                                                                                                                                                                      |     |
| <i><sup>+</sup>Portland State University, Oregon, USA</i>                                                                                                                                                                                      |     |
| A model for calculations of effective ion charges in microcircuit interconnects                                                                                                                                                                | 223 |
| <i>Tariel Makhviladze, Mikhail Sarychev, Yuri Zhitnikov;</i>                                                                                                                                                                                   |     |
| <i>Institute of Physics and Technology, Russian Federation</i>                                                                                                                                                                                 |     |

## Session H      Soft Error Rate

|                                                                                             |     |
|---------------------------------------------------------------------------------------------|-----|
| Invited Paper: Building a Reliable Internet Core Using Soft Error Prone Electronics         | 227 |
| <i>Allan L. Silburt, Adrian Evans, Ana Burghilea, Shi-Jie Wen, Ron Norrish, Dean Hogle;</i> |     |
| <i>Cisco Systems, USA</i>                                                                   |     |

|                                                                                                                     |     |
|---------------------------------------------------------------------------------------------------------------------|-----|
| Real-Time Neutron and Alpha Soft-Error Rate Testing of CMOS 130nm SRAM:<br>Altitude versus Underground Measurements | 233 |
|---------------------------------------------------------------------------------------------------------------------|-----|

*J.L. Autran<sup>\*o</sup>, P. Roche<sup>+</sup>, S. Sauze<sup>\*</sup>, G. Gasiot<sup>+</sup>, D. Munteanu<sup>\*</sup>, P. Loaiza<sup>#</sup>, M. Zampaolo<sup>#</sup>, J. Borel<sup>†</sup>;*

*<sup>\*</sup>Aix-Marseille University, CNRS and IM2NP, France*

*<sup>+</sup>STMicroelectronics, France*

*<sup>#</sup>LSM, CEA-CNRS, France*

*<sup>†</sup>JB R&D, France*

*<sup>o</sup>University Institute of France (IUF), France*

*●ASTEP platform, France*

|                                                              |     |
|--------------------------------------------------------------|-----|
| Traces of Errors due to Single Ion in Floating Gate Memories | 237 |
|--------------------------------------------------------------|-----|

*G. Cellere<sup>\*</sup>, A. Paccagnella<sup>\*</sup>, A. Visconti<sup>+</sup>, M. Bonanomi<sup>+</sup>, R. Harboe-Sørensen<sup>#</sup>, A. Virtanen<sup>†</sup>;*

*<sup>\*</sup>Univ. Padova, Italy*

*<sup>+</sup>STMicroelectronics, Italy*

*<sup>#</sup>European Space Agency, ESTEC, Netherlands*

*<sup>†</sup>University of Jyväskylä, Finland*

## Session I      SoC/MPSoC/SIP, IC & Platform Design & Process

|                                                           |     |
|-----------------------------------------------------------|-----|
| Invited Paper: 3D Contactless Communication for IC Design | 241 |
|-----------------------------------------------------------|-----|

*Roberto Canegallo<sup>\*</sup>, Luca Ciccarelli<sup>\*</sup>, Federico Natali<sup>+</sup>, Alberto Fazzi<sup>+</sup>, Roberto Guerrieri<sup>+</sup>, Pierluigi Rolandi<sup>\*</sup>;*

*<sup>\*</sup>STMicroelectronics Central CAD and Design Solutions, Italy,*

*<sup>+</sup>ARCES-University of Bologna, Italy*

|                            |     |
|----------------------------|-----|
| Integration of SAW Filters | 245 |
|----------------------------|-----|

*Tarak Hdihi, Hassene Mnif, Mourad Loulou;*

*National Engineering School of Sfax, Tunisia*

|                                                            |     |
|------------------------------------------------------------|-----|
| Invited Paper: Dynamic Measurement of Critical-Path Timing | 249 |
|------------------------------------------------------------|-----|

*Alan J. Drake<sup>\*</sup>, Robert M. Senger<sup>\*</sup>, Harmander Singh<sup>+</sup>, Gary D. Carpenter<sup>\*</sup>, Norman K. James<sup>\*</sup>;*

*<sup>\*</sup>IBM Austin Research Lab, USA*

*<sup>+</sup>AMD, USA*

|                                                                                                               |     |
|---------------------------------------------------------------------------------------------------------------|-----|
| Invited Paper: Key Considerations Given to the Design of a Next Generation Multi-core Communications Platform | 253 |
|---------------------------------------------------------------------------------------------------------------|-----|

*Dac C. Pham*

*Freescale Semiconductor, Austin, TX*

|                                                                                         |     |
|-----------------------------------------------------------------------------------------|-----|
| Invited Paper: On-Chip Circuit for Measuring Jitter and Skew with Picosecond Resolution | 257 |
|-----------------------------------------------------------------------------------------|-----|

*K. A. Jenkins<sup>\*</sup>, Z. Xu<sup>+</sup>, A.P. Jose<sup>+</sup>, K.L. Shepard<sup>†</sup>;*

*<sup>\*</sup>IBM USA,*

*<sup>+</sup>Columbia University, USA*

## Session J      Emerging Technology

|                                                                                              |     |
|----------------------------------------------------------------------------------------------|-----|
| Invited Paper: New State Variable Device Opportunities for Beyond CMOS: A System Perspective | 261 |
|----------------------------------------------------------------------------------------------|-----|

*Victor V. Zhirnov<sup>\*</sup>, Ralph K. Cavin<sup>\*</sup>, and George I. Bourianoff<sup>+</sup>;*

*<sup>\*</sup>Semiconductor Research Corporation, USA*

*<sup>+</sup>Intel Corporation, USA*



|                                                                                                                                                                                                            |     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Invited Paper: 3D Multichannels and stacked nanowires Technologies for New Design opportunities in Nanoelectronics                                                                                         | 265 |
| <i>T. Ernst*, E. Bernard*, C. Dupré*, A. Hubert*, S. Bécu*, B. Guillaumot*, O. Rozeau*, O. Thomas*, P. Coroneil*, J.-M. Hartmann*, C. Vizioz*, N. Vulliet*, O. Faynot*, T. Skotnicki*, S. Deleonibus*;</i> |     |
| <i>*CEA-LETI, Minatec, France</i>                                                                                                                                                                          |     |
| <i>+STMicroelectronics, France</i>                                                                                                                                                                         |     |
| Invited Paper: Device Architectures based on Graphene Channels                                                                                                                                             | 269 |
| <i>M. Baus, T.J. Echtermeyer, B.N. Szafranek, M.C. Lemme, H. Kurz;</i>                                                                                                                                     |     |
| <i>AMO GmbH, Germany</i>                                                                                                                                                                                   |     |
| A simple compact model to analyze the impact of ballistic and quasi-ballistic transport on ring oscillator performance                                                                                     | 273 |
| <i>S. Martinie*, G. Le Carval*, D. Munteanu+, M.-A. Jaud, J.L. Autran*#;</i>                                                                                                                               |     |
| <i>*CEA-LETI MINATEC, France</i>                                                                                                                                                                           |     |
| <i>+IM2NP-CNRS, France.</i>                                                                                                                                                                                |     |
| <i>#Institut Universitaire de France (IUF), Paris, France</i>                                                                                                                                              |     |
| A 3-Tier, 3-D FD-SOI SRAM Macro                                                                                                                                                                            | 277 |
| <i>Aamir Zia, Philip Jacob, Russell P. Kraft, John F. McDonald;</i>                                                                                                                                        |     |
| <i>Rensselaer Polytechnic Institute, USA</i>                                                                                                                                                               |     |
| 3D CMOS Integration: Introduction of Dynamic coupling and Application to Compact and Robust 4T SRAM                                                                                                        | 281 |
| <i>P.Batude*, M.-A.Jaud*, O.Thomas*, L.Clavelier*, A.Pouydebasque*, M.Vinet*, S.Deleonibus*, A.Amara*;</i>                                                                                                 |     |
| <i>*CEA/LETI-MINATEC, France</i>                                                                                                                                                                           |     |
| <i>+ISEP, France</i>                                                                                                                                                                                       |     |
| <b>Session K CAD</b>                                                                                                                                                                                       |     |
| A Generic Method for Variability Analysis of Nanoscale Circuits                                                                                                                                            | 285 |
| <i>Saibal Mukhopadhyay;</i>                                                                                                                                                                                |     |
| <i>Georgia Institute of Technology, USA</i>                                                                                                                                                                |     |
| Stochastic Analysis for Crosstalk Noise of Coupled interconnects with Process Variations                                                                                                                   | 289 |
| <i>Xin Li*, Janet M. Wang+, Weiqing Tang#, Huizhong Wu*;</i>                                                                                                                                               |     |
| <i>*Nanjing University of Science and Technology, China</i>                                                                                                                                                |     |
| <i>+University of Arizona, USA</i>                                                                                                                                                                         |     |
| <i>#Institute of Computing Technology of Chinese Academy of Sciences, China</i>                                                                                                                            |     |
| A Novel Moment-Based Methodology For Accurate And Efficient Static Timing Analysis                                                                                                                         | 293 |
| <i>Ahmed Shebaita*, Dusan Petranovic+, Yehea Ismail*;</i>                                                                                                                                                  |     |
| <i>*Northwestern University, USA</i>                                                                                                                                                                       |     |
| <i>+Mentor Graphics, USA</i>                                                                                                                                                                               |     |
| How Does Inversed Temperature Dependence Affect Timing Sign-off                                                                                                                                            | 297 |
| <i>Sean H. Wu**, Alexander Tetelbaum*, Li-C. Wang*;</i>                                                                                                                                                    |     |
| <i>*LSI Corporation, USA</i>                                                                                                                                                                               |     |
| <i>+University of California Santa Barbara, USA</i>                                                                                                                                                        |     |
| Statistical Leakage Modeling in CMOS Logic Gates Considering Process Variations                                                                                                                            | 301 |
| <i>Carmelo D'Agostino*, Philippe Flatresse*, Edith Beigne+, Marc Belleville*;</i>                                                                                                                          |     |
| <i>*STMicroelectronics Crolles, FTM/DAIS</i>                                                                                                                                                               |     |
| <i>+CEA-LETI Grenoble, MINATEC</i>                                                                                                                                                                         |     |

*A. Noiré<sup>\*</sup>, S. Bergeon<sup>+</sup>, A. Olliver<sup>\*</sup>, Y. Courant<sup>+</sup>;*

*<sup>\*</sup>STMicroelectronics, France*

*<sup>+</sup>Infiniscale, France*