

Proceedings

**Eighth International Workshop  
on Microprocessor Test  
and Verification  
MTV 2007**

5-6 December 2007  
Austin, Texas, USA

Sponsored by  
IEEE Computer Society Test Technology Technical Council  
IBM  
Freescale Semiconductor Inc.



Los Alamitos, California  
Washington • Tokyo



Eighth International Workshop on  
Microprocessor Test and Verification

MTV 2007

## TABLE OF CONTENTS

Preface  
Acknowledgment  
Committees

### POWER ANALYSIS

<b>Assertion-Based Modal Power Estimation</b> .....	1
<i>Sumit Ahuja, Deepak A. Mathaikutty, Sandeep Shukla, Ajit Dingankar</i>	
<b>Early Models for System-Level Power Estimation</b> .....	6
<i>Dam Sunwoo, Hassan Al-Sukhni, Jim Holt, Derek Chiou</i>	
<b>Reduction of Power Dissipation during Scan Testing by Test Vector Ordering</b> .....	13
<i>Wang-Dauh Tseng, Lung-Jen Lee</i>	

### FORMAL METHODS

<b>Mechanized Certification of Secure Hardware Designs</b> .....	20
<i>Sandip Ray, Warren A. Hunt_Jr.</i>	
<b>Application of Lifting in Partial Design Analysis</b> .....	28
<i>Marc Herbstritt, Vanessa Struve, Bernd Becker</i>	
<b>Model Checking Bluespec Specified Hardware Designs</b> .....	34
<i>Gaurav Singh, Sandeep K. Shukla</i>	
<b>Runtime Verification of k-Mutual Exclusion for SoCs</b> .....	39
<i>Selma Ikiz, Alper Sen</i>	
<b>A Scalable Symbolic Simulator for Verilog RTL</b> .....	46
<i>Sasidhar Sunkari, Supratik Chakraborty, Vivekananda Vedula, Kailasnath Maneparambil</i>	

### SYSTEM LEVEL VALIDATION AND TEST

<b>Top Level SOC Interconnectivity Verification Using Formal Techniques</b> .....	55
<i>Subir K. Roy</i>	
<b>On Automatic Test Block Generation for Peripheral Testing in SoCs via Dynamic FSMs Extraction</b> .....	63
<i>D. Ravotto, E. Sanchez, M. Schillaci, M. Sonza Reorda, G. Squillero</i>	
<b>Automotive Microcontroller End-of-Line Test via Software-Based Methodologies</b> .....	69
<i>W. Di Palma, D. Ravotto, E. Sanchez, M. Schillaci, M. Sonza Reorda, G. Squillero</i>	

## **FUNCTIONAL VALIDATION AND ATPG**

<b>Intel® First Ever Converged Core Functional Validation Experience: Methodologies, Challenges, Results and Learning</b> .....	75
<i>Tommy Bojan, Igor Frumkin, Robert Mauri</i>	
<b>Chico: An On-chip Hardware Checker for Pipeline Control Logic</b> .....	81
<i>Andrew DeOrio, Adam Bauserman, Valeria Bertacco</i>	
<b>A CLP-Based Functional ATPG for Extended FSMs</b> .....	88
<i>Franco Fummi, Cristina Marconcini, Graziano Pravadelli, Ian G. Harris</i>	

## **AMS VERIFICATION**

<b>Application of Automated Model Generation Techniques to Analog/Mixed-Signal Circuits</b> .....	96
<i>Scott Little, Alper Sen, Chris Myers</i>	

## **FUNCTIONAL MODELING AND TESTBENCHES**

<b>An ADL for Functional Specification of IA32</b> .....	103
<i>Wei Qin, Asa Ben-Tzur, Boris Gutkovich</i>	
<b>Automatic Testbench Generation for Rearchitected Designs</b> .....	112
<i>Mark Nodine</i>	

**Author Index**