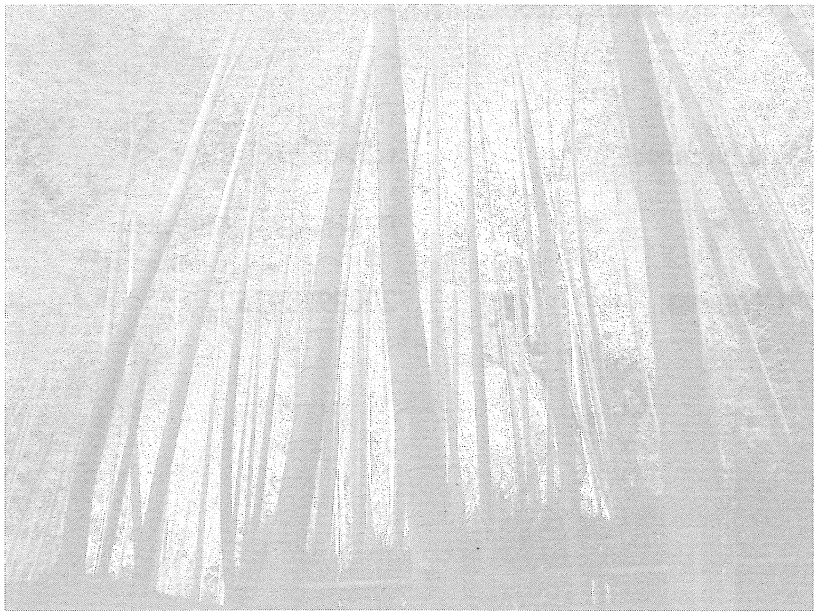
IEEE 9th VLSI Packaging Workshop in Japan

VPWJ2008

December 1st – 2nd, 2008
The Westin Miyako Kyoto, Kyoto, Japan



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Technical Program Schedule

Dec. 1st (Monday)

09:30 - 10:15 **Welcome and Invited Talk**

Chair: Michitaka Kimura, Renesas Technology Corp.

Opening Remarks
Michitaka Kimura, Renesas Technology Corp

01 **Invited Talk, 3D-SiP: the latest Miniaturization Technology ,**
Leonard W. Schaper, University of Arkansas

10:15 - 11:30 **Session 1: Advanced Packaging**

Co-Chairs: Michitaka Kimura & Len Schaper

07 **Stretchable electronic Systems for wearable and textile Applications,**
Thomas Löher, Rene Vieroth, Manuel Seckel, Andreas Ostmann*, and Herbert Reichl*,*
*Technische Universität Berlin, Fraunhofer-IZM**

11 **SLC-Based Optical Interconnect for Computing Systems,**
Shigeru Nakagawa, Yoichi Taira, Hidetoshi Numata, Kaoru Kobayashi, Kenji Terada* and Yutaka Tsukada*,*
*IBM Tokyo Research Laboratory, Kyocera SLC Technologies Corporation**

15 **Applied optimization of black oxide heat spreader for low-k flip chip packages,**
Chun-An Huang, Hui Ming Huang, Ho-Yi Tsai, Steve Chiu and C.M. Huang,
Siliconware Precision Industries

11:30-12:30 [Lunch]

12:30-14:35 **Session 2: Thermal Design**

Co-Chairs: Nobuo Kamehara & Rolf Aschenbrenner

21 **Accurate Junction Temperature prediction method for plastic LSI packages,**
Naoto Taoka, Atsushi Nakamura and Masao Urase,*
Renesas Technology Corp., Wave Technology Inc.*

25 **Solder Joint Lifetime Evaluation of WLP and Cause Investigation,**
Tomio Matsuzaki,
Casio Computer Co., Ltd

29 **A Study of material properties for Package Flatness in 3D Package,**
Yutaka Suzuki and Masazumi Amagai,
Texas Instruments Japan Limited Tsukuba Technology Center

33 **Enabling Dynamic Voltage & Frequency Scaling In Next-Generation Microprocessors: Thermal & Reliability Considerations,**
Sai Ankireddi and David Copeland,
Sun Microsystems

37 **Material property calculation of interposer card for modeling of Package-on-Package,**
Masanori Kuzuno, Hirokazu Noma and Toshihiko Nishio,*
*High Density Packaging Technology, Global Engineering Solutions AP Delivery, Global Engineering Solutions, * IBM Japan, Ltd.*

14:35-14:50 [Coffee Break]

14:50 - 16:30 **Session 3: Mechanical Design**

Co-Chairs: Takeshi Takamori and Tadaaki Mimura

43 **Numerical Analysis and Experimental Validation for the Prediction of Flip Chip Solder Joint Standoff Height in MEMS Microphone Application,**
Jeffery C. C. LO and S. W. Ricky Lee,
Electronic Packaging Laboratory Center for Advanced Microsystems Packaging Hong Kong University of Science and Technology

47 **WLCSP Parameter Study for Ball Reliability Analysis,**
Yuan Lin Tzeng, Eason Chen, Jeng Yuan Lai, Yu Po Wang and C.S. Hsiao,
Siliconware Precision Industries Co. Ltd.

51 **Prediction of Board Level Reliability of Drop Test for System-in-Package,**
Eiichi Yamada and Masazumi Amagai,
Texas Instruments Japan Limited Tsukuba Technology Center

55 **Board Level Reliability of Novel Fan-in Package on Package(PoP),**
Young-Lyong Kim, Cheul-Joong Youn, Jong-Ho Lee, Hyung-Kil Baek, Eun-Chul Ahn and Young-Hee Song,
Package Development Team, Memory Division, Samsung Electronics Co., Ltd.

16:30 - 18:35 **Session 4: Signal and Power Integrity**

Co-Chairs: Atsushi Nakamura and Toshio Sudo

63 **Enhanced Power Supply Structure with New Mesh Wiring and Electroless Plated Shunt Line and Assembly-Stress-Relaxation Structure,**
Taichi Nishio, Kazuhiro Ishikawa, Fumito Itoh, Yutaka Itoh, Chikako Karatani, Koji Koike, Yukitoshi Ota, Masao Takahashi and Hiroshige Hirano,
Panasonic Corporation.

67 **Development of Low Characteristic Impedance Transmission Line for Power Supply,**
Kaoru Hashimoto, Yutaka Akiyama, Toshiyuki Kawaguchi, Kazutoki Tahara*, and Kanji Otsuka,*
*Meisei University, Shin-Etsu Polymer Co., Ltd **

71 **Experimental Verification and Analysis for Noise Isolation of Analog and Digital Chip-Package-PCB Hierarchical Power Distribution Network,**
Hyunjeong Park, Jongjoo Shim, Yujeong Shim, Jeongsik Yoo and Joungho Kim,
School of Electrical Engineering & Computer Science, Division of Electrical Engineering, KAIST

75 **A Chip Stacking Technology Utilizing Transmission Line Coupling,**
Daisuke Iguchi, Yutaka Akiyama, Tsuneo Ito** and Kanji Otsuka*,*
Fuji Xerox Co., Ltd. Meisei University, Excel Service Co.***

79 **A Study on High-Speed Transmission Characteristics of Interconnections from PCB to Chip,**
Keitro Yamagishi, Takuma Ishibashi, Hideyuki Ohashi and Seiichi Saito,*
*Mitsubishi Electric Corp., Mitsubishi Electric Engineering Co.,Ltd.**

18:40 - 20:40 [Welcome Party]

Dec. 2nd (Tuesday)

09:00 - 10:40 **Session 5: Flip Chip and Interconnection**

Co-Chairs: Hirofumi Nakajima and Tomoshi Ohde

85 **Chip Package Interaction Analysis for Cu/Ultra Low-k Large Die Flip Chip Ball Grid Array,**
Chihiro J. Uchibori, Michael Lee, Xeufeng Zhang and Paul S. Ho*,*
*Fujitsu Laboratories of America, Inc., Microelectronics Research Center, University of Texas at Austin**

89 **The Chip-on-Board Bonding Using Non-Conductive Film and Metallic Bumps by the Surface Activated Bonding Method,**

Ying-Hui Wang and Tadatomo Suga,
School of Engineering, the University of Tokyo

93 **MPS-C2 and Post Encapsulation Grinding Technology for Ultra Fine Pitch and Thin Die Flip Chip Applications**
Yasumitsu Orii, Kazushige Toriyama, Yukifumi Oyama and Toshihiko Nishio,
Microlectronics Division, IBM Japan Ltd.

97 **New Developments in Flip Chip,**
E. Jan Vardaman,
TechSearch International, Inc.

10:40-10:55 [Coffee Break]

10:55 - 12:35 **Session 6: Advanced Material**

Co-Chairs: Kanji Otsuka and Rickey Lee

103 **Electrochemical Migration of Electronic Components at Sea Environments - Characterization and Solutions,**
Mohamed A. Hussain and Fuad M. Khoshnaw,*
*University of Sulaimani , Loughborough University**

107 **Unique High Reliability Urethane Resin for Car Electronic Module Packaging,**
Yoshimichi Takei, Kenji Ueda, Naokastu Hisanaga, Hatsuhiro Nakata, Kenji Ishii, Tomio Nagi, Atsush. Okuno,
Sanyu Rec Co.,

111 **Effect of Rare Earth Elements Doping on the Electrical Properties of (Ba,Sr)TiO_3 Thin Film Capacitors,**
Nobuo Kamehara, and Kazuaki Kurihara,*
*Fujitsu Quality Laboratory Ltd., Fujitsu Laboratories Ltd.**

115 **Highly reliable silicone TIM for CPU package - Silicone curable grease- ,**
Kei Miyoshi, Kunihiro Yamada and Kenichi Isobe,
Shin-Etsu Chemical Co., Ltd.

12:35-13:35 [Lunch]
13:35-14:05 [Award Ceremony]

14:05 - 15:45 **Session 7: Embedded Device and IPD**

Co-Chairs: Shigenori Aoki and Hiroshi Manita

121 **Comparative Stress Analysis of an Innovative Package with Embedded Die**

Substrate,
Albert Ou, Y.H. Wang, C.C. Fu, C.J. Hsu and C.L. Kao,
Advanced Semiconductor Engineering, Inc

125 **Si Interposers Integrated with $SrTiO_3$ Thin Film Decoupling Capacitors and Through-Si-Vias,**
Koichi Takemura, Akira Ohuchi and kinobu Shibuya,
Device Platforms Research Laboratories, NEC Corporation

129 **Reliability of Polyimide-based Thin and Flexible Capacitors with $SrTiO_3$,**
Yasuhiro Ishii, Toru Mori, Akinobu Shibuya and Koichi Takemura,
Device Platforms Research Laboratories, NEC Corporation

133 **Analysis of High Performance RF Integrated Passive Circuits Using the Glass Substrate ,**
Chen-Chao Wang, Hsueh-An Yang, Ying-Chieh Shyu, Meng-Hsun Li , Chi-Tsung Chiu , Sung-Mao Wu*, Chih-Wen Kuo** and Chih-Pin Hung,*
Electrical Laboratory, Corporation Design Division, Corporate R&D, Advanced Semiconductor Engineering Inc., Kaohsiung 811, Taiwan, Department of Electrical Engineering, National University of Kaohsiung, Taiwan, Department of Electrical Engineering, National Sun Yat-Sen University, Taiwan***

15:45-16:00 [Coffee Break]

16:00 - 17:15 **Session 8: 3-D Packaging**

Co-Chairs: Hiroshi Yamada and E. Jan Vardaman

139 **Room Temperature Wafer Bonding Using Surface Activated Bonding Method,**
Shingo Taniyama, Ying-Hui Wang, Masahisa Fujino and Tadatomo Suga,
School of Engineering, the University of Tokyo

143 **Integrated System Development for 3-D VLSI,**
Leonard Schaper, Yang Liu, Susan L. Burkett, Alphonse Kamto*, Gayathri Jampana**, Susan Jacob and Isibhakhomen Umolu Abhulimen*** ,*
University of Arkansas,Department of Electrical Engineering, University of Alabama, Brewer Science**, Intel Corp.****

147 **High Density Assembly Technology using Stacking Method,**
Takanori Maebashi, Natsuo Nakamura, Yutaka Sacho, Shigeto Nakayama, Eiri Hashimoto, Shinjiro Toyoda and Nobuaki Miyakawa,
Honda Research Institute

17:15 **Closing Remarks**