

2009 First International Conference on Advances in System Testing and Validation Lifecycle

(VALID 2009)

**Porto, Portugal
20-25 September 2009**



**IEEE Catalog Number: CFP0971H-PRT
ISBN: 978-1-4244-4862-3**

2009 First International Conference on Advances in System Testing and Validation Lifecycle

VALID 2009

Table of Contents

Preface

Organizing Committee

Reviewers

VALID 1: Testing Techniques and Mechanisms I

Reusing Component Test Cases for Integration Testing of Retarding Embedded System Components	1
<i>Abel Marrero Pérez and Stefan Kaiser</i>	
Fault Models for Neural Hardware	7
<i>Amit Prakash Singh, Pravin Chandra, and Chandra Sekhar Rai</i>	
A Web-Based Application to Verify Open Mobile Alliance Device Management Specifications	13
<i>Jose Felipe Mejia Bernal, Paolo Falcarin, and Maurizio Morisio</i>	
Towards Automated Test Practice Detection and Governance	19
<i>Roy Oberhauser</i>	

VALID 2: Testing Techniques and Mechanisms II & Work in Progress

SAT-Based On-Line Fault Isolation in Serial Systems	25
<i>Jinseong Jeon, Sangwon Kim, and Dongkeun Lee</i>	
Scenario-Based Test Case Generation Using Event-B Models	31
<i>Qaisar Ahmad Malik, Johan Lilius, and Linas Laibinis</i>	
An Open Real Time Test System Approach	38
<i>Nicolas Belanger, Nicolas Favarcq, and Yann Fusero</i>	

VALID 3: Robust Design Methodologies & Defects and Debugging

Is Depth of Inheritance Tree a Good Cost Prediction for Branch Coverage Testing?	42
<i>Muhammad Rabee Shaheen and Lydie du Bousquet</i>	
Improving TTCN-3 Test System Robustness Using Software Fault Tolerance	48
<i>Juho Perälä</i>	
Verification and Validation in the Recommended Practice for Integrated Software-Dependent Systems	57
<i>Thierry Coq</i>	
A High-Level Language and Compiler to Configure the Multi-core Debug Solution (MCDS)	62
<i>Jens Braunes and Rainer G. Spallek</i>	

VALID 4: Software Verification and Validation I

Security Inspection Scenarios – A Facet of Security	68
<i>Alexander Klaus and Frank Elberzhager</i>	
An Aspect-Oriented Approach for Assertion Verification	74
<i>Ulises Juarez-Martinez, Giner Alor-Hernández, Rubén Posada-Gómez, Joaquín Santos-Luna, Juan Miguel Gómez, and Alejandro Rodriguez Gonzalez</i>	
Integration Test Order Strategies to Consider Test Focus and Simulation Effort	80
<i>Lars Borner and Barbara Paech</i>	
Using the Testability Analysis Methodology for the Validation of AIRBUS Systems	86
<i>Fassely Doumbia, Odile Laurent, Chantal Robach, and Michel Delaunay</i>	

VALID 5: Software Verification and Validation II

Quality of Code Can Be Planned and Automatically Controlled	92
<i>Yegor Bugayenko</i>	
Stress Testing the Logical Decision Making Server of a Surveillance System	98
<i>Mikko Nieminen, Tomi Räty, and Jukka Palokangas</i>	
Automated Refactoring Suggestions Using the Results of Code Analysis Tools	104
<i>Steffen Herbold, Jens Grabowski, and Helmut Neukirchen</i>	
Time-Optimal Real-Time Test Case Generation Using Prioritized Time Petri Nets	110
<i>Noureddine Adjir, Pierre de Saqui-Sannes, and Mustapha Kamel Rahmouni</i>	

VALID 6: Software Verification and Validation III & Domain Oriented Testing

Validating the Behavioral Equivalence of TTCN-3 Test Cases	117
<i>Philip Makedonski, Jens Grabowski, and Helmut Neukirchen</i>	
Tracing Requirements in a Model-Based Testing Approach	123
<i>Fredrik Abbors, Dragoş Truşcan, and Johan Lilius</i>	
Model-Based Development and Testing of Process-Aware Information Systems	129
<i>Ronny S. Mans, Wil M.P. van der Aalst, Nick C. Russell, Piet J.M. Bakker, and Arnold J. Moleman</i>	
FPGA-Accelerated Baseband Design and Verification of Broadband MIMO Wireless Systems	135
<i>Amirhossein Alimohammad, Saeed Fouladi Fard, and Bruce F. Cockburn</i>	

VALID 7: Diagnosis & System and Feature Testing

A Low-Cost FPGA-Based Test and Diagnosis Architecture for SRAMs	141
<i>Stefano Di Carlo, Paolo Prinetto, Alberto Scionti, Joan Figueras, Salvador Manich, and Rosa Rodriguez-Montañés</i>	
Diagnosability of Input Output Symbolic Transition Systems	147
<i>Gauvain Bourgne, Philippe Dague, Farid Nouioua, and Nicolas Rapin</i>	
Using TMR Architectures for SoC Yield Improvement	155
<i>J. Vial, A. Virazel, A. Bosio, L. Dilillo, P. Girard, C. Landrault, and S. Pravossoudovitch</i>	
Problem Space and Special Characteristics of Security Testing in Live and Operational Environments of Large Systems Exemplified by a Nationwide IT Infrastructure	161
<i>Christian Schanes, Florian Fankhauser, Thomas Grechenig, Michael Schafferer, Kai Behning, and Dieter Hovemeyer</i>	

Author Index