

2010 IEEE International Conference on Computer Design (ICCD 2010)

**Amsterdam, Netherlands
3 – 6 October 2010**



**IEEE Catalog Number: CFP10ICD-PRT
ISBN: 978-1-4244-8936-7**

Table of Contents

Intro.

Welcome Message

Organizing Committee

Program Committee

External Reviewers

Keynote Presentations

Session 1.1. Architecture Innovation for High Performance

Session Chair. Jarmo Takala, Tampere Univ. of Technology

Out-of-Order Retirement of Instructions in Sequentially Consistent Multiprocessors 1
Rafael Ubal, Julio Sahuquillo, Salvador Petit, Pedro Lopez, David Kaeli

Efficient MIMD Architectures for High-Performance Ray Tracing 9
Daniel Kopta, Josef Spjut, Erik Brunvand, Al Davis

A Study on Performance Benefits of Core Morphing in an Asymmetric Multicore Processor 17
Anup Das, Rance Rodrigues, Israel Koren, Sandip Kundu

Session 1.2. Synchronous Circuits and Interfaces

Lowering the Latency of Interfaces for Rationally-Related Frequencies 23
Jean-Michel Chablotz, Ahmed Hemani

High Throughput, Low Set-up Time, Reconfigurable Linear Feedback Shift Registers..... 31
Rick Nas, Kees van Berkel

Robust and Energy-Efficient DSP Systems via Output Probability Processing 38
Rami Abdallah, Naresh Shanbhag

Session 1.3. Simulation, Optimization and Scheduling

Session Chair. Andy Pimentel, University of Amsterdam

Optimization of Back Pressure and Throughput for Latency Insensitive Systems	45
<i>Bin Xue, Sandeep Shukla</i>	
QoS Scheduling for NoCs: Strict Priority Queueing versus Weighted Round Robin	52
<i>Yue Qian, Zhonghai Lu, Qiang Dou</i>	
A Flexible Simulation Methodology and Tool for Nanoarray-based Architectures.....	60
<i>Stefano Frache, Mariagrazia Graziano, Maurizio Zamboni</i>	
Elaboration-time Synthesis of High-level Language Constructs in SystemC-based Microarchitectural Simulators	68
<i>Zhuo Ruan, Kurtis Cahill, David Penry</i>	
Session 2.1. High Performance Cache Architecture	
Session Chair. Mohamed Zahran, New York University	
Improving Cache Performance by Combining Cost-Sensitivity and Locality Principles in Cache Replacement Algorithms	76
<i>Rami Sheikh, Mazen Kharbutli</i>	
HELIA: Heterogeneous Interconnect for Low Resolution Cache Access in Snoop-based Chip Multiprocessors	84
<i>Amirali Baniasadi, Ali Shafiee, Narges Shahidi</i>	
A Tag-Based Cache Replacement	92
<i>Chuanjun Zhang, Bing Xue</i>	
A Voting-Based Working Set Assessment Scheme for Dynamic Cache Resizing Mechanisms	98
<i>Masayuki Sato, Ryusuke Egawa, Hiroyuki Takizawa, Hiroaki Kobayashi</i>	
Insertion Policy Selection Using Decision Tree Analysis	106
<i>Samira Khan, Daniel Jimenez</i>	
Session 2.2. Energy/Area efficient Circuit Design in Conventional and Emerging Technologies	
Minimizing Total Area of Low-Voltage SRAM Arrays through Joint Optimization of Cell Size, Redundancy, and ECC	112
<i>Nam Sung Kim, Shi-Ting Zhou, Sumeet Katariya, Hamid Ghasemi, Stark Draper</i>	
Thermal-Aware Scratchpad Memory Design and Allocation	118
<i>Morteza Damavandpeyma, Sander Stuijk, Twan Basten, Marc Geilen, Henk Corporaal</i>	

Spintronic Logic Gates for Spintronic Data Using Magnetic Tunnel Junctions	125
<i>Shruti Patil, Andrew Lyle, Jonathan Harms, David Lilja, Jian-Ping Wang</i>	

On Mismatch Number Distribution of Nanocrossbar Logic Mapping	132
<i>Yehua Su, Wenjing Rao</i>	

Sub-Threshold Charge Recovery Circuits	138
<i>Mehrdad Khatir, Hassan Ghasemzadeh Mohammadi, Alireza Ejlali</i>	

Data Rate Maximization by Adaptive Thresholding RF Power Management under Renewable Energy	145
<i>Weiguo Tang, Lei Wang</i>	

Practical Completion Detection for 2-of-N Delay-Insensitive Codes	151
<i>Marco Cannizzaro, Weiwei Jiang, Steven Nowick</i>	

Session 2.3. Real-Time and Embedded Systems

Rate-Monotonic Scheduling for Reducing System-Wide Energy Consumption for Hard Real-time Systems	159
<i>Linwei Niu</i>	

Design and Implementation of A Special Purpose Embedded System for Neural Machine Interface	166
<i>Xiaorong Zhang, He Huang, Qing Yang</i>	

A Control-Theoretic Energy Management for Fault-Tolerant Hard Real-Time Systems	173
<i>Ali Sharif-Ahmadian, Mahdieh Hosseingholi, Alireza Ejlali</i>	

RTOS-Aware Modeling of Embedded Hardware/Software Systems	179
<i>Matthias Mueller, Joachim Gerlach, Wolfgang Rosenstiel</i>	

Adaptive TDMA bus Allocation and Elastic Scheduling: a unified approach for enhancing robustness in multi-core RT systems	187
<i>Paolo Burgio, Martino Ruggiero, Francesco Esposito, Mauro Marinoni, Giorgio Buttazzo, Luca Benini</i>	

Session 3.1. Advances in Physical Design and Synthesis

Session Chair. Deming Chen, UIUC

The Fidelity Property of the Elmore Delay Model in Actual Comparison of Routing Algorithms	195
<i>Glauco Santos, Tiago Reimann, Ricardo Reis, Marcelo Johann</i>	

Routability-Driven Flip-Flop Merging Process for Clock Power Reduction .	203
<i>Zhi-Wei Chen, Jin-Tai Yan</i>	

Skew-Aware Capacitive Load Balancing for Low-Power Zero Clock Skew Rotary Oscillatory Array	209
<i>Vinayak Honkote, Baris Taskin</i>	
Incremental Gate Sizing for Late Process Changes	215
<i>John Lee, Puneet Gupta</i>	
Microarchitecture Aware Gate Sizing: A Framework for Circuit-Architecture Co-Optimization	222
<i>Sanghamitra Roy, Koushik Chakraborty</i>	
Boolean Factoring with Multi-Objective Goals	229
<i>Mayler Martins, Leomar Rosa Jr., Anders Rasmussen, Renato Ribas, Andre Inacio Reis</i>	
Session 3.2. Circuits for Arithmetic, Cryptography and Signal Processing	
A Simple Pipelined Logarithmic Multiplier	235
<i>Patricio Bulic, Zdenka Babic, Aleksej Avramovic</i>	
A Radix-10 Digit Recurrence Division Unit with a Constant Digit Selection Function	241
<i>Malte Baesler, Sven-Ole Voigt, Thomas Teufel</i>	
A Unified Addition Structure for Moduli Set $2n-1, 2n, 2n+1$ Based on a Novel RNS Representation	247
<i>Somayeh Timarchi, Mahmood Fazlali, Sorin Cotofana</i>	
Pulse Latch Based FSRs for Low-Overhead Hardware Implementation of Cryptographic Algorithms	253
<i>Shohreh Sharif Mansouri, Elena Dubrova</i>	
VEDA: Variation-aware Energy-efficient Discrete wavelet transform Archi- tecture	260
<i>Vaibhav Gupta, Georgios Karakostas, Debabrata Mohapatra, Kaushik Roy</i>	
Combined Optimal and Heuristic Approaches for Multiple Constant Mul- tiplication	266
<i>Jason Thong, Nicola Nicolici</i>	
Session 3.3. Multiprocessor Systems	
Threads vs. Caches: Modeling the Behavior of Parallel Workloads	274
<i>Zvika Guz, Oved Itzhak, Idit Keidar, Avinoam Kolodny, Avi Mendel- son, Uri C. Weiser</i>	

Predicting the Throughput of Multiprocessor Applications under Dynamic Workload	282
<i>Peter Poplavko, Marc Geilen, Twan Basten</i>	
M5 Based EDGE Architecture Modeling	289
<i>Pengfei Gou, Qingbo Li, Qi Zheng, Yinghan Jin, Bing Yang, Jinxiang Wang, Mingyan Yu</i>	
A Lightweight Run-time Scheduler for Multitasking Multicore Stream Applications	297
<i>Michael Baker, Karam S. Chatha</i>	
Scenario-Based Design Space Exploration of MPSoCs	305
<i>Peter van Stralen, Andy D. Pimentel</i>	

ICCD 2010 Best Papers Session.

Session Chairs. Sofiene Tahar (Concordia University), Lars Svensson (Chalmers University)

Toward Reliable SRAM-based Device Identification	313
<i>Joonsoo Kim, Joonsoo Lee, Jacob A. Abraham</i>	
DSS: Applying Asynchronous Techniques to Architectures Exploiting ILP at Compile Time	321
<i>Wei SHi, Zhiying Wang, Hongguang Ren, Ting Cao, Wei Chen, Bo Su, Hongyi Lu</i>	
Using Variable Clocking to Reduce Leakage in Synchronous Circuits	328
<i>Navid Toosizadeh, Safwat G. Zaky, Jianwen Zhu</i>	
Efficient Provably Good OPC Modeling and Its Applications to Interconnect Optimization	336
<i>Shih-Lun Huang, Chung-Wei Lin, Yao-Wen Chang</i>	
Lizard: Energy-efficient Hard Fault Detection, Diagnosis and Isolation in the ALU	342
<i>Seokin Hong, Soontae Kim</i>	

Session 5.1. Architecture Innovation for System Robustness and Performance

Session Chair. Sung Woo Chung, Korea University

Feasibility Study of Dynamic Trusted Platform Module	350
<i>Arun K. Kanuparthi, Mohamed Zahran, Ramesh Karri</i>	

Optimal Power/Performance Pipelining for Error Resilient Processors	356
<i>Nicolas Zea, John Sartori, Ben Ahrens, Rakesh Kumar</i>	

Implicit Hints: Embedding Hint Bits in Programs without ISA Changes . . .	364
<i>Hans Vandierendonck, Koen De Bosschere</i>	

Countering code injection attacks with TLB and I/O monitoring	370
<i>Dongkyun Ahn, Gyungho Lee</i>	

Session 5.2. Modeling and Optimization for Test Development

Session Chair. Klaus Schneider, University of Kaiserslautern

Energy-Optimal On-Line Self-Test of Microprocessors in WSN Nodes	376
<i>Andreas Merentitis, Antonis Paschalis, Dimitris Gizopoulos, Nektarios Kranitis</i>	

Temperature-to-Power Mapping	384
<i>Zhenyu Qi, Brett Meyer, Wei Huang, Robert Ribando, Kevin Skadron, Mircea Stan</i>	

Delay Test Quality Maximization through Process-aware Selection of Test Set Size	390
<i>Baris Arslan, Alex Orailoglu</i>	

Crosstalk Modeling to Predict Channel Delay in Network-on-Chips	396
<i>Ahmad Patooghy, Seyed Ghassem Miremdei, Mansour Shafaei</i>	

Generation of I/O Sequences for A High-level Design from Those in Post-Silicon for Efficient Post-Silicon Debugging	402
<i>Yeonbok Lee, Takeshi Matsumoto, Masahiro Fujita</i>	

Session 5.3. Energy and Performance Optimization

An Energy Model for Graphics Processing Units	409
<i>Jeff Pool, Anselmo Lastra, Montek Singh</i>	

LMS-based Low-Complexity Game Workload Prediction for DVFS	417
<i>Benedikt Dietrich, Swaroop Nunna, Dip Goswami, Samarjit Chakraborty, Matthias Gries</i>	

Exploiting SIMD Extensions for Linear Image Processing with OpenCL . .	425
<i>Samuel Antao, Leonel Sousa</i>	

A Co-Processor Approach for Accelerating Data-Structure Intensive Algorithms	431
<i>Jason Loew, Jesse Elwell, Dmitry Ponomarev, Patrick Madden</i>	

Session 6.1. Networks-on-Chip

Session Chair. Ben Juurlink, Technical Univ. of Berlin

SWIFT: A SWing-reduced Interconnect For a Token-based Network-on-Chip in 90nm CMOS 439
Tushar Krishna, Jacob Postman, Christopher Edmonds, Li-Shiuan Peh, Patrick Chiang

A Fine-Grained Link-Level Fault-Tolerant Mechanism for Networks-on-Chip 447
Arseniy Vitkovskiy, Vassos Soteriou, Chrysostomos Nicopoulos

Bandwidth Optimization in Asynchronous NoCs by Customizing Link Wire Length 455
Junbok You, Daniel Gebhardt, Kenneth Stevens

A High Performance Router With Dynamic Buffer Allocation For On-Chip Interconnect Networks 462
Qi Shubo, Zhang Minxuan, Li Jinwen, Zhao Tianlei, Zhang Chengyi, Li Shaoqing

Session 6.2. Verification and Design for Test with Reduced Overhead

Session Chair. Alex Orailoglu, UC San Diego

DDPSL: an Easy Way of Defining Properties 468
Luigi Di Guglielmo, Franco Fummi, Graziano Pravadelli, Nicola Orlando

DfT Optimization for Pre-Bond Testing of 3D-SICs containing TSVs 474
Jia Li, Dong Xiang

Efficient Test Response Compaction for Robust BIST using Parity Sequences 480
Thomas Indlekofer, Michael Schnittger, Sybille Hellebrand

EQUIPE: Parallel Equivalence Checking with GP-GPUs 486
Debapriya Chatterjee, Valeria Bertacco

Session 7.1. Energy Efficient Architecture

Session Chair. Andrei Terechko, Vector Fabrics

Identifying Optimal Generic Processors for Biomedical Implants 494
Christos Strydis, Dhara Dave

Exploiting Application-dependent Ambient Temperature for Accurate Architectural Simulation 502
Hyung Beom Jang, Jinhang Choi, Ikroh Yoon, Sung-Soo Lim, Seungwon Shin, Naehyuck Chang, Sung Woo Chung

Inter-socket Victim Cacheing for Platform Power Reduction	509
<i>Subhra Mazumdar, Dean Tullsen, Justin Song</i>	
Dynamic Register File Partitioning in Superscalar Microprocessors for En- ergy Efficiency	515
<i>Meltem Ozsoy, Yusuf Onur Kocerber, Mehmet Kayaalp, Oguz Ergin</i>	
Session 7.2. Power and Thermal Analysis and Optimization	
Session Chair. Baris Taskin, Drexel University	
Package-Aware Scheduling of Embedded Workloads for Temperature and Energy Management on Heterogeneous MPSoCs	521
<i>Sherwin Sharifi, Tajana Rosing</i>	
Towards cool and reliable digital systems: RT level CED techniques with runtime adaptability	528
<i>Yu Liu, Kaijie Wu</i>	
IP Characterization Methodology for Fast and Accurate Power Consump- tion Estimation at Transactional Level Model	534
<i>Michel Rogers-Vallee, Marc-Andre Cantin, Guy Bois, Laurent Moss</i>	
Enhancing Dual-Vt Design with Consideration of On-Chip Temperature Variation	542
<i>Junjun Gu, Lin Yuan, Gang Qu</i>	
BDD-Based Circuit Restructuring for Reducing Dynamic Power	548
<i>Quang Dinh, Deming Chen, Martin Wong</i>	
Author Index	555