

2010 IEEE International 3D Systems Integration Conference

(3DIC 2010)

Munich, Germany
16-18 November 2010



IEEE Catalog Number: CFP10DIC-PRT
ISBN: 978-1-4577-0526-7

TABLE OF CONTENTS

Cost Effectiveness of 3D Integration Options.....	1
<i>Dimitrios Velenis, Erik Jan Marinissen, Eric Beyne</i>	
Fine-Pitch Bump-less Cu-Cu Bonding for Wafer-on-Wafer Stacking and Its Quality Enhancement.....	7
<i>L. Peng, H. Y. Li, D. F. Lim, R. I. Made, G. Q. Lo, D. L. Kwong, C. S. Tan</i>	
3D Heterogeneous Integration for Novel Functionality.....	12
<i>Montserrat Fernández-Bolaños, Adrian M. Ionescu</i>	
3D Integration – A Server Perspective.....	31
<i>Jeff Burns</i>	
3D Integration Infrastructure & Market Status	51
<i>Christophe Zinck</i>	
3D R & D Technology for the Future Voyage in Japan.....	85
<i>Kenzo Inagaki</i>	
Thermal Isolation in 3D Chip Stacks using Vacuum Gaps and Capacitive or Inductive Communications	127
<i>Paul Franzon, John Wilson, Ming Li</i>	
Post-Bond Sub-500 nm Alignment in 300 mm Integrated Face-To-Face Wafer-To-Wafer Cu-Cu Thermocompression, Si-Si Fusion and Oxide-Oxide Fusion Bonding	131
<i>W. H. Teh, C. Deeb, J. Burggraf, D. Arazi, R. Young, C. Senowitz, A. Buxbaum</i>	
Design and Early Evaluation of a 3-D Die Stacked Chip Multi-Vector Processor	137
<i>Ryuusuke Egawa, Yusuke Funaya, Ryu-Ichi Nagaoka, Akihiro Musa, Hiroyuki Takizawa, Hiroaki Kobayashi</i>	
High Performance 3D Interconnects Based on Electrochemical Etch and Liquid Metal Fill	145
<i>Harry Hedler, Thomas Scheiter, Markus Schieber, Armin Klumpp, Peter Ramm</i>	
3D DfT Architecture for Pre-Bond and Post-Bond Testing	152
<i>Erik Jan Marinissen, Chun-Chuan Chi, Jouke Verbree, Mario Konijnenburg</i>	
Logic-on-Logic 3D Integration and Placement	160
<i>Thorlindur Thorolfsson, Guoqie Luo, Jason Cong, Paul D. Franzon</i>	
Impact of Microbump Induced Stress in Thinned 3D-LSIs after Wafer Bonding.....	164
<i>Mariappan Murugesan, Yuki Ohara, Jichael Bea, Kang-Wook Lee, Takafumi Fukushima, Tetsu Tanaka, Mitsumasa Koyanagi</i>	
Enabling Power Distribution Network Analysis Flows for 3D IEs.....	169
<i>Xiang Hu, Thomas Toms, Riko Radojcic, Matt Nowak, Nick Yu, Chung-Kuan Cheng</i>	
Reliability Testing of High Aspect Ratio Through Silicon Vias Fabricated with Atomic Layer Deposition Barrier, Seed Layer and Direct Plating and Material Properties Characterization of Electrografted Insulator, Barrier and Seed Layer for 3-D Integration	173
<i>Jason D. Reed, Scott Goodwin, Chris Gregory, Dorota Temple</i>	
Through Silicon Photonic Via (TSPV) with Si Core for Low Loss and High-Speed Data Transmission in Opto-Electronic 3-D LSI.....	181
<i>Akihiro Noriki, Kang-Wook Lee, Jichael Bea, Takafumi Fukushima, Tetsu Tanaka, Mitsumasa Koyanagi</i>	
Evaluation of Alignment Accuracy on Chip-to-Wafer Self-Assembly and Mechanism on the Direct Chip Bonding at Room Temperature.....	185
<i>T. Fukushima, E. Iwata, J. Bea, M. Murugesan, K.-W. Lee, T. Tanaka, M. Koyanagi</i>	
3D Stacked Buck Converter with 15µm Thick Spiral Inductor on Silicon Interposer for Fine-Grain Power-Supply Voltage Control in SiP's	190
<i>Koichi Ishida, Koichi Takemura, Kazuhiro Baba, Makoto Takamiya, Takayasu Sakurai</i>	
All-Wet Fabrication Technology for High Aspect Ratio TSV Using Electroless Barrier and Seed Layers	194
<i>Fumihiro Inoue, Takumi Yokoyama, Hiroshi Miyake, Shukichi Tanaka, Toshifumi Terui, Tomohiro Shimizu, Shoso Shingubara</i>	
Application of the SLID-ICV Interconnection Technology for the ATLAS Pixel Upgrade at SLHC	199
<i>L. Andricek, M. Beimforde, A. Klumpp, A. Macchiolo, K.-R. Merkel, H.-G. Moser, R. Nisius, R. H. Richter, J. Weber, P. Weigell, R. Wieland</i>	
Hierarchical 3D Interconnection Architecture with Tightly-Coupled Processor-Memory Integration.....	203
<i>Kiyoto Ito, Makoto Saen, Kenichi Osada, Tomoyuki Kodama, Hiroyuki Mizuno</i>	
Monolithic 3D Integration of SRAM and Image Sensor Using Two Layers of Single Grain Silicon.....	209
<i>Negin Golshani, Jaber Derakhshandeh, Ryoichi Ishihara, C. I. M Beenakker, Michael Robertson, Thomas Morrison</i>	

Developing Digital Test Sequences for Through-Silicon Vias within 3D Structures.....	213
<i>Matthias Gulbins, Fabian Hopsch, Peter Schneider, Bernd Straube, Wolfgang Vermeiren</i>	
Fabrication of TSV-Based Silicon Interposers	219
<i>D. Malta, E. Vick, S. Goodwin, C. Gregory, M. Lueck, A. Huffman, D. Temple</i>	
Timing Analysis and Optimization for 3D Stacked Multi-Core Microprocessors	225
<i>Young-Joon Lee, Sung Kyu Lim</i>	
A Successful Implementation of Dual Damascene Architecture to Copper TSV for 3D high Density Applications.....	232
<i>Rebha El Farhane, Myriam Assous, Patrick Leduc, Aurélie Thuaire, David Bouchu, Hélène Feldis, Nicolas Sillon</i>	
A 3D SoC Design for H.264 Application with On-Chip DRAM Stacking.....	236
<i>Tao Zhang, Kui Wang, Yi Feng, Yan Chen, Qun Li, Bing Shao, Jing Xie, Xiaodi Song, Lian Duan, Yuan Xie, Xu Cheng, Youn-Long Lin</i>	
Real-time Thermal Management of 3D Multi-core System with Fine-grained Cooling Control.....	242
<i>Hanhua Qian, Xiwei Huang, Hao Yu, Chip Hong Chang</i>	
CMIT- A Novel Cluster-based Topology for 3D Stacked Architectures.....	248
<i>Masoud Daneshtalab, Masoumeh Ebrahimi, Pasi Liljeberg, Juha Plosila, Hannu Tenhunen</i>	
Cache Partitioning Strategies for 3-D Stacked Vector Processors	253
<i>Yusuke Funaya, Ryusuke Egawa, Hiroyuki Takizawa, Hiroaki Kobayashi</i>	
Recent Developments of Cu-Cu Non-thermo Compression Bonding for Wafer-to-wafer 3D Stacking	259
<i>I. Radu, D. Landru, G. Gaudin, G. Riou, C. Tempesta, F. Letertre, L. Di Cioccio, P. Gueguen, T. Signamarcheix, C. Euvrard, J. Dechamp, L. Clavelier, M. Sadaka</i>	
Wireless Power Transfer Using Resonant Inductive Coupling for 3D Integrated ICs	265
<i>Sangwook Han, David D. Wentzloff</i>	
A High-Speed, Low-Power Capacitive-Coupling Transceiver for Wireless Wafer-Level Testing Systems	270
<i>Gil-Su Kim, Katsuyuki Ikeuchi, Mutsuo Daito, Makoto Takamiya, Takayasu Sakurai</i>	
TSV Development for Miniaturized MEMS Acceleration Switch.....	274
<i>Nicolas Lietaer, Anand Summanwar, Thor Bakke, Maaike Taklo, Per Dalsjø</i>	
Development of a CAD Tool for 3D-FPGAs.....	278
<i>Naoto Miyamoto, Yohei Matsumoto, Hanpei Koike, Tadayuki Matsumura, Kenichi Osada, Yaoko Nakagawa, Tadahiro Ohmi</i>	
3D System on Chip Memory Interface Based on Modeled Capacitive Coupling Interconnections	284
<i>M. Scandiuzzo, R. Cardu, S. Cani, S. Spolzino, L. Perugini, E. Franchi, R. Canegallo, R. Guerrieri</i>	
Wafer-Level Hybrid Bonding Technology with Copper/Polymer Co-planarization	288
<i>Mayu Aoki, Kazuyuki Hozawa, Kenichi Takeda</i>	
High Density 3D Integration by Pre-applied Inter Chip Fill	292
<i>Akihiro Horibe, Kuniaki Sueoka, Katsuyuki Sakuma, Sayuri Kohara, Keiji Matsumoto, Hidekazu Kikuchi, Yasumitsu Orii, Toshiro Mitsuhashi, Fumiaki Yamada</i>	
A Study of IR-drop Noise Issues in 3D ICs with Through-Silicon-Vias.....	297
<i>Moongon Jung, Sung Kyu Lim</i>	
Wafer-Level 3D Integration Using Hybrid Bonding.....	304
<i>Cheng-Ta Ko, Kuan-Neng Chen, Wei-Chung Lo, Chuan-An Cheng, Wen-Chun Huang, Zhi-Cheng Hsiao, Huan-Chun Fu, Yu-Hua Chen</i>	
In-Pixel ADC for a Vision Architecture on CMOS-3D Technology	308
<i>M. Suarez, V. M. Brea, Carlos Dominguez Matas, Ricardo Carmona, Gustavo Linan, Angel Rodriguez-Vazquez</i>	
Performance Analysis of 3-D Monolithic Integrated Circuits.....	315
<i>Shashikanth Bobba, Ashutosh Chakraborty, Olivier Thomas, Perrine Batude, Vasilis F. Pavlidis, Giovanni De Micheli</i>	
3D Memory Stacking for Fast Checkpointing/Restore Applications.....	319
<i>Jing Xie, Xiangyu Dong, Yuan Xie</i>	
Early Estimation of TSV Area for Power Delivery in 3-D Integrated Circuits.....	325
<i>Nauman H. Khan, Sherief Reda, Soha Hassoun</i>	
300mm Wafer Thinning and Backside Passivation Compatibility with Temporary Wafer Bonding for 3D Stacked IC Applications	331
<i>Anne Jourdain, Thibault Buisson, Alain Phommahaxay, Mark Privett, Dan Wallace, Sumanth Sood, Peter Bisson, Eric Beyne, Youssef Travaly, Bart Swinnen</i>	
Silicon-Interposer with High Density Cu-filled TSVs.....	335
<i>R. Wieland, K. Zoschke, N. Jürgensen, R. Merkel, L. Nebrich, J. Wolf</i>	
Development of High Accuracy Wafer Thinning and Pickup Technology for Thin Wafer	339
<i>Chuichi Miyazaki, Haruo Shimamoto, Toshihide Uematsu, Yoshiyuki Abe, Kosuke Kitaichi, Tadahiro Morifuji, Shoji Yasunaga</i>	

A Block-Parallel Signal Processing System for CMOS Image Sensor with Three-Dimensional Structure.....	343
<i>K. Kiyoyama, K-W Lee, T. Fukushima, H. Naganuma, H. Kobayashi, T. Tanaka, M. Koyanagi</i>	
Low Temperature Direct Wafer to Wafer Bonding for 3D Integration: Direct Bonding, Surface Preparation, Wafer-to-wafer Alignment	347
<i>Gweltaz Gaudin, Gregory Riou, Didier Landru, Catherine Tempesta, Ionut Radu, Mariam Sadaka, Kevin Winstel, Emily Kinser, Robert Hannon</i>	
Use of Optical Metrology for Wafer Level Packaging of CMOS Image Sensor.....	351
<i>D. Le Cunff, A. Pravdivtsev, K. Le Chao, S. Couvrat, C. Euvrard, E. Deloffre, A. Cailean</i>	
Integration of Multi Physics Modeling of 3D Stacks into Modern 3D Data Structures.....	357
<i>Peter Schneider, Andy Heinig, Robert Fischbach, Jens Lienig, Sven Reitz, Jörn Stolle, Andreas Wilde</i>	
Power Delivery Network Design and Optimization for 3D Stacked Die Designs	363
<i>Pratyush Singh, R. Sankar, Xiang Hu, Weize Xie, Aveek Sarkar, Toms Thomas</i>	
Solution Space Investigation and Comparison of Modern Data Structures for Heterogeneous 3D Designs.....	369
<i>Robert Fischbach, Jens Lienig, Matthias Thiele</i>	
Crosstalk Evaluation, Suppression and Modeling in 3D Through-Strata-Via (TSV) Network	377
<i>Zheng Xu, Adam Beece, Dingyou Zhang, Qianwen Chen, Kuan-Neng Chen, Kenneth Rose, Jian-Qiang Lu</i>	
Equipment Challenges and Solutions for Diverse Temporary Bonding and De-bonding Processes in 3D Integration.....	385
<i>Markus Gabriel, Thomas Knauer, Peter Bisson, Sumant Sood, Wilfried Bair, Jim Hermanowski</i>	
A Novel Concept for Ultra-Low Capacitance Via-Last TSV	390
<i>Y. Civale, M. Gonzalez, D. S. Tezcan, Y. Travaly, P. Soussan, E. Beyne</i>	
Additive Interconnect Fabrication by Picosecond Laser Induced Forward Transfer	394
<i>Gerrit Oosterhuis, Bert Huis In'T Veld, Gerald Ebberink, Daniël Arnaldo Del Cerro, Edwin Van Den Eijnden, Peter Chall, Ben Van Der Zon</i>	
Pixel Detectors in 3D Technologies for High Energy Physics	399
<i>G. Depuch, M. Demarteau, J. Hoff, R. Lipton, A. Shenai, R. Yarema, T. Zimmerman</i>	
Pre Bonding Metrology Solutions for 3D Integration.....	403
<i>Gregory Riou, Gweltaz Gaudin, Didier Landru, Catherine Tempesta, Ionut Radu, Emily Kinser, Robert Hannon, Mariam Sadaka, Boris V. Kamenev, Michael Darwin, Kevin Winstel, Robert Sachs</i>	
3DIC Multi-Project-Wafer Program: A Collaboration to Provide Fabrication Access.....	408
<i>Vance Tyree</i>	
Design Platform and Tools For 3D IC Integration	425
<i>Khaldoun Torki</i>	
The NCSU Tezzaron Design Kit.....	450
<i>Steve Lipa, Thor Thorolfsson, Paul Franzon</i>	
3DIC Multi-Project Fabrication Run being Organized by CMC/CMP/MOSIS and Tezzaron - Testimony: The First 3DIC Run Realized for the High Energy Physics Community.....	465
<i>G. Depuch</i>	
3D IEs and Pixel Sensors: The Italian VIPIX Project and the European AIDA WP3 Project	475
<i>Valerio Re</i>	
3D motivations for High Energy Physics and for Imaging Devices	481
<i>Jean Claude Clémens</i>	
High Sensitivity Fully Digital Photodetector	487
<i>Jean-François Pratte, Marc-André Tétrault, Réjean Fontaine</i>	

Author Index