

2011 IEEE Custom Integrated Circuits Conference

(CICC 2011)

**San Jose, California, USA
19 – 21 September 2011**



**IEEE Catalog Number: CFP11CIC-PRT
ISBN: 978-1-4577-0222-8**

TABLE OF CONTENTS

SESSION 2 -ENHANCED MODELING TECHNIQUES

Characterization and Analysis of Gate-All-Around Si Nanowire Transistors for Extreme Scaling.....	1
<i>Ru Huang, Runsheng Wang, Jing Zhuge, Changze Liu, Tao Yu, Liangliang Zhang, Xin Huang, Yujie Ai, Jinbin Zou, Yuchao Liu, Jiewen Fan, Huailin Liao, Yangyuan Wang</i>	
Broadband Compact Model for On-Chip mm-Wave Transformers and Baluns with Emphasis on Capacitive Coupling Effects.....	9
<i>Yang Tang, Zuochang Ye, Yan Wang</i>	
Bottom-up Digital System-level Reliability Modeling.....	13
<i>N. Ruiz Amador, V. Huard, E. Pion, F. Cacho, D. Croain, V. Robert, S. Engels, P. Flatresse, L. Anghel</i>	
Wafer-specific Centering of Compact Transistor Model Parameters for Advanced Technologies and Models.....	17
<i>B. De Vries, A. J. Scholten, P. F. E. Rommers, M. Stoutjesdijk, D. B. M. Klaassen</i>	

SESSION 3 - CLOCK SYNTHESIS AND CDRS

Area Efficient Phase Calibration of a 1.6 GHz Multiphase DLL	21
<i>Ankur Agrawal, Pavan Kumar Hanumolu, Gu-Yeon Wei</i>	
Digital Clock and Data Recovery Circuit Design: Challenges and Tradeoffs	25
<i>Mrunmay Talegaonkar, Rajesh Inti, Pavan Kumar Hanumolu</i>	
An All-Digital PLL Synthesized from a Digital Standard Cell Library in 65nm CMOS	33
<i>Youngmin Park, David D. Wentzloff</i>	
An Open-Loop 10GHz 8-Phase Clock Generator in 65nm CMOS.....	37
<i>Xiaochen Yang, Jin Liu</i>	

SESSION 4 - WIRELESS TRANSCEIVERS IN CMOS

SAW-less Software-Defined Radio Transceivers in 40nm CMOS.....	41
<i>Jan Craninckx, Jonathan Borremans, Mark Engels</i>	
A Dual-Channel GPS/Compass/Galileo/GLONASS Reconfigurable GNSS Receiver in 65nm CMOS.....	49
<i>Nan Qi, Yang Xu, Baoyong Chi, Yang Xu, Xiaobao Yu, Xing Zhang, Zhihua Wang</i>	
Complete SOC Transceiver in 0.18μm CMOS Using Q-enhanced Filtering, Sub-sampling and Injection Locking	53
<i>Ralph Mason, Justin Fortier, Chris Devries</i>	
A Wireless Sensor Node for Condition Monitoring Powered by a Vibration Energy Harvester	57
<i>Jae Hyuk Jang, David F. Berdy, Jangjoon Lee, Dimitrios Peroulis, Byunghoo Jung</i>	

SESSION 5 - TECHNOLOGY AND CIRCUIT DRIVERS FOR ULTRA-SCALE CMOS

Design and Technology Interaction Beyond 32nm.....	61
<i>Michael Clinton, Clive Bittlestone, G. Girishankar, Viet Le, Vinod Menezes</i>	
Statistical Advantages of Intrinsic Channel Fully Depleted SOI MOSFETs over Bulk MOSFETs	70
<i>Toshiro Hiramoto, Anil Kumar, Tomoko Mizutani, Jun Nishimura, Takuya Saraya</i>	
28nm Metal-gate High-K CMOS SoC Technology for High-Performance Mobile Applications	74
<i>S. H. Yang, J. Y. Sheu, M. K. Jeong, M. H. Chiang, T. Yamamoto, J. J. Liaw, S. S. Chang, Y. M. Lin, T. L. Hsu, J. R. Hwang, J. K. Ting, C. H. Wu, K. C. Ting, F. C. Yang, C. M. Liu, I. L. Wu, Y. M. Chen, S. J. Chent, K. S. Chen, J. Y. Cheng, M. H. Tsai, W. Chang, R. Chen, C. C. Chen, T. L. Lee, C. K. Lin, S. C. Yang, Y. M. Sheu, J. T. Tzeng, L. C. Lu, S. M. Jang, C. H. Diaz, Y. J. Mii</i>	

SESSION 6 - 3D AND PHOTONIC INTERCONNECT

Three Dimensional Integration - Considerations for Memory Applications	79
<i>S. S. Iyer, T. Kirihata, J. E. Barth</i>	

DRAM-on-logic Stack - Calibrated Thermal and Mechanical Models Integrated into PathFinding Flow	86
<i>Dragomir Mилоjevic, Herman Oprins, Julien Ryckaert, Paul Marchal, Geert Van Der Plas</i>	
Test Challenges for 3D Integration	90
<i>W. R. Bottoms</i>	
CDM-ESD Induced Damage in Components Using Stacked-Die Packaging	98
<i>Nicholas Olson, Nathan Jack, Vrashank Shukla, Elyse Rosenbaum</i>	
Silicon Photonics for On-Chip Interconnections	102
<i>Alan R. Mickelson</i>	

SESSION 7 - HIGH SPEED WIRELINE AND OPTICAL TRANSCEIVERS

A 19 mW/Lane SerDes Transceiver for SFI-5.1 Application	110
<i>Siavash Fallahi, Delong Cui, Deyi Pi, Rose Zhu, Greg Unruh, Marcel Lugthart, Afshin Momtaz</i>	
A Monolithic 3.125 Gbps Fiber Optic Receiver Front-end for POF Applications in 65 nm CMOS	114
<i>Yunzhi Dong, Ken Martin</i>	
Addressing Link-Level Design Tradeoffs for Integrated Photonic Interconnects	118
<i>Michael Georgas, Jonathan Leu, Benjamin Moss, Chen Sun, Vladimir Stojanovic</i>	
A 7.4 Gb/s Forwarded Clock Receiver Based on First-Harmonic Injection-Locked Oscillator Using AC Coupled Clock Multiplication Unit in 0.13µm CMOS	126
<i>Young-Ju Kim, Sang-Hye Chung, Lee-Sup Kim</i>	
Low-Power 8Gb/s Near-Threshold Serial Link Receivers Using Super-Harmonic Injection Locking in 65nm CMOS	130
<i>Kangmin Hu, Tao Jiang, Sam Palermo, Patrick Yin Chiang</i>	
A 16-Gb/s Backplane Transceiver with 12-Tap Current Integrating DFE and Dynamic Adaptation of Voltage Offset and Timing Drifts in 45-nm SOI CMOS Technology	134
<i>Gautam R. Gangasani, Chun-Ming Hsu, John F. Bulzacchelli, Sergey Rylov, Troy Beukema, David Freitas, William Kelly, Michael Shannon, Jieming Qi, Hui H. Xu, Joseph Natonio, Todd Rasmus, Jong-Ru Guo, Michael Wielgos, Jon Garlett, Michael A. Sorna, Mounir Meghelli</i>	
Power-Efficient I/O Design Considerations for High-Bandwidth Applications	138
<i>John C. Eble, Scott Best, Brian Leibowitz, Lei Luo, Robert Palmer, John Wilson, Jared Zerbe, Amir Amirkhany, Nhat Nguyen</i>	

SESSION 8 - SENSORS AND BIOSYSTEMS

Thermal Diffusivity Sensing: A New Temperature Sensing Paradigm	146
<i>C. P. L. Van Vroonhoven, K. A. A. Makinwa</i>	
A Self-Clocked ASIC Interface for MEMS Gyroscope with 1m°/s/√Hz Noise Floor	152
<i>A. Elsayed, A. Elshennawy, A. Elmallah, A. Shaban, B. George, M. Elmala, A. Ismail, A. Wassal, M. Sakr, A. Mokhtar, M. Hafez, A. Hamed, M. Saeed, M. Samir, M. Hammad, M. Elkhoully, A. Kamal, M. Rabieah, A. Elghufaili, S. Shaibani, I. Hakami, T. Alanazi</i>	
A 20 µW Contact Impedance Sensor for Wireless Body-Area-Network Transceiver	156
<i>Kiseok Song, Joonsung Bae, Long Yan, Hoi-Jun Yoo</i>	
256-site Active Neural Probe and 64-channel Responsive Cortical Stimulator	160
<i>R. Shulyzki, K. Abdelhalim, A. Bagheri, C. M. Florez, P. L. Carlen, R. Genov</i>	
Power Management Subsystem with Bi-directional DC to DC Converter for µ-Power Biomedical Applications	164
<i>Raymond E. Barnett, Ganesh K. Balachandran</i>	
A Capacitor-Based AC-DC Step-Up Converter for Biomedical Implants	168
<i>Edward K. F. Lee</i>	
Fully Integrated Power-Efficient AC-to-DC Converter Design in Inductively-Powered Biomedical Applications	172
<i>Hyung-Min Lee, Maysam Ghovanloo</i>	
Noise and Bandwidth Performance of Single-Molecule Biosensors	180
<i>J. Rosenstein, S. Sorgenfrei, K. L. Shepard</i>	

SESSION 9 (FORUM 1) – ENERGY MANAGEMENT: FROM DATACENTER TO HANDHELDS

Energy Efficient Computing In Large Scale Systems	187
<i>Tajana Rosing</i>	

Energy Efficient Designs with Wide Dynamic Range	188
<i>Vivek De</i>	
Advances and Challenges of Computing with FPGAs	189
<i>John Wawrzynek</i>	
High-Efficient Dc-Dc Converter Design	190
<i>Philip K T Mok</i>	

POSTER SESSION

A Discrete-Time Charge-Domain Filter with Bandwidth Calibration for LTE Application	191
<i>Ming-Feng Huang</i>	
A True Single SoC for UHF Mobile RFID Reader	195
<i>Jongmoon Kim, Seokoh Yun, Wonkab Oh, Minsu Kil, Sanghyun Cho</i>	
An 80% Peak Efficiency, 410mW, Single Supply Rail Powered Class-I Linear Audio Amplifier	199
<i>Zhenfei Peng, Shanshan Yang, Yong Feng, Zhiliang Hong, Bill Liu</i>	
Band-gap Circuit Design Challenges in High-performance 32-nm Technology	203
<i>J. F. Buller, J. Fletcher, S. Meyers, M. Robinson, F. Tamayo, A. Prakash, D. Cabler</i>	
Low Power and Error Resilient PN Code Acquisition Filter via Statistical Error Compensation	207
<i>Eric P. Kim, Daniel J. Baker, Sriram Narayanan, Douglas L. Jones, Naresh R. Shanbhag</i>	
0.4V SRAM with Bit Line Swing Suppression Charge Share Hierarchical Bit Line Scheme	211
<i>Shinichi Moriwaki, Atsushi Kawasumi, Toshikazu Suzuki, Takayasu Sakurai, Shinji Miyano</i>	
An Output Structure for a Bi-Modal 6.4-Gbps GDDR5 and 2.4-Gbps DDR3 Compatible Memory Interface	215
<i>Navin K. Mishra, Manish Jain, Phuong Le, Sanku Mukherjee, Arul Sendhil, Amir Amirkhany</i>	
A CMOS Image Sensor with on-chip Motion Detection and Object Localization	219
<i>Bo Zhao, Xiangyu Zhang, Shoushun Chen</i>	
Ultra Low-FOM High-Precision $\Delta\Sigma$ Modulators with Fully-Clocked SO and Zero Static Power Quantizers	223
<i>Jian Xu, Xiaobo Wu, Menglian Zhao, Rui Fan, Hanqing Wang, Xiaofen Ma, Bill Liu</i>	
A New CMOS Image Sensor Readout Structure for 3D Integrated Imagers	227
<i>Shang-Fu Yeh, Jin-Yi Lin, Chih-Cheng Hsieh, Ka-Yi Yeh, Chung-Chi Jim Li</i>	
All-Digital 3-50 GHz Ultra-Wideband Pulse Generator for Short-Range Wireless Interconnect in 40nm CMOS	231
<i>Changhui Hu, Patrick Y. Chiang</i>	
A 4GS/s, 8.45 ENOB and 5.7fJ/Conversion, Digital Assisted, Sampling System in 45nm CMOS SOI	235
<i>M. A. T Sanduleanu, S. Reynolds, J. O. Plouchart</i>	
Energy-Efficient Transceiver Circuits for Short-Range On-chip Interconnects	239
<i>Jacob Postman, Patrick Chiang</i>	
A Novel Audio Playback Chip Using Digitally Driven Speaker Architecture with 80%@-10dBFS Power Efficiency, 5.5W@3.3V Supply and 100dB SNR	243
<i>Michitaka Yoshino, Mitsuhiro Iwaide, Daigo Kuniyoshi, Hajime Ohtani, Akira Yasuda, Jun-Ichi Okamura</i>	
32-nm SOI Programmable, High-bandwidth 8.0-GHz Digital PLL	247
<i>Sanjeev K. Maheshwari, Emerson Fang, Sanjeev Aggarwal</i>	
A 38.6nV/Hz^{0.5} -59.6dB THD Dual-Band Micro- Electrode Array Signal Acquisition IC	251
<i>Jing Guo, Jiageng Huang, Jie Yuan, Jessica Ka-Yan Law, Chi-Kong Yeung, Mansun Chan</i>	
Analysis and Modeling of On-Chip Power Combiners and Their Losses in LINC Transmitters	255
<i>Adil Koukab, Omid Talebi Amiri</i>	
Programmable Phase/Frequency Generator for System Debug and Diagnosis Using The IEEE 1149.1 Test Bus	259
<i>Tsung-Yen Tsai, Gordon W. Roberts</i>	
Overlapped Inductors and Its Application on a Shared RF Front-end in a MultiStandard IC	263
<i>Lei Feng, Ram Sadhwani, Yaron Peperovits, Christopher Hull, Jonathan Jensen</i>	
A 1.0V 45nm Nonvolatile Magnetic Latch Design and Its Robustness Analysis	267
<i>Peiyuan Wang, Xiang Chen, Yiran Chen, Hai (Helen) Li, Seung Kang, Xiaochun Zhu, Wenqing Wu</i>	
A 1V 13mW Frequency-Translating $\Delta\Sigma$ ADC with 55dB SNDR for a 4MHz Band at 225MHz	271
<i>Philip M. Chopp, Anas A. Hamoui</i>	
CMOS Field-Modulated Color Sensor	275
<i>Derek Ho, Glenn Gulak, Roman Genov</i>	

SESSION 10 - RF BUILDING BLOCKS

A Fully Integrated Highly Linear Efficient Power Amplifier in 0.25μm BiCMOS Technology for Wireless Applications	279
<i>H. Hedayati, M. Mobarak, G. Varin, P. Meunier, P. Gamand, E. Sánchez-Sinencio, K. Entesari</i>	
A 1.9/2.4GHz Dual Band CMOS Power Amplifier with Integrated AM-PM Distortion Canceller.....	283
<i>K. Onizuka, H. Isihara, M. Hosoya, S. Saigusa, O. Watanabe, S. Otaka</i>	
Managing Linearity in Radio Front-Ends	287
<i>Ranjit Gharpurey</i>	
A Transformer-Based Broadband I/O Matching-Balun-T/R Switch Front-end Combo Scheme in Standard CMOS	295
<i>Yanjie Wang, Hua Wang, Chris Hull, Shmuel Ravid</i>	
A Low Conversion Loss Passive Frequency Doubler.....	299
<i>Muhammad Adnan, Ehsan Afshari</i>	

SESSION 11 - OVER-SAMPLING CONVERTERS

An 18μW 79dB-DR 20KHz-BW MASH $\Delta\Sigma$ Modulator Utilizing Self-Biased Amplifiers for Biomedical Applications.....	303
<i>Le Wang, Luke Theogarajan</i>	
A 75dB SNDR, 10MHz Conversion Bandwidth Stage- Shared 2-2 MASH $\Delta\Sigma$ Modulator Dissipating 9mW	307
<i>Ramin Zanbaghi, Saurabh Saxena, Gabor C. Temes, Terri S. Fiez</i>	
A 1-1-1-1 MASH Delta-Sigma Modulator Using Dynamic Comparator-Based OTAs	311
<i>Kentaro Yamamoto, Anthony Chan Carusone</i>	
A Double-Sampled Low-Distortion Cascade $\Delta\Sigma$ Modulator with an Adder/Integrator for WLAN Application	315
<i>S. Lee, J. Chae, M. Aniya, S. Takeuchi, K. Hamashita, P. K. Hanumolu, G. C. Temes</i>	
A 77dB SNDR, 4MHz MASH $\Delta\Sigma$ Modulator with a Second-Stage Multi-rate VCO-Based Quantizer	319
<i>Samira Zali Asl, Saurabh Saxena, Pavan Kumar Hanumolu, Kartikeya Mayaram, Terri S. Fiez</i>	
A 16MHz BW 75dB DR CT $\Delta\Sigma$ ADC Compensated for More Than One Cycle Excess Loop Delay	323
<i>Vikas Singh, Nagendra Krishnapura, Shanthi Pavan, Baradwaj Vignraham, Nimit Nigania, Debasish Behera</i>	
A 3.6GS/s, 15mW, 50dB SNDR, 28MHz Bandwidth RF $\Delta\Sigma$ ADC with a FoM of 1pJ/bit in 130nm CMOS	327
<i>Ahmed Ashry, Hassan Aboushady</i>	

SESSION 12 - SINGLE CHIP ARCHITECTURES FOR SENSING AND SIGNAL PROCESSING

A 45nm CMOS Neuromorphic Chip with a Scalable Architecture for Learning in Networks of Spiking Neurons.....	331
<i>Jae-Sun Seo, Bernard Brezzo, Yong Liu, Benjamin D. Parker, Steven K. Esser, Robert K. Montoye, Bipin Rajendran, José A. Tierno, Leland Chang, Dharmendra S. Modha, Daniel J. Friedman</i>	
A Digital Neurosynaptic Core Using Embedded Crossbar Memory with 45pJ per Spike in 45nm.....	335
<i>Paul Merolla, John Arthur, Filipp Akopyan, Nabil Imam, Rajit Manohar, Dharmendra S. Modha</i>	
Smart Integrated Temperature Sensor - Mixed-Signal Circuits and Systems in 32-nm and Beyond	339
<i>Y. William Li, Hasnain Lakdawala</i>	
ReSSP: A 5.877 TOPS/W Reconfigurable Smart-Camera Stream Processor	347
<i>Wei-Kai Chan, Yu-Hsiang Tseng, Pei-Kuei Tsung, Tzu-Der Chuang, Yi-Min Tsai, Wei-Yin Chen, Liang-Gee Chen, Shao-Yi Chien</i>	
3.6-GHz 0.2-mW/ch/GHz 65-nm Cross-Correlator for Synthetic Aperture Radiometry.....	351
<i>E. Ryman, A. Emrich, S. Andersson, J. Riesbeck, L. Svensson, P. Larsson-Edefors</i>	

SESSION 13 (FORUM 2) – EVOLUTION OF CLOCKS

Understanding the Antikythera Mechanism	355
<i>Tom Malzbender</i>	
Timing Inaccuracy of Clocks	356
<i>Ali Hajimiri</i>	

Frequency Reference Challenges - A Systemic View	357
<i>Harmeet Bhugra</i>	

SESSION 14 - VCOS, QUADRATURE VCOS, PLLS AND ALL DIGITAL PLLS

A Dither-less All Digital PLL for Cellular Transmitters	358
<i>L. Vercesi, L. Fanori, F. De Bernardinis, A. Liscidini, R. Castello</i>	
A 0.5-V, 440-μW Frequency Synthesizer for Implantable Medical Devices	366
<i>Wu-Hsin Chen, Wing-Fai Loke, Gabriel J. Thompson, Byunghoo Jung</i>	
A 4-GHz All Digital Fractional-N PLL with Low- Power TDC and Big Phase-Error Compensation	370
<i>Ja-Yol Lee, Mi-Jeong Park, Byonghoon Mhin, Seong-Do Kim, Moon-Yang Park, Hyunku Yu</i>	
A Quadrature LO Generator Using Bidirectionally-Coupled Oscillators for 60-GHz Applications.....	374
<i>Mohammad Hekmat, David K. Su, Bruce A. Wooley</i>	
A 0.6V Quadrature VCO With Optimized Capacitive Coupling for Phase Noise Reduction	378
<i>Feng Zhao, Fa Foster Dai</i>	
A Combined VCO and Divide-by-Two for Low-Voltage Low-Power 1.6 GHz Quadrature Signal Generation	382
<i>Shen Wang, Dong Sam Ha, Beomsup Kim, Vipul Chawla</i>	

SESSION 15 - PHASE-LOCKED LOOP AND ANALOG TECHNIQUES

A 2.2GHz PLL Using a Phase-Frequency Detector with an Auxiliary Sub-Sampling Phase Detector for In-Band Noise Suppression	386
<i>Chun-Wei Hsu, Karthik Tripurari, Shih-An Yu, Peter R. Kinget</i>	
A Fractional-N Frequency Synthesizer Using High-OSR Delta-Sigma Modulator and Nested-PLL.....	390
<i>Pyoungwon Park, Dongmin Park, Seonghwan Cho</i>	
A Sub-100μW 2GHz Differential Colpitts CMOS/FBAR VCO	394
<i>Jianlei Shi, Brian P. Otis</i>	
A 60mW 1.15mA/Channel Class-G Stereo Headphone Driver with 111dB DR and 120dB PSRR.....	398
<i>Sherif Galal, Hui Zheng, Khaled Abdelfattah, Vinay Chandrasekhar, Iuri Mehr, Alex Jianzhong Chen, John Platenak, Nir Matalon, Todd L. Brooks</i>	
A Multi-GHz Area-Efficient Comparator with Dynamic Offset Cancellation	402
<i>Lingkai Kong, Yue Lu, Elad Alon</i>	
Zero-Pole Modulation and Demodulation for Noise Reduction in Charge Amplifiers	406
<i>Nasrin Jaffari, Katelijn Vleugels, Bruce A. Wooley</i>	

SESSION 16 - EMBEDDED MEMORY TRENDS

Device-Conscious Circuit Designs for 0.5-V High- Speed Memory-Rich Nanoscale CMOS LSIs	410
<i>Akira Kotabe, Kiyoo Itoh, Riichiro Takemura, Ryuta Tsuchiya, Masashi Horiguchi</i>	
Dynamic Stability in Minimum Operating Voltage V_{min} for Single-port and Dual-port SRAMs.....	417
<i>Y. Tsukamoto, T. Kida, T. Yamaki, Y. Ishii, K. Nii, K. Tanaka, S. Tanaka, Y. Kihara</i>	
Characterization of SRAM Sense Amplifier Input Offset for Yield Prediction in 28nm CMOS.....	421
<i>Mohamed H. Abu-Rahma, Ying Chen, Wing Sy, Wee Ling Ong, Leon Yeow Ting, Sei Seung Yoon, Michael Han, Esin Terzioglu</i>	
Design Challenges for Prototypical and Emerging Memory Concepts Relying on Resistance Switching.....	425
<i>Ch. Muller, D. Deleruyelle, O. Ginez, J-M. Portal, M. Bocquet</i>	
A 28 nm 50% Power Reduced 2T Mask ROM with 0.72 ns Read Access Time Using Column Source Bias.....	432
<i>Y. Umemoto, K. Nii, J. Ishikawa, K. Okamoto, K. Mori, K. Yanagisawa</i>	
Improved Circuits for Microchip Identification Using SRAM Mismatch	436
<i>Srivatsan Chellappa, Aritra Dey, Lawrence T. Clark</i>	

POSTER SESSION

A Low-Power and Low-Noise 21~29 GHz Ultra-Wideband Receiver Front-End in 0.18 μm CMOS Technology	440
<i>Sheng-Li Huang, Yo-Sheng Lin, Jen-How Lee</i>	

A 2GHz Digital PLL, with Temperature Lock Range of -40°C to 125°C, in 45nm CMOS	444
<i>Biman Chattopadhyay, Anant S Kamath, Satyasai Evani, Karthik Subburaj</i>	
Indirect Phase Noise Sensing for Self-Healing Voltage Controlled Oscillators	448
<i>S. Yaldiz, V. Calayir, X. Li, L. Pileggi, A. S. Natarajan, M. A. Ferriss, J. Tierno</i>	
An At-speed Self-testable Technique for the High Speed Domino Adder	452
<i>Yu-Shun Wang, Min-Han Hsieh, Chia-Ming Liu, Chi-Wei Liu, James C.-M. Li, Charlie Chung-Ping Chen</i>	
A 95dB SNDR Audio $\Delta\Sigma$ Modulator in 65nm CMOS	456
<i>L. Liu, D. Li, Y. Ye, L. Chen, Z. Wang</i>	
A Fully Integrated CMOS Nanoscale Biosensor Microarray	460
<i>Lei Zhang, Xiangqing He, Yan Wang, Zhiping Yu</i>	
A Passive UHF Tag for RFID-based Train Axle Temperature Measurement System	464
<i>Jianqin Qian, Chun Zhang, Liji Wu, Xijin Zhao, Dingguo Wei, Zhihao Jiang, Yuhui He</i>	
A 48-mW, 12-bit, 150-MS/s Pipelined ADC with Digital Calibration in 65nm CMOS	468
<i>Bei Peng, Guanzhong Huang, Hao Li, Peiyuan Wan, Pingfen Lin</i>	
Statistical V_{TH} Shift Variation Self-Convergence Scheme Using Near Threshold V_{WL} Injection for Local Electron Injected Asymmetric Pass Gate Transistor SRAM	472
<i>Kousuke Miyaji, Yasuhiro Shinozuka, Shinji Miyano, Ken Takeuchi</i>	
A Fully-integrated Optical Duobinary Transceiver in a 130nm SOI CMOS Technology	476
<i>James F. Buckwalter, Joohwa Kim, Xuezhe Zheng, Guoliang Li, Kannan Raj, Ashok Krishnamoorthy</i>	
Electrically-Driven Retargeting for Nanoscale Layouts	480
<i>Shayak Banerjee, Kanak B. Agarwal, Sani R. Nassif</i>	
A Partial Tree Vector Quantizer Dynamic Element Matching Technique for Audio $\Delta-\Sigma$ Converters	484
<i>Emmanuel Hardy, Hassan Ihs, Christian Dufaza, Stéphane Meillère, Rachid Bouchakour</i>	
5 Gbps BPSK CMOS Transmitter with On-Chip Antenna Using Gaussian Monocycle Pulses	488
<i>S. Kubota, N. Sasaki, M. Hafiz, A. Toya, T. Kikkawa</i>	
Amorphous Silicon Current Steering Digital to Analog Converter	492
<i>Aritra Dey, David R. Allee</i>	
A 65nm CMOS Self-Terminated Open-Drain IDAC Line Driver Suitable for Fast Ethernet Applications	496
<i>Joseph Aziz, Ark-Chew Wong, Andrew Chen, Derek Tam</i>	
A High-PSR LDO Using a Feedforward Supply-Noise Cancellation Technique	500
<i>Bangda Yang, Brian Drost, Sachin Rao, Pavan Kumar Hanumolu</i>	
A Time-domain Latch Interpolation Technique for Low Power Flash ADCs	504
<i>Jong-In Kim, Wan Kim, Barosaïm Sung, Seung-Tak Ryu</i>	
Low-Power Block-Level Instantaneous Comparison 7T SRAM for Dual Modular Redundancy	508
<i>Shunsuke Okumura, Yohei Nakata, Koji Yanagida, Yuki Kagiya, Shusuke Yoshimoto, Hiroshi Kawaguchi, Masahiko Yoshimoto</i>	
A 40 nm 144 mW VLSI Processor for Realtime 60 kWord Continuous Speech Recognition	512
<i>Guangji He, Takanobu Sugahara, Tsuyoshi Fujinaga, Yuki Miyamoto, Hiroki Noguchi, Shintaro Izumi, Hiroshi Kawaguchi, Masahiko Yoshimoto</i>	
A Non-Coherent Versatile DPSK Receiver for High Channel-Density Neural Prosthesis	516
<i>Le Zheng, Kuanfu Chen, Wentai Liu</i>	
Performance, Metastability and Soft-Error Robustness Tradeoffs for Flip-Flops in 40nm CMOS	520
<i>David Rennie, David Li, Manoj Sachdev, Bharat Bhuvra, Srikanth Jagannathan, Shijie Wen, Rick Wong</i>	

SESSION 18 - MM WAVE CIRCUITS AND SYSTEMS

Circuit Technologies for mm-Wave Wireless Systems on Silicon	524
<i>John R. Long, Y. Zhao, Y. Jin, W. Wu, M. Spirito</i>	
A 76-81GHZ Transmitter with 10dBm Output Power at 125°C for Automotive Radar in 65nm Bulk CMOS	532
<i>Kun-Hin To, Vishal P. Trivedi</i>	
A 2.9-dB Noise Figure, Q-Band Millimeter-Wave CMOS SOI LNA	536
<i>Mehmet Parlak, James F. Buckwalter</i>	
A High Gain 107 GHz Amplifier in 130 nm CMOS	540
<i>Omeed Momeni, Ehsan Afshari</i>	
Double-Balanced 130-180 GHz Passive and Balanced 145-165 GHz Active Mixers in 45 nm CMOS	544
<i>Ozgur Inac, Andy Fung, Gabriel M. Rebeiz</i>	
60GHz Low-Loss Compact Phase Shifters Using A Transformer-Based Hybrid in 65nm CMOS	548
<i>Maryam Tabesh, Amin Arbabian, Ali Niknejad</i>	

SESSION 19 - NYQUIST A/D

A 0.5V 1KS/s 2.5nW 8.52-ENOB 6.8fJ/Conversion- Step SAR ADC for Biomedical Applications	552
<i>Tsung-Che Lu, Lan-Da Van, Chi-Sheng Lin, Chun-Ming Huang</i>	
A 0.7V 810μW 10b 30MS/s Comparator-Based Two-Step Pipelined ADC.....	556
<i>Ho-Young Lee, David Gubbins, Bumha Lee, Un-Ku Moon</i>	
A 450 MS/s 10-bit Time-Interleaved Zero-Crossing Based ADC	560
<i>J. Chu, H.-S. Lee</i>	
A 40-mW 7-bit 2.2-GS/s Time-Interleaved Subranging ADC for Low-Power Gigabit Wireless Communications in 65-nm CMOS	564
<i>I-Ning Ku, Zhiwei Xu, Yen-Cheng Kuan, Yen-Hsiang Wang, Mau-Chung Frank Chang</i>	

SESSION 20 - ENHANCED SIMULATION TECHNIQUES

High-Dimensional Statistical Modeling and Analysis of Custom Integrated Circuits	568
<i>Trent McConaghy</i>	
Fast and Accurate Event-Driven Simulation of Mixed-Signal Systems with Data Supplementation	576
<i>Myeong-Jae Park, Hanseok Kim, Minbok Lee, Jaeha Kim</i>	
Enhanced Sensitivity Computation for BEM Based Capacitance Extraction Using the Schur Complement Technique	580
<i>Yu Bi, Simon De Graaf, Nick Van Der Meijs</i>	
Power Gating Implementation for Noise Mitigation with Body-Tied Triple-Well Structure	584
<i>Yasumichi Takai, Masanori Hashimoto, Takao Onoye</i>	
Exploration of On-Chip Switched-Capacitor DC-DC Converter for Multicore Processors Using a Distributed Power Delivery Network.....	588
<i>Pingqiang Zhou, Dong Jiao, Chris H. Kim, Sachin S. Sapatnekar</i>	

SESSION 21 - POWER MANAGEMENT

A 90nm Data Flow Processor Demonstrating Fine Grained DVS for Energy Efficient Operation from 0.25V to 1.2V	592
<i>Y. Shakhsheer, S. Khanna, K. Craig, S. Arrabi, J. Lach, B. H. Calhoun</i>	
An Integrated Four-Phase Buck Converter Delivering 1A/mm² with 700ps Controller Delay and Network-on-Chip Load in 45-nm SOI	596
<i>N. Sturcken, M. Petracca, S. Warren, L. P. Carloni, A. V. Peterchev, K. L. Shepard</i>	
A Wide-Range DC/DC Converter with 2nd Order Digital Compensation and Direct Battery Connection in 40nm CMOS	600
<i>Justin Shi, Ying-Chih Hsu, Eric Soenen, Alan Roth, Justin Gaither</i>	
An 80% Peak Efficiency, 0.84mW Sleep Power Consumption, Fully-Integrated DC-DC Converter with Buck/LDO Mode Control	604
<i>Xiaohan Gong, Jinhua Ni, Zhiliang Hong, Bill Liu</i>	
Perturbation On-time (POT) Control and Inhibit Time Control (ITC) in Suppression of THD of Power Factor Correction (PFC) Design.....	608
<i>Jen-Chieh Tsai, Chi-Lin Chen, Yi-Ting Chen, Chia-Lung Ni, Chun-Yen Chen, Ke-Horng Chen, Chih-Jen Chen, Heng-Lin Pan</i>	
A Reconfigurable 2x / 2.5x / 3x / 4x SC DC-DC Regulator for Enhancing Area and Power Efficiencies in Transcutaneous Power Transmission	612
<i>Xiwen Zhang, Hoi Lee</i>	
A Near-Zero Cross-Regulation Single-Inductor Bipolar-Output (SIBO) Converter with an Active-Energy-Correlation Control for Driving Cholesteric-LCD.....	616
<i>Yu-Huei Lee, Ming-Yan Fan, Wei-Chung Chen, Ke-Horng Chen, Sheng-Fa Liu, Pao-Hsien Chiu, Sandy Chen, Chun-Yu Shen, Ming-Ta Hsieh, Huai-An Li</i>	
Author Index	