

8th Annual International Wafer-Level Packaging Conference & Tabletop Exhibition 2011

(IWLPC 2011)

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IWLPC 2011 CONFERENCE PROGRAM

Wednesday, October 5, 2011

OPENING COMMENTS

Andy Strandjord, *Pac Tech USA*, Conference General Chair

Morning Plenary

High Density TSV Chip Stacking: Fabless Infrastructure Status

Matt Nowak, *Qualcomm*

WLP TRACK

Session 1 - Advanced Wafer Level Packaging Technologies

Chair: Beth Keser, Ph.D., *Qualcomm*

Board Level Reliability of Wafer Level CSP's for Telecommunication System Applications

Weifeng Liu, Ph.D., *Huawei Technologies*, Presented by Anwar Mohammed, *Huawei Technologies*

Disruptive Wafer-Level Package-on-Package Technology

Andrew Holland, *RF Module and Optical Design Limited (RFMOD)*, Presenting on his behalf is Terence Q. Collier, *CV Inc*

Wafer Backside Coating (WBC): Low Cost & Flexible Die-Attach Technology for Reliable Thin Die Stack Assembly

Gyan Dutt, *Henkel Electronic Materials LLC*

3D TRACK

Session 2 - 3D Process Advancements Part I

Chair: Francoise von Trapp, *3D InCites*

Lithography Challenges for Leading Edge 3D Packaging Applications

Manish Ranjan, *Ultratech, Inc.*

Resist Removal Technology for Next Generation 3D Packaging Solutions

Kimberly Pollard, Ph.D., *Dynaloy, LLC*

Process and Equipment Enhancements for C2W Bonding in a 3D Integration Scheme

Keith Cooper, *SET North America*

MEMS TRACK

Session 3 - MEMS Packaging Simulation and Wafer Level Technologies

Chair: Russ Shumway, *Amkor Technology*

Wafer Level Vacuum Encapsulation for an Uncooled Microbolometer Array

Martin Bring, Ph.D., *Sensor Technologies AS*

Packaging Nanoporous Energetic Silicon for On-Chip MEMS Applications

Wayne Churaman, *U.S. Army Research Laboratory*

Design Considerations and Computer Aided Design (CAD) Solutions for Packaging MEMS

Mary Ann Maher, *SoftMEMS LLC*

WLP TRACK

Session 4 - Fan-Out Wafer Level Packaging Technologies

Chair: Ravi Chilukuri, *Amkor Technology*

Potential of Large Area Mold Embedded Packages with PCB Based Redistribution

Tanja Braun, *Fraunhofer IZM*

New Applications for Fan-Out Wafer Level Packaging Technology

José Campos, *NANIUM, S.A.*

Design for Board Level Reliability Improvement in eWLB (Embedded Wafer Level BGA) Packages

Won Kyoung Choi, *STATS ChipPAC*, Presented by Yeong Lee, Ph.D., *STATS ChipPAC*

3D TRACK

Session 5 - 3D Inspection, Measurement & Reliability

Chair: Russell Stapleton, Ph.D., *LORD Corporation*

Laser Triangulation Provides Essential Metrology and Defect Inspection for Microbumps in 3DIC Manufacturing

Reza Asgari, *Rudolph Technologies, Inc.*

Processing and Reliability Assessment of Silicon Based, Integrated Ultra High Density Substrates

Daniel Baldwin, Ph.D., *Engent, Inc.*

Identify the Mechanism of Stress-Assisted Void Growth in Through Silicon Via (TSV) by X-ray Microscopy and Finite Element Modeling

LayWai Kong, *College of Nano Scale Science & Engineering at SUNY Albany*

MEMS TRACK

Session 6 - MEMS 3D and Wafer Bonding Technologies

Chair: Peter Ramm, Ph.D., *Fraunhofer EMFT*

Wafer-Level Packaged MEMS Switch With TSV

Nicolas Lietaer, *SINTEF*

3D Interconnect Integration Success and Challenges

Jeff Visser, *SVTC Technologies*

Intermetallic SLID Bonding (Cu-Sn and Au-Sn) for Wafer Level Encapsulation

Kaiying Wang, *Vestfold University College*

IWLPC 2011 CONFERENCE PROGRAM

Thursday, October 6, 2011

Morning Plenary

Evolution, Challenge, and Outlook of 3D Si/IC Integrations

John Lau, Ph.D., *Industrial Technology Research Institute* *****\$- -

WLP TRACK

Session 7 - Embedded Chip Packaging Technologies

Co-Chair: Yeong Lee, Ph.D., *STATS ChipPAC*

Co-Chair: Vern Solberg, *Solberg Technical Consulting*

Development of Next Generation eWLB (Embedded Wafer Level BGA) Technology

Yong Gang Jin, *ST Mircoelectronics*, Presented by Yeong Lee, Ph.D., *STATS ChipPAC* *****%&

Laminate Based Fan-Out Embedded Die Packaging Using Polyimide Multilayer Wiring Boards

Kazuhisa Itoi, *Fujikura Ltd.* *****%&'

System-In-Package Solutions with IMBR® Substrates

Tuomas Waris, *Imbera Electronics* *****% \$

3D TRACK

Session 8 - 3D Process Advancements Part II

Chair: George Li, Ph.D., Intel ATTD

Wafer Backside Processes in TSV Technology

Niranjan Kumar, *Applied Materials, Inc.* *****% +

Feasibility of Double-sided Electroplating for Advanced Packaging Applications

Richard Hollman, Ph.D., *NEXX Systems, Inc.* *****% ,

Near Term Solutions for 3D Packing of High Performance DRAM

Vern Solberg, *Invensas*, Presented by Simon McElrea, *Invensas* *****% \$

WLP TRACK

Session 9 - Wafer Level Packaging: Probe, Cost, and Reliability

Chair: Ted Tessier, *Flip Chip International*

Cost Comparison of Fine Pitch Chip Scale Packaging Technologies

Alan Palesko, *SavanSys Solutions LLC* *****% +

Effects of Current Density and Pulse Frequency on Electroplated Copper Solder Joint Reliability

Darren Moore, *Fairchild Semiconductor* *****% €

3D TRACK

Session 10 - Next Generation 3D Fan-Out WLP

Chair: Luu Nguyen, Ph.D., *National Semiconductor*

System-In-Package Opportunities with the Redistributed Chip Package (RCP)

Scott Hayes, *Freescale Semiconductor* *****% *

eWLB (Embedded Wafer Level BGA) Technology: Dawn of a New Age of Thin and 3D Package Technology

Seung Wook Yoon, *STATS ChipPAC*, Presented by Yeong Lee, Ph.D., *STATS ChipPAC* *****%*'

Design Concept and Processing Solution for Molded Via BGA

Paul Lin, *Via Pak LLC* *****%*,