

**Stress Management for 3D
ICs Using Through Silicon Vias:
Product-Level Reliability
Workshop 2011**

**San Francisco, California, USA
14 July 2011**

ISBN: 978-1-61839-390-6

Printed from e-media with permission by:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571



Some format issues inherent in the e-media version may also appear in this print version.

Copyright© (2011) by SEMATECH
All rights reserved.

Printed by Curran Associates, Inc. (2012)

For permission requests, please contact SEMATECH
at the address below.

SEMATECH
2706 Montopolis Drive
Austin, Texas 78741

Phone: (512) 356-3500
Fax: (512) 356-7848

www.sematech.org

Additional copies of this publication are available from:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: 845-758-0400
Fax: 845-758-2634
Email: curran@proceedings.com
Web: www.proceedings.com

Stress Management for 3D ICs Using Through Silicon Vias: Product-Level Reliability Workshop

July 14, 2011
San Francisco, CA

Product-Level Reliability Workshop – Stress Management for 3D ICs Using Through Silicon Vias	Larry Smith, SEMATECH	1
3D TSV Product Qualification Challenges Product Level Reliability	Mark Nakamoto, Qualcomm	5
Failure Analysis for 3D TSV Systems	Eric Beyne, Imec	16
TSV: Current Product Reliability – ‘What’s Missing?’	R. Huemoeller, Amkor Technology	32
3D TSV Reliability Challenges and Qualification Considerations	You-wen Yau, Qualcomm CDMA Technologies	45
Stacked Silicon Interconnect Technology (SSIT) Qualification –Requirements and Tools	Suresh Ramalingam, Xilinx Inc.	53
Implications of mechanical stress in 3D technologies on reliability	Valeriy Sukharev, Mentor Graphics	64
Discussion Summary Session		69
Speaker Bios		72