9th Annual International Wafer-Level Packaging Conference 2012

(IWLPC 2012)

San Jose, California, USA
5-8 November 2012

ISBN: 978-1-62276-897-4

Printed from e-media with permission by:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571

Some format issues inherent in the e-media version may also appear in this print version.

Copyright© (2012) by Surface Mount Technology Association (SMTA)
All rights reserved.

Printed by Curran Associates, Inc. (2013)

For permission requests, please contact Surface Mount Technology Association (SMTA)
at the address below.

Surface Mount Technology Association (SMTA)
5200 Wilson Road
Suite 215
Edina, MN 55424

Phone: (952) 920-4682
Fax: (952) 926-1819

www.smta.org

Additional copies of this publication are available from:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: 845-758-0400
Fax: 845-758-2634
Email: curran@proceedings.com
Web: www.proceedings.com

IWLPC 2012 CONFERENCE PROGRAM

Tutorials

Monday, November 5th

T1: TSV and Other Key Enabling Technologies for 3D IC/Si Integration
John H. Lau, Ph.D., Industrial Technology Research Institute (ITRI)
8:30am-12:00pm
Monterey

T2: IC Package Cost Reduction Using Supply Chain Modeling
Chet Palesko, SavanSys Solutions LLC and Jan Vardamann, TechSearch International, Inc.
8:30am-12:00pm
Carmel

T3: Embedded Components Design and Process Implementation
Vern Solberg, Invensas Corporation
1:30pm-5:00pm
Monterey

T4: Failure Analysis Techniques for a 3D World
Chris Henderson, Semitracks, Inc.
1:30pm-5:00pm
Carmel

Tuesday, November 6th

T5: Wafer-Level Packaging
Luu Nguyen, Ph.D., Texas Instruments, Inc.
8:30am-12:00pm
Monterey

T6: PiezoMEMS from Design to Packaging
Dag Wang, Ph.D., SINTEF ICT
8:30am-12:00pm
Carmel

T7: Packaging for MEMS
Andy Oliver, Ph.D., Wireless Integrated MicroSensing and Systems Research Center (WIMS2)
University of Michigan
1:30pm-5:00pm
Monterey

T8: Failure Mode Analysis of Flip Chip and Advanced Package and Board Assemblies
Brian Lewis, Engent, Inc.
1:30pm-5:00pm
Carmel

IWLPC 2012 CONFERENCE PROGRAM

Wednesday, November 7th

Opening Comments
Andrew Strandjord, Ph.D., PacTech-USA, Conference General Chair
9:00am – 9:10am, Cedar Ballroom

Morning Plenary
Silicon Interposer: Much More than a "Piece of Silicon"
Nicolas Sillon, Ph.D., CEA-Leti
9:10am – 10:00am, Cedar Ballroom

Coffee Break
10:00am – 10:30am
Exhibit Hall, Pine/Fir/Oak Ballroom

WLP TRACK

Session 1 – Wafer-Level Testing: Challenges and Solutions
Chair: Ted Tessier, FlipChip International
10:30am – 12:00pm, Monterey

10:30am
Embedded Barrel Spring Probe – Solution for WLCSP Testing ˙%
Frank Zhou, Ph.D., IDI, Smith Group

11:00am
Wafer-Level Testing Challenge for Flip Chip and Wafer-Level Packages ¨*
Muru Yogathasan, STATS ChipPAC, Ltd. speaking on behalf of Lim Kok Hwa, STATS ChipPAC, Ltd.

11:30am
Processing, Bumping and Assembly of Single Chip Plated Ni/Pd Over ALCAP Bond Pads for Flip Chip Applications and Prototyping ¨%%
Brian Lewis, Engent, Inc.

3D TRACK

Session 2 – Process and Materials
Chair: Keith Cooper, SET North America
10:30am – 12:00pm, San Carlos

10:30am
Understanding the Stacked Dies Interface Temperature and its Influence During the 3D IC Thermocompression Stacking Process ¨%&
Robert Daily, IMEC

11:00am
Evaluating Methods of Shipping Thin Silicon Wafers For 3D Stacked Applications ¨˙%+
Richard Allen, SEMATECH

11:30am
3D Packaging- Synthetic Quartz Substrate and Interposers for High Frequency Applications ¨˙&'
Vern Stygar, Asahi Glass Corporation

MEMS TRACK

Session 3 –Wafer Bonding MEMS and Hermeticity Standards
Chair: Russell Shumway, Amkor Technology
10:30am – 12:00pm, Santa Clara

10:30am
Co-Design Strategies for MEMS Packaging ¨&,
Mary Ann Maher, SoftMEMS

11:00am
Yield and Strength of Metal Wafer-Level MEMS Device Sealing Using Al, Au, or Ti ¨" &
Kari Schjølberg-Henriksen, Ph.D., SINTEF ICT

11:30am
Sealing Dispensing for MEMS Wafer Capping ¨" -
Heakyoung Park, Nordson ASYMTEK

Lunch Break
12:00pm to 1:30pm
Exhibit Hall, Pine/Fir/Oak Ballroom

PANEL DISSCUSION
MEMS Integration Strategies: From A Packaging Perspective ¨
1:30pm – 3:00pm, Cedar Ballroom
Moderator: Roger Grace, Roger Grace Associates & Russell Shumway, Amkor Technology
Panelists:
- Matthew Apanius, Desich SMART Center
- Mary Ann Maher, SoftMEMS
- Sean Ding, Ph.D., MEMSIC
- Thava Thavarajah, Fairchild Semiconductor

Coffee Break
3:00pm – 3:30pm
Exhibit Hall, Pine/Fir/Oak Ballroom

WLP TRACK
Session 4 – Wafer-Level Packaging Materials & Process
Chair: Steven Xu, Qualcomm
3:30pm – 5:00pm, Monterey

3:30pm
Low Stress Thick Film Photopatternable Thick Film Silicones for Large Die Wafer-Level Applications ¨¨()
Herman Meynen, Dow Corning Europe S.A.

4:00pm
A New Single Wafer Cleaning Technology for Advanced Packaging Applications ¨) %
Richard Peters, Ph.D., Dynaloy, LLC

4:30pm
Silicone and Cleaning Solvent Compatibility ¨))
Michelle Velderrain, NuSil Technology, LLC

3D TRACK
Session 5 - TSV's and Wafer Thinning
Chair: Peter Ramm, Fraunhofer EMFT
3:30pm – 5:00pm, San Carlos

3:30pm
TSV Process Variations for 2.5D and 3D Semiconductor Packaging ¨* &
Vern Solberg, Invensas Corporation

4:00pm
Single Sided Wet Etching for Thinning, Packaging, and Texturing Applications ¨*-
Ricardo Fuentes, Ph.D., Matech

4:30pm
Deposition Processes for Competitive Through Silicon Via Interposer For 3D ¨+(
Cyprian Uzoh, Invensas, Corporation

MEMS TRACK

Session 6 –MEMS WLP, 3D Integration, and Reliability
Chair: Maaike M.V. Taklo Ph. D., SINTEF ICT
3:30pm – 5:00pm, Santa Clara

3:30pm
Bonding and Contacting of Vertically Integrated 3-D Microscanners ¨, $
Maik Wiemer, Ph.D., Fraunhofer Institute for Electronic Nanosytems (ENAS)

4:00pm
MEMS Hermeticity and Reliability Testing Today ¨, +
Mike Shillinger, Innovative Micro Technology

4:30pm
Reliability of TSV and Wafer-Level Bonding for a 3D Integrable SOI Based MEMS Application¨-'
Maaike M.V. Taklo, Ph.D., SINTEF, ICT

EXHIBITS & WELCOME RECEPTION
5:00pm – 6:00pm
Exhibit Hall, Pine/Fir/Oak Ballroom

KEYNOTE DINNER AND ADDRESS
A Trojan Chip in Your Smartphone? It's Coming...
John Ellis, *bestselling author of 'Dormant Curse'*
Wednesday, November 7, 2012 | 6:00pm - 8:00pm, Cedar Ballroom

IWLPC 2012 CONFERENCE PROGRAM

Thursday, November 8th

Morning Plenary
3D Integration – A Corner Technology for Heterogeneous Integration
Paul Marchal, Ph.D., IMEC
Cedar Ballroom
9:10am – 10:00am

Coffee Break
10:00 – 10:30am
Exhibit Hall, Pine/Fir/Oak Ballroom

WLP TRACK

Session 7 – Wafer-Level Packaging Reliability
Chair: Janet Love, Interconnect Devices, Inc.
10:30am – 12:00pm, Monterey

10:30am
Characterization of eWLB PoP Structures ¨%$-
Tom Strothmann, STATS ChipPAC, Ltd.

11:00am
Marked Reliability Increase of Plastic-Cored Solder Ball for Large Size Wafer-Level CSP ¨%%(
Hiroya Ishida, Sekisui Chemical Co., Ltd.

11:30am
Pad Lift Failure Mode Investigation for Wafer-Level Package ¨%$$
Laurent Gay, STMicroelectronics is not available to speak due to travel restrictions
* Paper and presentation will be available on proceedings

3D TRACK

Session 8 – TSVs and Lithography
Chair: Laurette Nacamulli, Dow Chemical Company
10:30am – 12:00pm, San Carlos

10:30am
3D TSV Micro Cu Pillar Chip-To-Substrate/Chip Assembly/Packaging Technology ¨%&'
Tom Strothman, Ph.D., STATS ChipPAC, Ltd

11:00am
Verification of Back-to-Front Side Alignment for Advanced Packaging ¨%&+
Robert Hsieh, Ph.D., Ultratech, Inc.

11:30am
A Study of a Development Lithography Processes for 3Di Plating Applications ¨% (
Patrick Kearney, P.E., Tokyo Electron Europe, Ltd.

Lunch Break
12:00pm to 1:00pm
Exhibit Hall, Pine/Fir/Oak Ballroom

PANEL DISSCUSION

3D Integration: How Did We Get Here? Where Do We Need To Go Now?
1:00pm – 2:30pm, Cedar Ballroom
Moderator: Keith Cooper, SET North America

Panelists:

- Jeff Calvert, Ph.D., Dow Chemical
- John Lau, Ph.D., Industrial Technology Research Institute (ITRI)
- David Love, Rambus
- Garret Oakes, EV Group
- Peter Ramm, Ph.D., Fraunhofer EMFT
- Tom Strothmann, STATS ChipPAC

Coffee Break
2:30pm– 3:00pm
Conference Foyer

WLP TRACK

Session 9 - Fan-Out Wafer-Level Packaging Technologies
Chair: Curtis Zwenger, Amkor Technology
3:00pm – 5:00pm, Monterey

3:00pm
Innovative 2.5D Solution: Extended/Flip Chip eWLB (Embedded Wafer Level Ball Grid Array) Technology ¨% -
Tom Strothman, STATS ChipPAC, Ltd.

3:30pm
Developments of Fan-Out Wafer-Level Packaging Technology for System-in-Package on Wafer-Level (WLSiP) ¨%()
Jose Campos, NANIUM, S.A.

4:00pm
Adaptive Patterning for Panelized Packaging ¨%) '
Chris Scanlan, Deca Technologies

3D TRACK

Session 10 – 3D Materials and Debonding
Chair: Laurette Nacamulli, Dow Chemical Company
3:00pm – 5:00pm, San Carlos

3:00pm
Optical Profilometry of Substrate Bow Reduction Using Temporary Adhesives ¨%) -
John Moore, Daetec LCC

3:30pm
Wafer Spray Coating for Pre-Applied Underfill ¨%*)
Akira Morita, Nordson ASYMTEK

4:00pm
Equipment and Process Solutions for Low Cost High Volume Manufacturing of 3D Integrated Devices ¨%+%
Garrett Oakes, EV Group, Inc.

5XX]h]cbU` DUdYfg

<YhYfc[YbYci g DUW_U[ ]b[Zcf A 9A G ``%+)
A Uh 5dUb]i g

OA 9A G =bhY[fUh]cb =ggi Yg ``%+, ``
A Ufm 5bb A U\Yf

DUW_U[Y A cXY`]b[cZ A 9A G 8Yj]Wg ``%, %
AA Ub]W_Ua H\Uj UfU'U\ž >c\b 6`cca gVi f[ \ž : U]fVU]`X GYa]Wcb Xi Wcf