Known Good Die 2012

Reducing Costs Through Yield Optimization

Co-located with Roadmaps for Multi Die Integration 2012
MEPTEC Symposium Proceedings Number 52

Santa Clara, California, USA
15 November 2012

ISBN: 978-1-62276-961-2

Printed from e-media with permission by:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571

Some format issues inherent in the e-media version may also appear in this print version.

Copyright© (2012) by MEPTEC
All rights reserved.

Printed by Curran Associates, Inc. (2013)

For permission requests, please contact MEPTEC
at the address below.

MEPTEC
P.O. Box 222
Medicine Park, Oklahoma 73557

Phone: 650-714-1570
Fax: 1-866-424-0130

info@meptec.org

Additional copies of this publication are available from:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: 845-758-0400
Fax: 845-758-2634
Email: curran@proceedings.com
Web: www.proceedings.com

MEPTECPRESENTS
MicroElectronics Packaging and Test Engineering Council

MEPTEC
THE NEXT GENERATION

KNOWN GOOD DIE 2012 – REDUCING COSTS THROUGH YIELD OPTIMIZATION

CONTENTS

Agenda

Sponsor and Exhibitor Directory

Participant Biographies

SESSION ONE: 3D TSV APPLICATIONS

- **3D for the 3C Era 1**
  Abe Yee, Ph.D., Sr. Director Advanced Technology and Package Development, NVIDIA Corporation
- **The KGD Problem: Leveraging Current Solutions for Future Designs 9**
  Terrence Caskey, Ph.D., Sr. Director & Portfolio Manager for 3D Technology, Invensas
- **Known Good Die: More of the Story 20**
  Richard Otte, President, Promex Industries Inc.

SESSION TWO: DESIGN, MANUFACTURING AND TEST OF KGD AND 2.5/3D STACKS

- **Challenges for Known Good Die in the Era of 3D Integration 32**
  W. R. Bottoms, Ph.D., Chairman, 3MTS
- **Known Good Die Revisited: Applied to 3D Stacked ICs 48**
  Bassilios Petrakis, Product Marketing Director, Cadence
- **KGD and 2.5D/3D IC Assembly - Building a Path to Success 63**
  Rich Rice, Senior Vice President of Sales, ASE US, Inc.

KEYNOTE:

- **Using Repair & Redundancy with KGD to Produce Cost Effective 2.5 and 3D Devices 76**
  Robert Patti, Chief Technical Officer and VP of Design Engineering, Tezzaron Semiconductor (Singapore) Pte Ltd.

SESSION THREE: TESTING FOR PERFECTION

- **Enhancing Testability and Yield of KGD in 2.5D/3D ICs Through the Analysis Data from Die-Level Traceability Database 95**
  Mike Alperin, dataPOWER Product Manager, Volume Manufacturing Solutions Marketing, PDF Solutions, Inc.
- **3D & 2.5D Test Challenges: Getting to Known Good Die & Known Good Stack 103**
  Gary Fleeman, Director of Business Development, Advantest Corporation
- **Test Strategies for Wide IO Memory, 3D-TSV Technology Test Vehicles and Ultra Fine Pitch Applications 115**
  Ken Smith, VP Technology Development, Cascade Microtech, Inc.

SESSION FOUR: PANEL – IS KNOWN GOOD DIE A BARRIER TO 3D TSV COMMERCIALIZATION?

Moderator: Linda Matthew, Research Analyst, TechSearch International, Inc.