

DesignCon 2013

Where Chipheads Connect

**Santa Clara, California, USA
28-31 January 2013**

Volume 1 of 2

ISBN: 978-1-62748-472-5

Printed from e-media with permission by:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571



Some format issues inherent in the e-media version may also appear in this print version.

Copyright© (2013) by UBM Electronics
All rights reserved.

Printed by Curran Associates, Inc. (2013)

For permission requests, please contact UBM Electronics
at the address below.

UBM Electronics
303 Second Street
South Tower, 9th Floor, Suite 900
San Francisco, CA 94107

Phone: (415) 947-6000

feedback@techweb.com

Additional copies of this publication are available from:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: 845-758-0400
Fax: 845-758-2634
Email: curran@proceedings.com
Web: www.proceedings.com

TABLE OF CONTENTS

Volume 1

| | |
|--|-----|
| Multi Level Hierarchical Flow for Giga Scale ASIC Designs: 1-TA4 | 1 |
| <i>Kamalpreet Singh</i> | |
| Power/Ground Bump Optimization Technique on Early Design Stage | 18 |
| <i>Youngsoo Lee, Dongyoun Yi</i> | |
| 3D Si Interposer Design and Electrical Performance Study | 34 |
| <i>Mandy (Ying) Ji, Ming Li, Julia Cline, Dave Secker, Kevin Cai, John Lau, Pei-Jer Tzeng, Chau-Jie Zhan, Ching-Kuan Lee</i> | |
| Cracking the Challenge of SoC Low-Power Verification | 57 |
| <i>Thomas L. Anderson</i> | |
| Multi Level Hierarchical Flow for Giga Scale ASIC Designs | 69 |
| <i>Shashank Prasad, Kamal Preet Singh, Matthias Andersch</i> | |
| High-frequency TSV Failure Analysis and Detection Method with Z-parameter | 77 |
| <i>Joohee Kim, Daniel H. Jung, Joungho Kim</i> | |
| How to Improve Power Integrity on Analog-to-Digital Converter (ADC) with Chip-PCB Hierarchical Structure | 99 |
| <i>Bumhee Bae, Jonghyun Cho, Sunkyu Kong, Jonghoon J. Kim, Yujeong Shim, Joungho Kim</i> | |
| Behavioral Modeling Approaches for Analog, Mixed-Signal and RF | 123 |
| <i>Helene Thibieroz</i> | |
| UPF based Verification for Mixed-Signal Sign-Off Using UVM-MS | 128 |
| <i>Ravi Surepeddi</i> | |
| Mixed RF-Digital Design-to-Test Framework for Power Amplifier Digital Predistortion | 141 |
| <i>Takao Inoue</i> | |
| Applying Microwave Techniques to Digital Systems: A Simple Case Study | 157 |
| <i>Andrew Becker, Michael Higgins, Michael Steinberger, Paul Wildes</i> | |
| Enabling DFT Logic and Timing Verification in Mixed-Signal Designs | 180 |
| <i>Bing Chuang, Kaneez Tumpa</i> | |
| A Rapid Prototyping of FPGA-Based Duobinary Transmitter/Receiver for High Speed Electrical Backplane Transmission | 197 |
| <i>Ashraf Umar, Aldo Morales, Sedig Agili, Mike Resso, Marcel Christoph Welpot</i> | |
| Accelerating Automated Test and Protocol Aware ATE Through Open FPGA-Based Solutions | 210 |
| <i>Ryan Mosley</i> | |
| Modeling, Simulation, and Implementation of High Power Inverter Plants and FPGA-based Controllers | 231 |
| <i>Brian Maccleery, Oleg Stepanov, Lee Johnston, Matt Spexarth, Mahmoud Wahby, Muris Mujagic, Jesse Ormston</i> | |
| A Reusable Generic Platform for Validation and Characterization of High Speed Mixed Signal Designs | 248 |
| <i>Sanku Mukherjee, Narayanan Mayandi, Brian Tsang, Sreeja Menon, Benedict Lau, Norman Chan, Arul Sendhil</i> | |
| Reliability Modeling of Electronics for Co-Designed System Applications | 273 |
| <i>Greg Caswell</i> | |
| Advances in Onboard Optical Interconnects: A New Generation of Miniature Optical Engines | 289 |
| <i>Jean-Marc Verdiell</i> | |
| Thermal Co-analysis of 3D-IC/Packages/System | 316 |
| <i>Stephen H. Pan, Norman Chang, Mark Qi Ma, Gokul V. Shankaran, Manoj Nagulapally</i> | |
| Platform Enabling Interposer (PEI) DDR3L Memory Design Challenges and Solutions | 339 |
| <i>Bo Yu, Lomberto P Jimenez</i> | |
| Cross-interface Full Channel Analysis | 353 |
| <i>Yinglei Ren, Weifeng Shu, Kai Xiao, Adrian Grigoras</i> | |
| Using Power Aware IBIS v5.0 Behavioral IO Models to Simulate Simultaneous Switching Noise | 371 |
| <i>Romi Mayder, Chris Wyland, Bradley Brim, Yingxin Sun</i> | |
| High Speed Signal Path Losses as Related to PCB Laminate Type and Copper Roughness | 393 |
| <i>Lee Ritchey, John Zasio, Rich Pangier, Gerry Partida</i> | |
| Analytic Solutions for Periodically Loaded Transmission Line Modeling | 409 |
| <i>Priya Pathmanathan, Paul G. Huray, Steven G. Pytel</i> | |
| Accurate Insertion Loss and Impedance Modeling of PCB Traces | 431 |
| <i>Jeff Loyer, Andy Burkhardt, Richard Kunze, Richard Attrill</i> | |

| | |
|--|-----|
| Humidity and Temperature Effects on PCB Insertion Loss | 450 |
| <i>Jeff Loyer, Richard Kunze, Gary Brist</i> | |
| Which One is Better? Comparing Options to Describe Frequency Dependent Losses | 469 |
| <i>Eric Bogatin, Don Degroot, Paul G. Huray, Yuriy Shlepnev</i> | |
| Zen and the Collaborative Art of Designing, Manufacturing and Implementing Low-Loss, High Speed Flex Interconnects | 495 |
| <i>Glenn Oliver, Matt Doyle, Rick Brandwein, John Dangler, Paul Abrahamson</i> | |
| Effects of Temperature and Relative Humidity in Transmission Systems Using Differential Signaling | 520 |
| <i>Aldo Morales, Sedig Agili, Mike Resso, Jeff Clark, Chris Kocuba</i> | |
| Modeling and Optimization of High Speed Interconnects for Signal and Power Integrity | 537 |
| <i>Antonio Ciccomancini, Darryl Kostka, Mauro Lai, Jonathan Casanova, Madhumitha Seshadhri</i> | |
| Improving Circuit Board Reliability During the Schematic Capture Process with a Rules Based Automated Checker | 584 |
| <i>Kai Keskinen, Vance Bolling, Geoff Liu</i> | |
| Channel to Channel Crosstalk Behavior and Design Optimization for DDR4 Signaling | 598 |
| <i>Xiang Li, James McCall</i> | |
| Implementing Embedded Active Components | 612 |
| <i>Per Viklund</i> | |
| Determining PCB Trace Impedance by TDR: Challenges and Possible Solutions | 629 |
| <i>Istvan Novak, Ying Li, Eben Kunz, Sarah Paydavosi, Laura Kocubinski, Kevin Hinckley, Alexander Nosovitski, Nathaniel Shannon, Jason Miller, Gustavo Blando</i> | |
| Si-interposer Design for GPU-Memory Integration Concerning the Signal Integrity | 656 |
| <i>Jonghyun Cho, Joohee Kim, Hyun-Cheol Bae, Kwangseong Choi, Seungwook Paek, Lee-Sup Kim, JoungHo Kim</i> | |
| DDR Memory Channel Design from Passive Stub Equalizer Perspective | 676 |
| <i>Jongbae Park, Myunghyun Ha, Qin Li</i> | |
| Robust I/O Circuit Scheme for World's First Over 1.6Gbps LPDDR3 | 696 |
| <i>Kyounghoi Koo, Woong Hwan Ryu, Sang Min Lee, Baek Kyu Choi</i> | |
| A 256GB/s Memory Subsystem Built Using a Double-Sided IC Package with a Memory Controller and 3D-Stacked DRAM | 713 |
| <i>Scott Best, David Secker, Thomas Giovannini, Don Mullen, Ming Li, Mandy Ji</i> | |
| Accurate Receiver Clock Positioning in High-Speed Parallel Buses | 721 |
| <i>Arun Vaidyanath, Dan Oh, Chris Madden, Yohan Frans, Woopoung Kim</i> | |
| Pushing Mobile Memories Beyond the Smart Phone Envelope | 742 |
| <i>John Ellis</i> | |
| World's first LPDDR3 Enabling for Mobile Application Processors System | 764 |
| <i>Chanmin Jo, Baekkyu Choi, Sangmin Lee, Seongjae Moon, Seungbae Lee, Minho Seo, Yonghoon Kim</i> | |
| Fast, Efficient and Accurate: Via Models That Correlate to 20 GHz | 782 |
| <i>Michael Steinberger, Eric Brock, Donald Telian</i> | |
| Signal and Power Integrity (SPI) Co-Analysis for High-Speed Communication Channels | 807 |
| <i>Renato Rimolo-Donadio, Xiaomin Duan, Young H. Kwark, Xiaoxiong Gu, Christian W. Baks, Sebastian Müller, Thomas-Michael Winkel, Thomas Strach, Lei Shan, Hubert Harrer, Christian Schuster</i> | |
| Time Domain and Statistical Model Development, Simulation and Correlation Methods for High Speed SerDes | 832 |
| <i>Xingdong Dai, Fangyi Rao, Shiva Prasad Kotagiri, John Baprawski, Cathy Ye Liu</i> | |
| End to End Link Analysis and Optimization with Mid-channel-redrivers AMI Models | 852 |
| <i>Mahbulul Bari, Ron Olisar, Hassan Rafat, Fangyi Rao, Sharon (Xiaohua) Wang, Ming Yan</i> | |
| Channel Operating Margin (COM): Evolution of Channel Specifications for 25 Gbps and Beyond | 867 |
| <i>Richard Mellitz, Adeee Ran, Mike Peng Li, Vira Ragavassamy</i> | |
| Acquisition & Analysis of High-Speed Serial Statistical Eyes at the Sampling Point in a Receiver | 887 |
| <i>Mike Jenkins, David Mahashin</i> | |
| SI and EMI Impact of AC Coupling Capacitors on 25Gbps+ Systems | 897 |
| <i>Xin Wu, Casey Morrison, Bhavesh Patel, Raghav Nallan Chakravarthi, Peerouz Amleshi</i> | |
| Beyond 25 Gbps: A Study of NRZ & Multi-Level Modulation in Alternative Backplane Architectures | 940 |
| <i>Adam Healey, Chad Morgan, Megha Shanbhag</i> | |
| Performance Sensitivity to Package Manufacturing Tolerance and Material Properties in System for 25Gbps and Beyond | 965 |
| <i>Xiaohong Jiang, Hong Shi, Siow Chek Tan</i> | |

Volume 2

| | |
|--|------|
| Practical Receiver Equalization Tradeoffs Applicable to Next-Generation 28 Gb/s Links with 20–35 dB Loss Channels | 984 |
| <i>Edward Frlan, Francois Tremblay</i> | |
| A Study on Crosstalk Impact on System SNR and BER | 1005 |
| <i>Henry Wong, Xiaoqing Dong, Vincent Huang, Clarence Yu, Francois Tremblay, Geoffrey Zhan</i> | |
| Power Supply Noise Induced Jitter Estimation in High Speed Clock Tree for Full Chip Timing Analysis | 1039 |
| <i>Wen Yin, Zegui Pang, Wei Liu, Tonghao Ding, Erik Breiland</i> | |
| Statistical BER Analysis due to Supply Voltage Fluctuations at a Single-Ended Buffer | 1052 |
| <i>Jingook Kim, Dongil Shin, Junho Lee, Sunki Cho, Chulsoon Hwang, Jun Fan</i> | |
| Dramatic Noise Reduction using Guard Traces with Optimized Shorting Vias | 1072 |
| <i>Eric Bogatin, Lambert (Bert) Simonovich</i> | |
| Measurement-based Simulation: Increasing IBIS-AMI Model Accuracy with Data from Lab Measurements | 1105 |
| <i>Michael Steinberger, Paul Wildes, Anders Ekholm, Nicke Svee</i> | |
| Analysis and Decomposition of Duty Cycle Distortion from Multiple Sources | 1130 |
| <i>Daniel Chow, Shufang Tian, Yanjing Ke, Kaiyu Ren</i> | |
| Understanding Apparent Increasing Random Jitter with Increasing PRBS Test Pattern Lengths | 1143 |
| <i>Martin Miller</i> | |
| Partial Response and Noise Predictive Maximum Likelihood (PRML/NPML) Equalization and Detection for High Speed Serial Link Systems | 1160 |
| <i>Pervez M. Aziz, Cathy Ye Liu, Adam Healey</i> | |
| IBIS-AMI Model-to-Hardware Correlation | 1185 |
| <i>Greg Edlund</i> | |
| Comparison of Two Statistical Methods for High Speed Serial Link Simulation | 1205 |
| <i>Masashi Shimanouchi, Mike Peng Li, Hsinho Wu</i> | |
| On the Validity of Lumped Jitter Approximation in the Statistical Analysis of SerDes | 1222 |
| <i>Mohammad S. Mobin, Amaresh Malipatil, Cathy Liu, Chintan Desai, Adam Healey</i> | |
| Design and Analysis of a High-Speed Parallel Interface for 16 Gbps Coded Differential Signaling | 1248 |
| <i>Wendemagegnehu T. Beyene, Amir Amirkhany, Kambiz Kaviani, Aliazam Abbasfar</i> | |
| Partial Response and Noise Predictive Maximum Likelihood (PRML/NPML) Equalization and Detection for High Speed Serial Link Systems | 1265 |
| <i>Pervez M. Aziz, Cathy Ye Liu, Adam Healey</i> | |
| Innovative PDN Design Guidelines for Practical High Layer-Count PCBs | 1290 |
| <i>Ketan Shringarpure, Siming Pan, Jingook Kim, Brice Achkir, Bruce Archambeault, Jun Fan, James Drowniak</i> | |
| An Efficient Power Integrity Design Methodology to Prevent Platform Failures for High Density Designs | 1315 |
| <i>Vira Ragavassamy, Jiangqi He, Arul Kandasamy, Y. L. Li</i> | |
| Interactions-between Power-Planes-and Power-Planes to Traces in Power-Integrity-Issues | 1329 |
| <i>Joachim Held, Richard Sjiariel</i> | |
| Noble PDN Design of Maximum Allowable Target Impedance for Multi-GHz Mobile Application Processor Platforms | 1344 |
| <i>Seungbae Lee, Seil Kim, Jeongmin Jo, Jungman Lim</i> | |
| Supply Noise Simulation and Correlation for a Multi-GHz High-Speed Serial Link | 1359 |
| <i>Suzanne L. Huh, Xiaoping Liu, Vishram Pandit</i> | |
| Efficient Symbolic Circuit Analysis Based Transfer Functions and Input Impedance Computations for Core- Power Delivery Network with VRM | 1371 |
| <i>Om P. Mandhana</i> | |
| Memory Interface On-chip PDN Noise Characterization, Modeling and Its Impact on Timing | 1409 |
| <i>Bipin Dhavale, Yuri Tretiakov, Shishuang Sun, Sunitha Chandra, June Feng, Daniel Chow, Janani Chandrasekhar, Aman Aflaki, Mayra Sarmiento</i> | |
| Power-Signal Co-integrity Design for Multi-Gbps Low-Power DDR3 Mobile Platforms | 1426 |
| <i>Weiliang Yuan, Seungbae Lee, Chan-Min Jo, Woong Hwan Ryu, Sangmin Lee</i> | |
| Validating EMC Simulation by Measurement in Reverberation Chamber | 1447 |
| <i>Xiaoxia Zhou, Jing Li, Hongmei Fan, Alpesh Bhobe, Kam Taunk, Jinghan Yu, Philippe Sochoux</i> | |
| Effects of Nearby Ground Vias on High Speed Single-ended and Differential Signals | 1469 |
| <i>Alma Jaze, Bruce Archambeault, Samuel Connor</i> | |
| EMI Susceptibility and Reliability of Quartz- and MEMS-based Oscillator Components | 1495 |
| <i>Yin-Chen Lu, Jehangir Parvereshi, Sassan Tabatabaei</i> | |

| | |
|---|------|
| Mode Conversion: Missing Parameters in Understanding Alien Crosstalk of LAN Cabling for Higher Speed Ethernet | 1507 |
| <i>Christopher Diminico, Mike Resso, Mike Sapozhnikov</i> | |
| Innovative Defense Techniques for Damping Digital to RF Crosstalk | 1529 |
| <i>Davy Pissoort, Hany Fahmy, Mehdi Mechaik, Henry Zeng, Charlie Shu, Charles Jackson, Jan Van Hese</i> | |
| Design and Experimental Validation of Compact Common Mode Filter Based on EBG Technology | 1551 |
| <i>Xiaoxiong Gu, Renato Rimolo-Donadio, Young H. Kwark, Christian Baks, Francesco De Paulis, Muhammet Hilmi Nisanci, Antonio Orlandi, Bruce Archambeault, Samuel Connor</i> | |
| Methods of Improving 3D EM Model Development and Associated Time/Frequency Domain Measurements | 1573 |
| <i>Jim Bell, Al Neves, Bob Buxton, Jon Martens, Josiah Bartlett</i> | |
| Skew in Twin-axial Cables and its Significance in Next Generation Differential Signaling | 1653 |
| <i>Munawar Ahmad, Mark Bugg, Greg Fitzgerald, Michael Rost</i> | |
| A Removable Signal Probing and Monitoring Solution for Gigabit Memory ATE Applications | 1669 |
| <i>José Moreira, Marc Mössinger, Tom Bresnan, Masayuki Takahashi</i> | |
| High-Throughput, High-Sensitivity Measurement of Power Supply-Induced Bounded, Uncorrelated Jitter in Time, Frequency, and Statistical Domains | 1692 |
| <i>Daniel Chow, Yujeong Shim, Shishuang Sun</i> | |
| Tips and Advanced Techniques for Characterizing a 28 Gb/s Transceiver | 1704 |
| <i>Jack Carrel, Robert Sleigh, Heidi Barnes, Hoss Hakimi, Mike Resso</i> | |
| A Fast and Inexpensive Method for PCB Trace Characterization in Production Environments | 1735 |
| <i>Peter J. Pupalakis, Kaviyesh Doshi</i> | |
| Impact of Probe Coupling on the Accuracy of Differential VNA Measurements | 1762 |
| <i>Sarah Paydavosi, Laura Kocubinski, Jason Miller, Gustavo Blando, Eugene R. Whitcomb, Istvan Novak</i> | |
| Terabit/s Packaging Design for Testing of High-Speed IC Transceivers | 1786 |
| <i>Christian Baks, Renato Rimolo-Donadio, Young H. Kwark, Fuad E. Doany, Xiaoxiong Gu, Daniel M. Kuchta, Benjamin G. Lee, Alexander V. Rylyakov, Frank Libsch, Clint L. Schow</i> | |
| Modeling High-Speed Interconnect for the the Signal Integrity Engineer: Tips, Tricks, and Tradeoffs | 1807 |
| <i>John Dunn</i> | |
| Elements of Decompositional Electromagnetic Analysis of Interconnects | 1837 |
| <i>Yuriy Shlepnev</i> | |
| Numerically Robust, Fast and Accurate Method of Combining Linear Models of Arbitrary Topology Into a Single S-parameter Model | 1917 |
| <i>Vladimir Dmitriev-Zdorov, Scott McMorrow</i> | |
| A Reverse Nyquist Approach to Understanding the Importance of Low Frequency Information in Scattering Matrices | 1937 |
| <i>Daniel Dvorscak, Michael Tsuk</i> | |
| Challenges and Solutions in Characterizing a 10 Gb Device | 1949 |
| <i>Brian Fetz, Daniel Rubusch, Rob Sleigh</i> | |
| Author Index | |