

# **2013 5th Asia Symposium on Quality Electronic Design**

**(ASQED 2013)**

**Penang, Malaysia  
26-28 August 2013**



**IEEE Catalog Number: CFP1383H-POD  
ISBN: 978-1-4799-1313-8**

# 5th Asia Symposium on Quality Electronic Design 2013

## Table of Contents

### Keynote

<b>A Possibility of Crystalline Indium-Gallium-Zinc-Oxide</b> .....	1
Shunpei Yamazaki, Semiconductor Energy Laboratory Co., Ltd.,	

### SESSION 1A Analog Circuits

Chair: Edward Ho, Qualcomm

<b>A Wideband Multi-Stage Inverter-Based Driver Amplifier for IEEE 802.22 WRAN Transmitters</b> .....	6
Geng-Zhen Qi, Ka-Fai Un, Wei-Han Yu, Pui-In Mak, Rui P. Martins, University of Macau	
<b>A 128-phase Delay-Locked Loop with Cyclic VCDL</b> .....	10
Chien-Hung Kuo and Yu-Chieh Ma, National Taiwan Normal University	
<b>A Fast Transient Response Synchronous Buck Converter with Modified Ripple-Based Control (MRBC) Technique</b> .....	14
Yunwu Zhang, Jing Zhu, Weifeng Sun, Yangbo Yi, Southeast University	
<b>Ultra Low-Supply Voltage Reference Generator with Low Sensitivity to PVT Variations</b> .....	18
Hande Vinayak Gopal <sup>1</sup> , Praful Gupta <sup>2</sup> , Maryam Shojaei Baghini <sup>1</sup> , <sup>1</sup> IIT Bombay, <sup>2</sup> IIT Rajasthan	

### SESSION 1B Test & Design for Test

Chair: Otmane Ait Mohamed, Concordia University

<b>Detecting Resistive-Opens in RRAM Using Programmable DFT Scheme</b> .....	22
Nor Zaidi Haron <sup>1</sup> , Norsuhaidah Arshad <sup>1</sup> , Sukreen Hana Herman <sup>2</sup> , <sup>1</sup> Universiti Teknikal Malaysia Melaka, <sup>2</sup> Universiti Teknologi MARA	
<b>A Coverage Driven Test Generation Methodology Using Consistency Algorithm</b> .....	27
Jomu George Mani Paret and Otmane Ait Mohamed, Concordia University	
<b>Improved Test Methodology for Multi-Clock Domain SoC ATPG Testing</b> .....	33
Ee Mei Ooi and Chin Hai Ang, Altera Corporation (M) Sdn Bhd	
<b>On Using IEEE 1500 Standard for Functional Testing</b> .....	39
Ghazanfar Ali, Fawnizu Azmadi Hussin, Noohul Basheer Zain Ali, Nor Hisham Hamid, Universiti Teknologi Petronas	

### SESSION 1C Sensors & Nanoelectronics

Chair: Ramgopal Rao, IIT Bombay

<b>Ultra-sensitive Polymeric Sensor Platforms for Environmental Sensing Applications</b> .....	47
Prasenjit Ray, Harshil Raval, V. Ramgopal Rao, IIT Bombay	
<b>A Low Power Oscillator Based Temperature Sensor for RFID Applications</b> .....	50
Saqib Mohamad <sup>1</sup> , Fang Tang <sup>2</sup> , Abbas Amira <sup>3</sup> , Amine Bermak <sup>2</sup> , Mohieddine Benammar <sup>4</sup> , <sup>1</sup> HKUST/Qatar University, <sup>2</sup> HKUST, <sup>3</sup> University of West of Scotland, <sup>4</sup> Qatar University	
<b>Design and Simulation of Clamped-Clamped and Clamped-Free Resonators</b> .....	55
Ahmad Anwar Zainuddin <sup>1</sup> , Jamilah Karim <sup>2</sup> , Anis Nurashikin Nordin <sup>2</sup> , Mohanraj Soundara Pandian <sup>1</sup> , Sheroz Khan <sup>2</sup> , <sup>1</sup> Silterra, <sup>2</sup> IIUM	
<b>On Testing of MEDA Based Digital Microfluidics Biochips</b> .....	60
Vineeta Shukla <sup>1</sup> , Noohul Basheer Zain Ali <sup>1</sup> , Fawnizu Azmadi Hussin <sup>1</sup> , Mark Zwolinski <sup>2</sup> , <sup>1</sup> Universiti Teknologi Petronas, <sup>2</sup> University of Southampton	

### SESSION 2A Digital VLSI

<b>Applications of Crystalline Indium-Gallium-Zinc-Oxide Technology to LSI: Memory, Processor, Image Sensor, and Field Programmable Gate Array (Invited)</b> .....	66
Yoshiyuki Kurokawa <sup>1</sup> , Yuki Okamoto <sup>1</sup> , Takashi Nakagawa <sup>1</sup> , Takeshi Aoki <sup>1</sup> , Masataka Ikeda <sup>1</sup> , Munehiro Kozuma <sup>1</sup> , Takeshi Osada <sup>1</sup> , Takayuki Ikeda <sup>1</sup> , Naoto Yamada <sup>1</sup> , Yutaka Okazaki <sup>1</sup> , Hidekazu Miyairi <sup>1</sup> , Masahiro Fujita <sup>2</sup> , Jun Koyama <sup>1</sup> , Shunpei Yamazaki <sup>1</sup> <sup>1</sup> Semiconductor Energy Laboratory Co., Ltd., <sup>2</sup> University of Tokyo	

<b>Totally Self-Checking (TSC) VLSI Circuits using Scalable Error Detection Coding (SEDC) Technique</b> .....	72
Natarajan Somasundaram <sup>1</sup> , Farhad Mehdipour <sup>2</sup> , Jeong-A Lee <sup>3</sup> , Narayanadass Ramadass <sup>4</sup> , Y V Ramana Rao <sup>4</sup> , <sup>1</sup> SSM College of Engineering, <sup>2</sup> Kyushu University, <sup>3</sup> Chosun University, <sup>4</sup> Anna University	
<b>A Robust and Energy Efficient Pulse Generator for Ultra-Wide Voltage Range Operations</b> .....	80
Sébastien Bernard <sup>1</sup> , David Bol <sup>2</sup> , Alexandre Valentian <sup>3</sup> , Marc Belleville <sup>3</sup> , Jean-Didier Legat <sup>2</sup> , <sup>1</sup> CEA-LETI/ICTEAM-UCL, <sup>2</sup> ICTEAM-UCL, <sup>3</sup> CEA-LETI	
<b>Optimized Clock Gating Cell for Low Power Design in Nanoscale CMOS Technology</b> .....	85
Aniryudh Reddy Durgam and Ken Choi, Illinois Institute of Technology	

## SESSION 2B Design Solutions

<b>High-Quality Data Assignment to Hierarchical Memory Organizations for Multidimensional Signal Processing</b> .....	89
Florin Balasa <sup>1</sup> , Ilie I. Luican <sup>2</sup> , Doru V. Nasui <sup>3</sup> , <sup>1</sup> American University in Cairo, <sup>2</sup> Microsoft Inc., <sup>3</sup> American International Radio Inc.	
<b>Congestion-Oriented Approach in Placement for Analog and Mixed-Signal Circuits</b> .....	97
Hongxia Zhou <sup>1</sup> , Chiu-Wing Sham <sup>1</sup> , Hailong Yao <sup>2</sup> , <sup>1</sup> The Hong Kong Polytechnic University, <sup>2</sup> Tsinghua University	
<b>Tunable Stochastic Computing Using Layered Synthesis and Temperature Adaptive Voltage Scaling</b> .....	103
Neel Gala <sup>1</sup> , VR Devanathan <sup>2</sup> , Vish Visvanathan <sup>2</sup> , Virat Gandhi <sup>1</sup> , Veezhinathan Kamakoti <sup>1</sup> , <sup>1</sup> IIT-Madras, <sup>2</sup> Texas Instruments-India	
<b>Rapid Search of Pareto Fronts using D-logic Exploration during Multi-Objective Tradeoff of Computation Intensive Applications</b> .....	113
Anirban Sengupta <sup>1</sup> , Vipul Kumar Mishra <sup>1</sup> , Pallabi Sarkar <sup>2</sup> , <sup>1</sup> Indian Institute of Technology Indore, <sup>2</sup> Vellore Institute of Technology Chennai	

## SESSION 2C Advanced Packaging: Signal Integrity & 3D Technologies

<b>A New TSV Set Architecture for High Reliability</b> .....	123
Jaeseok Park and Sungho Kang, Yonsei University	
<b>Heterogeneous Stacking of 3D MPSoC Architecture: Physical Implementation Analysis and Performance Evaluation</b> .....	127
Mohamad Hairol Jabbar <sup>1</sup> , Dominique Houzet <sup>2</sup> , Omar Hammami <sup>3</sup> , <sup>1</sup> UTHM, Johor, <sup>2</sup> GIPSA-Lab, <sup>3</sup> ENSTA PARISTECH	
<b>Port Assignment for Multiplexer and Interconnection Optimization</b> .....	136
Cong Hao <sup>1</sup> , Hao-Ran Zhang <sup>2</sup> , Song Chen <sup>3</sup> , Takeshi Yoshimura <sup>2</sup> , Min-You Wu <sup>1</sup> , <sup>1</sup> Shanghai Jiao Tong University, <sup>2</sup> Waseda University, <sup>3</sup> University of Science and Technology of China	
<b>Full System Power Delivery Analysis for Single Ended Interface</b> .....	144
Heng Chuan Shu, Bok Eng Cheah, Jackson Kong, Sze Geat Pang, Li Chuang Quek, Intel Microelectronics (M) Sdn. Bhd.	

## SESSION P Poster Papers

<b>External Loopback Testing on High Speed Serial Interface</b> .....	148
Shen Shen Lee, ALTERA	
<b>Repairing of Faulty TSVs Using Available Number of Multiplexers in 3D ICs</b> .....	155
Surajit Kumar Roy, Sobitri Chatterjee, Chandan Giri, Hafizur Rahaman, Bengal Engineering and Science University	
<b>Innovative Solutions for Package on Package Test</b> .....	161
Chin Chien Tee and Siang Soh, Interconnect Devices, Inc	
<b>Simulation and Modeling of Heat-Dissipation Packaging for Nanoscale GaInP/GaAs Collector-Up HBTs</b> .....	167
Jhin-Fong-Chin Chang and Hsien-Cheng Tseng, Kun Shan University	
<b>Methods of Optimized Via Design for Higher Channel Bandwidth</b> .....	170
Chang Fei Yee, Agilent Technologies	

<b>Breakthrough of Micro USB Placement in Printed Circuit Board .....</b>	<b>178</b>
Kent Lee, Huoy Thyng Yow, Oliver Hooi, Motorola Solutions	
<b>Variability Aware Performance Evaluation of Low Power SRAM Cell .....</b>	<b>183</b>
Hansel Dsilva, Julian Pinto, Arzan Elchidana, Sudhakar Mande, Mumbai University	
<b>Distortion Analysis and Calculation of Wide-band Track and Hold Amplifier .....</b>	<b>188</b>
Hailang Liang <sup>1</sup> , Jin He <sup>1</sup> , Rob.J. Evans <sup>2</sup> , Efstratios Skafidas <sup>2</sup> , Cheng Wang <sup>1</sup> , Qingxing He <sup>3</sup> , Caixia Du <sup>3</sup> , Shengju Zhong <sup>3</sup> , <sup>1</sup> Peking University, <sup>2</sup> University of Melbourne, <sup>3</sup> Shenzhen Huayue Terascale Chip Co. LTD.	
<b>Multiobjective Evolutionary Approach to Silicon Solar Cell Design Optimization .....</b>	<b>192</b>
Wen-Tsung Huang, Chieh-Yang Chen, Yu-Yu Chen, Sheng-Chia Hsu, Yiming Li, National Chiao Tung University	
<b>An Electrical Study of Differential Clock Die-to-Die Interconnection in Multi-chip Packages .....</b>	<b>196</b>
Tang Min Keen and Tan Wei Jern, Intel Microelectronics	
<b>Cluster-Based Thermal-Aware 3D-Floorplanning Technique with Post-Floorplan TTSV Insertion at Via-Channels .....</b>	<b>200</b>
Chia-Chen Wen, Ying-Jung Chen, Shanq-Jang Ruan, National Taiwan University of Science and Technology	
<b>Oscillation Built-in-Self-Test for ADC Linearity Testing in Deep Submicron CMOS Technology .....</b>	<b>208</b>
Koay Soon Chan <sup>1</sup> , Nuzrul Fahmi <sup>1</sup> , Kim Chon Chan <sup>1</sup> , Terk Zyou Lok <sup>1</sup> , Chee Wai Yong <sup>1</sup> , Adam Osseiran <sup>2</sup> , <sup>1</sup> Marvell Semiconductor Sdn. Bhd., <sup>2</sup> Edith Cowan University	

### SESSION 3A ADC and Memory Readout

Chair: Kim Tae Hyoung, Nanyang Technological University

<b>A 2.93<math>\mu</math>W 8-Bit Capacitance-to-RF Converter for Movable Laboratory Mice Blood Pressure Monitoring .....</b>	<b>216</b>
Ka-Meng Lei, Pui-In Mak, Man-Kay Law, R. P. Martins, University of Macau	
<b>A 1.8 V 64.9 <math>\mu</math>W 54.1 dB SNDR 1st Order <math>\Sigma\Delta</math> Modulator Design Using Clocked Comparator Based Switched Capacitor Technique .....</b>	<b>220</b>
Sourav Chakraborty, Manodipan Sahoo, Hafizur Rahaman, Bengal Engineering and Science University, Shibpur	
<b>Highly Robust and Sensitive Charge Transfer Sense Amplifier for Ultra-Low Voltage DRAMs .....</b>	<b>227</b>
Choongkeun Lee and Hongil Yoon, Yonsei University	
<b>Digitally Controlled Variation Tolerant Timing Generation Technique for SRAM Sense Amplifiers .....</b>	<b>233</b>
Viveka K R and Bharadwaj Amrutur, IISc Bangalore	

### SESSION 3B 3D Design Solutions

Chair: Abbas Amira, University of West of Scotland

<b>Implementation of a Physical Unclonable Function (PUF) with Transmission Line Crosstalk in a Chip (Invited) .....</b>	<b>240</b>
Kyoungrok Cho, Kwan-Hee Lee, Seung-Yul Kim, Sang-Jin Lee, Younggap You, Chungbuk National University	
<b>Simultaneous Hotspot Temperature and Supply Noise Reductions using Thermal TSVs and Decoupling Capacitors .....</b>	<b>245</b>
Yan-Wun Wang, Pao-Jen Huang, Tai-Chen Chen, Chien-Nan Jimmy Liu, National Central University	
<b>Exploration of 2D EDA Tool Impact on the 3D MPSoC Architectures Performance .....</b>	<b>249</b>
Mohamad Hairol Jabbar <sup>1</sup> , Abir Mzah <sup>2</sup> , Omar Hammami <sup>2</sup> , Dominique Houzet <sup>3</sup> , <sup>1</sup> FKEE, UTHM, Johor, <sup>2</sup> ENSTA PARISTECH, <sup>3</sup> GIPSA-Lab	
<b>Path Resistance Reduction through Automated Multi-Level Metal and Via Insertion for IC Layout Design .....</b>	<b>256</b>
Thai Lee Lo, Gregory Sylvester Emmanuel, Thomas Fong Chee Goh, Chun Keong Lee, Joon Heong Ong, Yng Chuk Tam, Jonathan Yoong-Seang Ong, Hui Peng Ong, Spansion Penang Sdn Bhd	

### SESSION 3C Advanced Device Topics

<b>An ABCD Parameter-based Modeling and Analysis of Crosstalk Induced Effects in Single-Walled Carbon Nanotube Bundle Interconnects</b> .....	264
Manodipan Sahoo, Prasun Ghosal, Hafizur Rahaman, Bengal Engineering and Science University, Shibpur	
<b>The Effects of Elliptical Gate Cross Section on Carbon Nanotube Gate-All-Around Field Effect Transistor</b> .....	274
Hao Wang <sup>1</sup> , Sheng Chang <sup>1</sup> , Cheng Wang <sup>1</sup> , Yue Hu <sup>1</sup> , Hongyu He <sup>1</sup> , Jin He <sup>1</sup> , Qingxing He <sup>2</sup> , Caixia Du <sup>2</sup> , Shengju Zhong <sup>2</sup> , <sup>1</sup> Peking University, <sup>2</sup> Shenzhen Huayue Terascale Chip LTD.Co.	
<b>Study on Silicon Window Polarity of Partial-SOI LDMOS Power Devices</b> .....	278
Yue Hu <sup>1</sup> , Hao Wang <sup>1</sup> , Cheng Wang <sup>1</sup> , Jin He <sup>1</sup> , Xiaoan Zhu <sup>1</sup> , Sheng Chang <sup>2</sup> , Qijun Huang <sup>2</sup> , Dewen Wang <sup>3</sup> , Qingxing He <sup>4</sup> , Caixia Du <sup>4</sup> , Shengju Zhong <sup>4</sup> , <sup>1</sup> Peking University, <sup>2</sup> Wuhan University, <sup>3</sup> Shenzhen SI Semiconductors, <sup>4</sup> Shenzhen Huayue Terascale Chip	

### SESSION 4A Special Topics in Circuit and System Design

<b>A Low-Power Circuit Architecture for Transistor Electrical Overstress (EOS) Protection</b> .....	282
Chee Hong Aw, Intel Microelectronics (M) Sdn. Bhd.	
<b>Computationally Efficient Methodology for Statistical Characterization and Yield Estimation due to Inter- and Intra-die Process Variations</b> .....	287
Sudhakar Mande <sup>1</sup> , Arun Chandorkar <sup>2</sup> , Hiroshi Iwai <sup>3</sup> , <sup>1</sup> Don Bosco Institute of Technology, Kurla, <sup>2</sup> Indian Institute of Technology, Powai, <sup>3</sup> Tokyo Institute of Technology	
<b>On Improving at No Cost the Quality of Products Built with SRAM-based FPGAs</b> .....	295
Regis Leveugle and Mohamed Ben Jrad, Grenoble Institute of Technology / TIMA	

### SESSION 4B Test & Verification

Chair: Chin Hai Ang, Altera Corporation (M) Sdn Bhd

<b>Mu-GSIM: A Mutation Testing Simulator on GPUs</b> .....	302
Jason Tong <sup>1</sup> , Marc Boulé <sup>2</sup> , Zeljko Zilic <sup>1</sup> , <sup>1</sup> McGill University, <sup>2</sup> École de Technologie Supérieure	
<b>Logic Emulation with Forced Assertions: A Methodology for Rapid Functional Verification and Debug</b> .....	312
Somnath Banerjee, Tushar Gupta, Sanjay Gupta, Mentor Graphics Pvt. Ltd.	
<b>Online Error Detection in SRAM based FPGAs using Scalable Error Detection Coding</b> .....	321
Zahid Ali Siddiqui and Jeong-A Lee, Chosun University	
<b>An Efficient Metric for Detecting Timing Failure Region Due to Crosstalk Noise</b> .....	
Hyoeeon Yang and Young Hwan Kim, POSTECH 325	

### SESSION 4C Advanced Packaging: Thermal Integrity & Process Technologies

Chair: Bok Eng Cheah, Intel

<b>Influence of Phosphor Packaging Configurations on the Optical Performance of Chip on Board Phosphor Converted Warm White LEDs</b> .....	329
Peng Hui Yuen, Hwang Hsien Hsiung, Mutharasu Devarajan, Universiti Sains Malaysia	
<b>Thermal Simulation Analysis of High Power LED System using Two-Resistor Compact LED Model</b> .....	334
Zeng Yin Ong, Shamugan Subramani, Mutharasu Devarajan, Universiti Sains Malaysia	
<b>Heat Transfer in High-Power LED with Thermally Conductive Particles-Filled Epoxy Composite as Thermal Interface Material for System-Level Analysis</b> .....	339
Permal Anithambigai, Subramani Shanmugan, Devarajan Mutharasu, Kamarulazizi Ibrahim, Universiti Sains Malaysia	
<b>Optimization of Thermal Vias for Thermal Resistance in FR-4 PCBs</b> .....	345
Alex Lee Yuen Beng, Gan Sik Hong, Mutharasu Devarajan, Universiti Sains Malaysia	