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Stephen C. Hwang, Ph.D., Sandia National Laboratories

2D/3D X-Ray Inspection: Process Control and Development Tool˙"""""ʳ+(*
Zhen (Jane) Feng, Ph.D., Tho Vu, Michael Xie, *David Geiger, and Murad Kurwa, Flextronics International Inc.; Zohair Mehkri, Santa Clara University; Evstatin Krastev, Ph.D., Nordson DAGE

Fix the Process Not Just the Product˙"""""ʳ+* $
Mary Elmallakh, M.Sc., and Paul Groome, Digitaltest Inc.; Andy Shelton, Pulse Communications, Inc.

COUNTERFEIT ELECTRONICS SYMPOSIUM

Counterfeit Sessions Organized by William Cardoso, Ph.D., Creative Electron

PRC3: New Technologies for the Detection of Counterfeit Components
Chair: Robert Flores, Air Force Supply Chain Risk Management
Co-Chair: Kaye Porter, GDCA, Inc.

International Counterfeit Avoidance Certification by the IEC IECQ˙"""""ʳ+*(
Stanley H. Salot, Jr., ECC Corporation

JetEtch CuPROTECT and Copper IC Inspection˙"""""ʳ+*-
Erik Jordan, Nisene Technology Group

Data Fusion for Augmented Electronic Counterfeit Detection Efficacy˙"""""ʳ++'
Bill Cardoso, Ph.D., Creative Electron; Jose Barnabe, SpaceX

PRC4: Counterfeit Components and Supply Chain Management
Chair: Bill Cardoso, Ph.D., Creative Electron
Co-Chair: Erik Jordan, Nisene Technology Group

In Search of a Workable Counterfeit Risk Mitigation Strategy: Lessons Learned In Review of the Current State of the Electronics Industry as Regards Counterfeit Mitigation Requirements for Suppliers˙"""""ʳ++-
Kevin Sink, TTI, Inc.

Legacy Management: Cross-Industry Sustaining Engineering and Managing Obsolescence Counterfeit Risk˙"""""ʳ+,)
Kaye Porter, GDCA, Inc.

SUBSTRATES

Substrate Sessions Organized by Raiyo Aspandiar, Ph.D., Intel Corporation, Don Banks, St. Jude Medical and Srinivas Chada, Ph.D., Schlumberger

SUB1: PCB Fabrication and Reliability
Chair: Robert Kinyanjui, Ph.D., John Deere Electronic Solutions, Inc.
Co-Chair: Srini Aravamudhan, Intel Corporation

Reliable Plated Through Via Design and Fabrication˙"""""ʳ%$$%
Cheryl Tulkoff, and Craig Hillman, Ph.D., DfR Solutions, Inc.

Investigation of the Root-Cause of Solder Bubbles in a Via˙"""""ʳ%$$-
Wang Yang and Luo Daojun, China CEPREI Laboratory

Impact of FPC Fabrication Process on SMD Reliability˙"""""ʳ%$%
Susie Johansson, John Dzarnoski, Ph.D., and Yangjun Xing, Ph.D., Starkey Hearing Technologies

SUB2: Printed Circuit Board Performance and Reliability
Chair: Don Banks, St. Jude Medical
Co-Chair: Viswam Puligandla, Ph.D., Nokia (Retired)

Electrical Performance Evaluation of High-Frequency Laminates as a Function of Temperature and Humidity ˙"""""˚%$&$
Brian Wright, Agilent Technologies

Lead-Free Laminate DMA and TMA Data to Develop Stress Versus Temperature Relationship for Predicting Plated Hole Reliability ˙"""""˚%$&*
Stephanie Moran and Michael Freda, Oracle; Joseph Smetana, Alcatel-Lucent

Reliability Testing of PWB Plated Through Holes Using Interconnect Stress Testing Thermal Cycling Before and After Pb-Free Reflow Preconditioning ˙"""""˚%$' &
Bill Birch, PWB Interconnect Solutions, Inc.

SUB3: Investigation of Reliability for Alternate Surface Finishes
Chair: Lenora Toscano, MacDermid, Inc.
Co-Chair: Barry Hindin, Ph.D., P.E., Battelle Laboratories

Is a High Phosphorus Content in the Nickel Layer a Root Cause for "Black Pad" on ENIG Finishes? ˙"""""˚%$(*
Mustafa Oezkoek, Ph.D., P.E., Joe McGurran and Kenneth Lee, Ph.D., Atotech

Characteristics of EPIG Deposits for Fine Line Applications ˙"""""˚%$) &
Katsuhisa Tanabe, Masayuki Kiso, Kota Kitajima, Tatsushi Someya, *Don Gudeczaukas and George Milad, Uyemura International Corporation

Manufacturability Assessment of Next Generation PCB Surface Finishes ˙"""""˚%$) ,
Sue Teng, Jennifer Oliver, and Scott Priore, Cisco Systems, Inc.

SUB 4: Substrate Technologies for Advanced Electronics
Chair: Laura Turbini, Ph.D., International Reliability Consultant
Co-Chair: Patrick Ryan, Indium Corporation

Advanced Organic Substrate Technologies to Enable Extreme Electronics Miniaturization ˙"""""˚%$* (
Susan Bagen, P.E., Dave Alcoe, Kim Blackwell, Frank Egitto, Steven Rosser, Rabindra Das, and Glen Thomas, Endicott Interconnect Technologies, Inc.

Warpage Mitigation Processes in the Assembly of Large Body Size Mixed Pitch BGA Coreless Packages for Use in High Speed Network Applications ˙"""""˚%$+'
John Savic and Weidong Xie, Cisco Systems; Nokibul Islam, Park Gun Oh, Raj Pendse, and KyungOe Kim, STATS ChipPAC Ltd.

Ultra Flat and Almost No Profile ED-Copper Foils for High Speed Digital PCBs and Chip Scale Packaging ˙"""""˚%$, &
Raymond Gales, Circuit Foil Luxembourg

ENVIRONMENT

ENV1: Sustainability and Environmental Regulations
Chair: Julie Silk, Agilent Technologies, Inc.
Co-Chair: Cheryl Tulkoff, DfR Solutions

European Union RoHS Recast — Implication for Exemption and Substance Review˙"""""r&&*
Adam Wheeler, Jackie Adams, *Marie Cole, Curtis Grosskopf, Jeff Lagler, Sophia Lau, Dale Wilhite, and Kurt Van der Herten, IBM Corporation

Improving Electronics Sustainability With a Novel Reusable, Unzippable, Sustainable Electronics (ReUSE) Interconnect System˙"""""r&' +
*Christopher Hunt, Ph.D. and Martin Wickham, National Physical Laboratory; Robin Pittson, Gwent Electronic Materials; John Lewison, In2tec Ltd.

SPOTLIGHT SESSIONS

Spotlight 1: Polymeric Reinforcement of BGAs
Chair: Raiyo Aspandiar, Ph.D., Intel Corporation
Co-Chair: Ray Prasad, Ray Prasad Consultancy

Solder Joint Encapsulate Adhesive-PoP TMV High Reliability and Low Cost Assembly Solution˙"""""r- ' '
Mary Liu, Ph.D.and Wusheng Yin, Ph.D, YINCAE Advanced Materials, LLC

Underfill Encapsulates and Edgebond Adhesives for Enhancing of Board Level Reliability˙"""""r- ' -
Simon Chang, Edward Ibe and Karl Loh, Zymet, Inc.

Factors Impacting Solder Extrusion in Reworkable Underfills˙"""""r- ((
Neil Poole, Ph.D., Henkel Electronic Materials, LLC

Spotlight 3: Two PCB Reliability Impairment Mechanisms
Chair: Raiyo Aspandiar, Ph.D., Intel Corporation
Co-Chair: Ray Prasad, Ray Prasad Consultancy Services

A Technology to Reduce Pad Cratering Defects and the Impact on Product Cost˙"""""r-) $
Chet Palesko and Amy Palesko, SavanSys Solutions LLC; Chris Hunrath and Ken Parent, Integral Technology, Inc.

Spotlight 4: Process and Yield Improvement in SMT
Chair: Matt Seal, Tektronix
Co-Chair: Chrys Shea, Shea Engineering Services

SMT Assembly Challenges and Proven Solutions for Increasing Yields˙"""""r-))
Robert Dervaes, FCT Assembly, Inc.

Print Performance Studies Comparing Electroform and Laser-Cut Stencils˙"""""r- * %
Rachel Miller-Short and William E. Coleman, Ph.D., Photo Stencil; Joseph Perault, PARMI

Enclosed Media Printing as an Alternative to Metal Blades˙"""""r- +)
Michael L. Martel, Speedline Technologies, Inc.

Spotlight 5: Test Engineering Strategies and Systems for Test of PCBAs in Manufacturing
Chair: Riki Brown, LeeMAH Electronics
Co-Chair: Pat Scott, STI Electronics, Inc.

New Directions in Electrical Test Scalability and Automation˙"""r- +-
Alan Albee and Bobby Griffis, Teradyne, Inc.

State-of-the-Art Test Techniques˙"""r- , *
Vaughan Carlson, Acculogic Inc.

Spotlight 6: Increasing Product Reliability with Better ESD, SPI, SIR Understanding
Chair: Peter Biocca, P.E., Kester ITW
Co-Chair: Ray Chartrand, CharTrain Consulting

ESD Concept-Person, Workplace, Machinery, Transportation˙"""r- - $
Hartmut Berndt, B.E.STAT European ESD Competence Centre

New Requirements for SIR-Measurement˙"""r- - *
Jörg Trodler, Heraeus Materials Technology GmbH & Co.KG; Mathias Nowottnick, University of Rostock

ALTERNATE PAPERS

A Multi-level Finite Element Study to Analyze the Chip-Package-Interaction for Cu/Low-k Interconnects˙"""r% $
Hardik Parekh, Fahad Mirza, Samip Shah, and Dereje Agonafer, University of Texas at Arlington

Penetration Into an International Market: The Aspects of Sales Channels Management˙"""r% +
Moshe Shavit, D.B.A. and Kewal K. Verma, Ph.D., University of Phoenix Online