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Session A1L-A: Analog Circuits I

Chair: Ming Gu, *iWatt Inc.*
Co-Chair: Shantanu Chakrabartty, *Michigan State University*
Time: August 5, 2013, 10:10 - 11:50
Location: Barbie Tootle

[Abstract] Novel CMOS wide-bandwidth 1st- and 2nd-order current-mode allpass filters are proposed in this paper. The 1st- order filter consists of only one transistor, two resistors and one grounded inductor. An addition of one capacitor converts the 1st- order filter into a 2nd-order filter. A 1st-order allpass filter with delay of approximately 33 ps and pole-zero location of 10GHz is designed to confirm the circuit operation. The location of the pole-zero pair is confirmed with a current-mode quadrature oscillator based on the proposed allpass filter. A 2nd-order filter with maximum achievable delay-bandwidth-product is designed to achieve a group delay of approximate 60 ps across a 10GHz bandwidth.

[Abstract] A voltage regulator architecture implemented with floating-gate transistors is presented. The proposed approach substitutes the traditional bandgap voltage reference circuit and resistive feedback with analog memories. As an additional feature, charge modification of these analog memories allow for output voltage modification and circuit performance improvement after fabrication. Prototypes fabricated in 0.5µm CMOS process (Vthn=0.7V; Vthp=-0.9V) operate with 1µA of quiescent current and minimum supply of 1.8V. Experimental results show output voltage programmability from 0.6V to 1.4V, maximum load of 0.50mA, line regulation of 13mV/V, load regulation of 80mV/mA, and a maximum temperature coefficient of 58.2ppm/°C.

[Abstract] A new technique to decrease the transient recovery time in a very low-quiescent current low-dropout (LDO) voltage regulator is introduced. The new Transient Recovery Time Enhancement (TRTE) block comprises a voltage-to-current converter, current comparator and an NMOS output transistor. The proposed LDO using the TRTE block was fabricated in a 0.5-um 2P3M CMOS process. The circuit operates at a total quiescent current of 5.3 uA with a maximum load current of 50 mA while supplying a regulated output voltage of 1.5 V to a 100 pF load. Experimental results indicate a drop-out voltage of 123 mV with an average recovery time of 5.22 us under maximum load current changes.

Session A1L-B: Low Power Digital Circuit Design Techniques

Chair: Abhilash Goyal, *Oracle*
Time: August 5, 2013, 10:10 - 11:50
Location: Hayes Cape

[Abstract] This paper proposes a single-phase partially-adiabatic logic family and compares its energy characteristics with other adiabatic families and CMOS by simulating a full-adder and an 8-bit carry-lookahead adder. Simulation results show that the full-adder using the proposed family uses up to 79% less energy compared to its CMOS implementation and up to 67% less than other adiabatic families. The 8-bit carry-lookahead adder performs at least as well as the next best adiabatic implementation while using fewer clock phases.

[Abstract] Sleep Convention Logic (SCL) is a self-timed pipeline style that offers inherent power-gating, resulting in ultra-low static power consumption. After each pipeline stage has processed new data, control logic asserts a sleep signal causing the entire pipeline stage to be power-gated until the next data arrives. Due to the aggregate sleep capacitance for each pipeline stage, there is an energy overhead for waking and sleeping the pipeline stages. In this paper, an alternative is presented in which only a portion of each pipeline stage is put to sleep. This reduces the aggregate sleep capacitance for each pipeline stage, resulting in reduced dynamic energy consumption.

[Abstract] Universal Asynchronous Receiver Transmitter (UART) implements serial communication between peripherals and remote embedded systems.The UART protocol is defined based on fixed frequencies with a sampling method to achieve robustness under reasonable frequency variations between systems. Such design specifications are natural for clocked domains. This work investigates whether this simple clocked hardware protocol can be advantageously implemented using asynchronous design techniques. A full duplex clocked and asynchronous UART are implemented and compared. The asynchronous design results in average power of about one-fourth that of the clocked design under standard operating modes.

[Abstract] A new power efficient asynchronous circuit design is presented in this paper. By using new input channel restoring circuits and function block partitioning technique to restore only asserted input channels, the transistor area used in each asynchronous logic function unit and thus the load capacitance can be effectively minimized. As a result, the circuit power consumption can be reduced. Our simulation results show that the new asynchronous circuit consumes at least 26% less power. Thus, by applying the new asynchronous circuit design technique, low power consumption and area usage can be achieved.

[Abstract] Null convention logic units are the most important logic unit in asynchronous circuits. This paper propose a new design of Null Convention Logic(NCL) design method based on the differential cascode voltage-switch logic (DCVSL). Comparisons are analyzed on delay and power consumption between the conventional NCL circuits design methods and our proposed NCL circuit deisgn method. After each single NCL gate designs have been simulated and compared, the overall performance of the proposed NCL circuits design technique is compared with the previous designs with a test case of the 4X4 multiplier implementation in 110nm CMOS technology node. The comparison of NCL basic gates shows that the proposed design approach achieves more than 20% power savings and more than 30% delay improvement as well as transistor count reduction.These performance and power saving are also verified in 4X4 multiplier design case.

Session A1L-D: Design and Analysis for Power Systems and Power Electronics

Chair: Hoi Lee, *University of Texas, Dallas*
Co-Chair: Ayman Fayed, *Iowa State University*
Time: August 5, 2013, 10:10 - 11:50
Location: Cartoon Room II

[Abstract] This paper proposes a resonant converter with the class-E_M inverter along with its design procedure. Because the class-E_M inverter is applied to the inverter part of the resonant dc/dc converter, the proposed converter achieves high power conversion efficiency at high frequencies with low cost. By using the numerical design procedure, the accurate component values for achieving multiple constraint conditions without any analyses. In the laboratory measurements, the proposed converter achieved 88.5% power conversion efficiency with 7.5 W output power at 1 MHz operating frequency.

[Abstract] Pulse-width modulated (PWM) DC-DC buck converters can play a critical role in high-efficiency power management systems when operated as dynamic power supplies or amplitude modulators. However, no analysis or design methodology currently exists for a buck converter used as variable-output supply in continuous conduction mode (CCM). This paper describes a key difference in analysis and design for this application, namely the method for determining the optimum inductance value. New inductor design equations, different from those derived for fixed-output CCM buck converters in the existing literature, are presented and verified through simulation of an example design.

Session A1L-E: Design and Analysis of Linear and Non-Linear Systems

Chair: Samuel Palermo, *Texas A&M University*
Time: August 5, 2013, 10:10 - 11:50
Location: Suzanne M. Scharer

[Abstract] Model order reduction (MOR) is an approximation approach where a high order complex system is modeled by a low order parametric system. Power system transients, RLC interconnects in deep submicron technology, and large scale dynamical systems are just a few examples of MOR practical applications. In this paper, the focus is on approximating the impulse response of high order RLC-like systems which resemble most practical applications. The recent progress in compressed sensing field leading to the L1-minimization Basis Pursuit Denoising (BPDN) algorithm for sparse coding has motivated the proposed approach. In this approach an overcomplete dictionary of damped sinusoids is constructed and the sparse coding paradigm is used to find the sparsest solution to the given impulse response. Two other modifications of the basic dictionary with added random atoms are used. A particle swarm optimization with constraints algorithm is employed to refine the sparse coding model, and finally, the best model is chosen adaptively. A system of order 24 is used with 200 realizations, and reduced models of orders 4, 6 and 8 are tested for different dictionary sizes.

[Abstract] This paper introduces a Biquadratic approximation of the fractional-order Laplacian operator, s^α; 0<α≤1. Initially, a single Biquadratic transfer function is designed to approximate the fractional-order derivative over a narrowband spectrum that enjoys an exact gain and phase frequency response. A modular structure is then formed by cascading several Biquadratic transfer functions centered at different corner frequencies to widen the frequency band. The effectiveness and the simplicity of the proposed method are demonstrated against several approximation methods via numerical simulations

Session A1L-F: Emerging Technologues

Chair: Khaled Salama, *KAUST*
Time: August 5, 2013, 10:10 - 11:50
Location: Rosa M. Ailabouni

[Abstract] Vanadium dioxide (VO2) thin films have an insulator to metal transition above a critical temp of 68ºC. In this study, VO2 thin films were deposited on a sapphire substrate for thermally controllable RF/microwave devices. Presented are two thermally controlled varistor designs; a microwave switch and a resonant structure. VO2 devices showed ~2 kΩ at room temp and 2Ω at 70ºC. Switches using a VO2 shunt varistor showed good isolation (>20 dB) and low insertion loss (<1 dB) up to 20 GHz.

[Abstract] This paper presents the concept of a new field effect transistor (FET) based on ferroelectric insulator. The proposed design is named Silicon-on-Ferroelectric Insulator (SOF) FET. The design combines the concepts of negative capacitance in ferroelectric material and silicon-on-insulator (SOI) device. The design proposes that by burring a layer ferroelectric insulator inside bulk silicon substrate an effective negative capacitance (NC) can be achieved. The NC effect can provide internal signal boosting. It is demonstrated that by carefully selecting thickness of the ferroelectric film inside the device the subthreshold swing and the threshold voltage can be lowered. Lower subthreshold swing is a prime requirement for ultra-low-power design.

[Abstract] 3T1D-DRAM cells will still be operative with 7nm FinFETs but their performance is significantly degraded when factoring in variability. In order to improve the cell robustness against device process variation and high environment temperatures, we propose a Dual-VT strategy. Our results show a larger retention time, significant cell spread reduction and reliable behavior up to 100ºC.

[Abstract] We report an experimental study to understand the reduction in the forming voltage with slow electro-forming of HfO2 based Resistive Random Access Memory (ReRAM) devices. Using a combination of capacitance-voltage and current-voltage measurements, we captured the change in capacitance due to dielectric polarization as a function of voltage sweep rates. The dielectric polarization was attributed to the charge trapping or internal redistribution of charged centers under electric field. The dielectric polarization was significantly higher when voltage-sweep rate was slow which causes electro-forming of the dielectric at lower forming voltages.

Session A2L-A: Analog Circuits II

Chair: Ming Gu, *iWatt Inc.*
Co-Chair: Shantanu Chakrabartty, *Michigan State University*
Time: August 5, 2013, 13:10 - 14:50
Location: Barbie Tootle

[Abstract] A CMOS process-insensitive voltage reference generator, which is based on the weighted sum of thermal voltage and difference of threshold voltages, is presented. The voltage reference circuit uses high VTH and regular VTH transistors and produces reference level of 422mV. The proposed technique is analyzed theoretically and its results are compared with other methods. The circuit is designed and simulated in standard 180nm mixed mode CMOS technology for low-cost low-power applications. The circuit operates at minimum supply voltage of 1V with maximum drawn current of 577nA only. A temperature coefficient of 36ppm/°C is achieved with line sensitivity of 0.01%/V. The proposed reference generator exhibits PSRR of -60.34 dB and -37.09 dB at 100Hz and 1MHz, respectively.

[Abstract] Analysis and design of nano-watt bandgap references (BGR) in nano-meter (nm) CMOS are presented. Three different BGR topologies are studied and design trade-offs are discussed. Based on the analysis results, a BGR is fabricated in a TSMC 90 nm CMOS process. A special feature is that it can generate proportional to absolute temperature and complementary to absolute temperature current individually which enables more possibility of system co-design. Measurements show temperature coefficient and line sensitivity without trimming are 47.1 ppm/° C and 0.8 %/V respectively. The power consumption of the BGR core with a 1.2 V supply is 315 nW at room temperature. The core area is 0.026 mm².

[Abstract] A low-temperature coefficient, curvature-compensated CMOS bandgap voltage reference (BGR) is presented. The design was implemented in standard 0.18u m CMOS process with 1.8V power supply. The compensation is achieved generating the negative temperature coefficient (TC) voltage with a quadratic temperature dependent current biasing a bipolar transistor. In addition, the design has a 4-bit trimming circuit to compensate for process variations. The output voltage is 1.225V and shows a TC lower than 2ppm/ °C over a temperature range of 160° C (-20° C to 140° C). The bandgap reference consumes 620 µW and its total layout area is 217x147 µ m².

[Abstract] A bandgap reference source with a temperature coefficient adjustment block was proposed. The topology employs current summation and the circuit was designed through a metaheuristic algorithm in a 0.35-um CMOS technology. Monte Carlo simulations show that the designed circuit has an average temperature coefficient of 27 ppm/0C, average line regulation of 428 ppm/V, and average current consumption of 3.1 uA in a 1 V power supply. The 3-bit temperature adjustment block allowed a maximum temperature coefficient of 26.6 ppm/0C for 90% of the circuits without interfering in the reference voltage output or the line regulation.

Session A2L-B: Low Power VLSI Design Methodology

Chair: Genevieve Sapijaszko, *Devry University*
Time: August 5, 2013, 13:10 - 14:50
Location: Hayes Cape

[Abstract] A modified IC interface based on M×N-ary variable width period modulation is proposed to reduce the complexity of circuit design, and to improve the data transfer rate of a bandwidth-limited system. A demonstration system is built by using two Field Programmable Gate Arrays to simulate the transceiver functions in a RS232 bus, and to verify the feasibility and validity of the interface proposed. Theoretical analysis and experimental results indicates that, the interface proposed can be used not only to reduce the bandwidth and the switching frequency requirements, thereby reducing the design complexity of a high-speed system, but also to increase the data transfer rate of a bandwidth-limited system. Experimental results indicate that a data transfer rate of more than 1.7 Mbps can be achieved using the interface proposed in a RS232 serial bus without any other change in hardware circuit.

[Abstract] Optimized task scheduling with reduced energy consumption is ever demanding in the era of multicores. Power-aware scheduling does not guarantee thermal safety of systems components. Temperature plays an important role in the effective functioning of embedded systems. Therefore, temperature-aware task scheduling is a necessity to reduce the hotspots in such systems and to ensure overall thermal safety. In this paper, we propose a genetic algorithm based solution to task scheduling of different applications on a multi-core system with power and thermal safety. Results on different benchmarks show the effectiveness of our techniques.

[Abstract] This paper proposes two heuristic-based approaches for assessing the reliability of combinational logic in digital circuits. Both approaches take into account reconvergent signals but limited to a first-order-only analysis. Our results show that both approaches lead to more accurate results since the average as well as the maximum estimation error is smaller for the studied circuits.

[Abstract] In this paper, an embedded hardware and software system design and implementation for QR Decomposition Recursive Least Square (QRD-RLS) algorithm using Givens Rotation are presented. Furthermore, hardware and software design optimization are introduced to the Givens Rotation-based method. The computation performance is compared for hardware implementation running on Xilinx Virtex-5 FPGA, and software design running on two different processors (Intel i7 processor and ARM embedded processor) for solving least square problems. The challenges for hardware optimization and software algorithm are also presented.

[Abstract] In this paper, an ultra-low voltage cache with improved variation-tolerance is proposed. Variable strength error control codes are employed to enable the cache to work reliably under ultra-low voltage. An adaptive mechanism is adopted to make the switching between these ECCs fast and stable, which makes the cache more resilient to variations. Our proposed method shows a 10x improvement on residual error rates compared to adaptive ECC method while retaining its lower power feature. Our method provides similar reliability under voltage variation as VS_ECC while our storage overhead is less.

Session A2L-D: Power Management and Energy Harvesting

Chair: Ayman Fayed, *Iowa State University*
Co-Chair: Hoi Lee, *University of Texas, Dallas*
Time: August 5, 2013, 13:10 - 14:50
Location: Cartoon Room II

[Abstract] This paper presents a synchronous hysteretic current controlled (SHCC) buck-type LED driver in order to achieve high power efficiency and high accuracy of the LED current simultaneously. A low-power dynamic level shifter is developed to enable the use of high-voltage power pMOS as the high-side power switch instead of traditional power diodes for significant conduction power loss reduction. The simultaneous peak and valley current sensing scheme is also created in the proposed driver to eliminate the use of any sensing resistor in the power stage for further power efficiency enhancement. Implemented in a high-voltage (HV) 0.35-um CMOS, the proposed driver can deliver an average LED current of 1A. When the input voltage changes from 15V to 50V and the no. of series-connected LEDs varies from 1 to 12, the proposed driver can achieve the power efficiency of >89% and the average LED current error of <1.2%. The proposed SHCC LED driver achieves significant improvements in power efficiency and current accuracy over traditional peak- and hysteretic-current-controlled counterparts.

[Abstract] This paper presents an RF-DC rectifier for radio frequency energy harvesting applications. The proposed passive multi-stage RF-DC rectifier uses standard PMOS transistors to allow individual bulk biasing without the requirement of deep nwell technology. The RF-DC conversion circuit is based on passive threshold self-compensated topology. A design strategy to enhance the input voltage range and to optimize the power conversion efficiency is presented. Designed and simulated in IBM 130-nm CMOS technology, the proposed 915-MHz rectifier shows improved output voltage and power conversion efficiency compared to recent works. When driving a 1-MΩ load, the RF-DC power conversion unit is able to supply 1-V output with an input power of -22 dBm (6.3 μW) and obtains an efficiency of 11.4% at -16.1 dBm (24.5 μW) while supplying 2-V to the output.

[Abstract] This paper presents a regenerative electrostatic energy harvester based on a mechanically-variable capacitor and with no startup battery. We developed a simple model and demonstrated the main design tradeoffs through simulations. The proposed circuit has an improved output power range and can be used to extract from ambient motion the energy needed by small, low-power systems.

[Abstract] in this paper, an external capacitor-less low drop-out (ldo) voltage regulator with superior power supply rejection (psr) and small transient ripple is described. the proposed ldo has the advantages of wide-band psr and fast transient response while consuming only 18µa of quiescent current. simulation results show that the ldo designed in a mainstream 0.18µm cmos technology presents a psr better than -55db up to 1mhz when loaded by a 100pf capacitor. the peak-to-peak undershoots and overshoots are less than 75mv when load current pulses from 0 to 50ma with 1µs rise/fall times. load regulation is around 30mv/ma and output voltage deflection is under 75mv when sweeping the load current in the range 0-50ma.

Session A2L-E: Oscillators and Chaotic Systems

Chair: Samuel Palermo, *Texas A&M University*
Co-Chair: Warsame Ali, *Prairie View A&M University*
Time: August 5, 2013, 13:10 - 14:50
Location: Suzanne M. Scharer

[Abstract] The paper considers the push-pull RC-oscillator/multivibrator. In the sinusoidal regime the circuit develops two counter-phase oscillations located at different DC levels. The DC level of the first oscillation is close to the power supply level, the DC level of the second oscillation is close to the ground. The transition from sinusoidal oscillations to the relaxation ones is achieved by changing the value of the capacitor present in the circuit, so that for small values of this capacitor the oscillations are sinusoidal; for large values the circuit develops relaxation oscillations. This transition is similar to that which exists in source-coupled oscillators/multivibrators. Indeed, the proposed oscillator may be considered as a version of source-coupled multivibrator using complementary gain stages.

[Abstract] The paper considers transition from sinusoidal to relaxation oscillations in the RLC-oscillator the frequency of which is tuned by the resonator capacitance. The active element of this oscillator is a transconductance amplifier with limited output current. When the tuning capacitor is large the oscillations are nearly sinusoidal. Diminishing the tuning capacitor value one moves smoothly from sinusoidal to relaxation oscillations, and when this capacitor is reduced to zero value the oscillator becomes an RL-(magnetic) multivibrator. The transition is illustrated using two root loci; the first is called the placement root-locus, and it describes the location of characteristic equation roots when the tuning capacitor changes but the oscillations have not started yet. The second root locus is called the dynamical root locus, and it represents the periodic movement of the root locations within one oscillation period, and the oscillator is in steady-state oscillations. The oscillator was realized using a bipolar transconductance amplifier and then tested, and smooth transition from sinusoidal to relaxation oscillation was confirmed.

[Abstract] We use VHDL-AMS in modeling of oscillatory systems with mixed mode oscillations. Both the VHDL-AMS behavioral and structural models of a specific generator with mixed-mode oscillations are considered. The generator has interesting properties with MMOs following the Farey arithmetics of integer numbers. A special circuit of simulated inductor is used in the analysis. The VHDL-AMS codes and simulation results are included.

[Abstract] The Gardner's stability theory is vital for linear modeling and empirical design of the charge-pump phase locked loop (CP-PLL). This criterion is general to identify the stability boundary in the steady state. In some applications a voltage switched charge-pump (VSCP) is implied, which offers design simplicity and low cost. The VSCP architecture delivers an unequal amount of pump currents to the loop filter (LF), which introduces the curious non-linearity in the behavior. In this paper Gardner's stability boundary is investigated by making iterative transient simulation using the event driven model in the locked state.

[Abstract] Although discrete-time chaotic-map TRNGs, in principle, are capable of generating unbiased and uncorrelated random bits, implementation variations deteriorate the quality of the output sequence as a result of variation of the chaotic map parameters (which result in a non-ideal map). In this paper, we introduce an analytical technique to investigate the impact of process variations on the randomness of the output sequence generated using tent map-based discrete-time chaotic map truly random number generators (TRNGs). We validate our results against the probability density function (pdf) estimated using extensive Monte-Carlo simulations applied to the nonideal map characteristics. The simulation results suggest that the estimation of pdf using our simplified theoretical method is in good agreement with that of the Monte-Carlo simulations. Finally, the quality of the random bits have also been evaluated using the entropy measure.

Session A2L-F: Bioengineering Systems

Chair: Khaled Salama, *KAUST*
Time: August 5, 2013, 13:10 - 14:50
Location: Rosa M. Ailabouni

[Abstract] In this paper, we design a low power, low noise transimpedance amplifier for ultra-low biosignal amplification. The proposed transimpedance amplifier is implemented in a standard 6 metals, 1 poly, and 0.18um CMOS process. The amplifier is capable of producing 215MOhm transimpedance gain, 0.615MHz bandwidth; 910fA/sqrt(Hz) input referred noise at 100Hz while consuming only 139uW dc power.

[Abstract] Sapphire has better biocompatibility than silicon, higher mechanical resistance, it is transparent, and its lattice matches very well to Si and GaAs. Those unique characteristics enables Silicon-on Sapphire (SoS) technology as a potential solution for implementation of implantable electronic devices, such as retinal prostheses. However, some issues are yet to be solved, such as high cost, and voltage supply limitations. This paper presents circuit topologies and simulated results from a neural stimulator rated for 7.8V supply using standard low-voltage transistors in Silanna Silicon-on-Sapphire 0.5um/FC process.

[Abstract] A CMOS IS front-end which utilizes a time-to-digital converter (TDC) and a peak detector circuit (PDC) for rapid measurement of both impedance phase and magnitude, respectively, was presented. This fast IS front-end can enable cytometry systems capable of fast flow rates monitoring and improve scan rate for massive sensor array systems

[Abstract] This paper presents a high input impedance instrumentation amplifier with low-noise low-power operation. JFET input-pair is employed instead of CMOS to significantly reduce the flicker noise. This amplifier features high input impedance (15.3 Gohms||1.39 pF) by using current feedback technique and JFET input. This amplifier has a mid-band gain of 39.9 dB, and draws 3.65 uA from a 2.8-V supply and exhibits an input-referred noise of 3.81 uVrms integrated from 10 mHz to 100 kHz, corresponding to a noise efficiency factor (NEF) of 3.23.

Session A3P-G: Analog and Mixed-Signal Circuits I

Chair: Annajirao Garimella, *Intel Inc.*
Time: August 5, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] This paper investigates mixed-signal design for double-gate (DG) FinFET technology using a current-starved voltage controlled oscillator (VCO) as a case study. Design issues of the DG FinFET-based VCO is presented in a comparative perspective with a classical CMOS VCO. The DG FinFET VCO is analyzed for the figures-of-merit like center frequency, frequency-voltage (f-v) characteristics. Statistical process variation analysis is presented to study the variability in DG FinFET VCO. Models are investigated for the f-v characteristics and width quantization-aware modeling has been presented for the FinFET-based VCO. The models can be used for fast design optimization. To the best of the authors' knowledge, this is the first paper that examines DG FinFET technology for circuit-level mixed signal design while presenting a comparative between classical CMOS and DG FinFET technologies.

[Abstract] A new hexagon two-dimensional on-chip eye-opening monitor that outperforms the widely used rectangular two-dimensional eyeopening monitor is introduced and its design constraints are derived. The effectiveness of the proposed eye-opening monitor is evaluated by embedding it in a serial link implemented in an IBM 130 nm 1.2V CMOS technology. Simulation results of the data link demonstrate that the proposed eye-opening monitor outperforms the rectangular eye-opening monitor by providing a tightened control of data jitter at the edge of data eyes and by eliminating unnecessary errors flagged by the rectangular eye-opening monitor.

[Abstract] The paper considers that the source follower is the core of such seemingly unconnected circuits as the wideband amplifier, crystal oscillator and emitter-coupled multivibrator. It is shown that the input impedance of the capacitor loaded follower considered as a function of frequency has a negative real part. This allows a designer to compensate partially or completely the resistive component of the signal source impedance. The compensation results in the oscillating nature of the step-signal transmission. In case of inductive component in the source impedance the circuit may operate as oscillator. The oscillations may be also obtained coupling two source followers.

[Abstract] A low power circuit topology for interfacing differential capacitive microsensors is presented. The topology is remarkably compact and low-power due to the heavy reliance on switches rather than analog blocks. The dynamic range and sensitivity of the circuit can further be adjusted by modifying a single capacitor value. The proposed topology has been designed and fabricated in a standard 0.35µm CMOS technology from AMS. The core circuit dissipates 40µW when biased with ±1.65V supply voltages. Measurement results show that the circuit can achieve 1 V/pF differential sensitivity with a total sensing capacitance of 170 fF.

[Abstract] To date, optically reconfigurable gate arrays (ORGAs) consisting of a holographic memory, a laser array, and an optically reconfigurable gate array VLSI have been developed to realize both fast reconfiguration and numerous reconfiguration contexts. A large number of configuration contexts can be stored on a holographic memory and can dynamically be programmed onto a gate array at a nanosecond-order period. Such high-speed dynamic reconfiguration enables a large virtual gate over a physical gate, for example a 1 Tera gate VLSI. However, in addition to the advantage, the ORGA architecture allows high-speed optical Fourier transformation by adding a programmable Fresnel lens. This paper presents a proposal of a new ORGA architecture to support Fourier Transformation and its demonstration result.

Session A3P-H: Analog and Mixed-Signal Circuits II

Chair: Dong Ha, *Virginia Tech*
Time: August 5, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] This work aims to generalize the analysis of the fractional order filter to work for the low-pass, band-pass and high-pass responses. So, general expression for the maximum and minimum frequency points and the half power frequency points will be driven. In addition, the effect of the transfer function parameters on the filter poles and hence the stability is introduced. Besides, the effect of the fractional orders on the frequency response will be presented. Finally, to verify the numerical analysis and the proposed design procedure, circuit simulation will be used

[Abstract] This paper introduces and analyzes a novel method of printed circuit board (PCB) power distribution network (PDN) improvement. This is achieved by using stacked passive components on an integrated circuit (IC) die to improve circuit performance by providing local power supply decoupling. These stacked passives are orders of magnitude greater than what is available for die integration. The capacitors reduce PDN impedance resulting in lower system noise on the device's power supply rails. As the passive devices are located on top of the die, they are not impacted by packaging parasitics which would lessen the impact of package or board mounted decoupling capacitors.

[Abstract] A CMOS fifth-order Gm-C elliptic lowpass filter based on the voltage-mode multiple loop feedback (MLF) leap-frog (LF) configuration is designed. The filter is implemented using a fully-differential linear operational transconductance amplifier (OTA). PSpice simulations using a standard TSMC 0.18um CMOS process with 1.8V power supply have shown that the cut-off frequency of the proposed filter can be tuned from 28MHz to 44MHz, dynamic range is about 67dB, and power consumption is about 67mW at 30MHz. Moreover, 0.7dB passband ripple and 65dB stopband attenuation are achieved for the designed filter.

[Abstract] A method is proposed to realize high-frequency wavelet transform in analogue filter by employing Gm-C circuits and current-mode leap-frog multiple loop feedback structure in this paper. Also, to enhance the performance, the fully differential Nauta transconductor is utilized as the Gm cell in the design. The Marr wavelet is used as an example, with the design procedure illustrated. Using standard TSMC 0.18um CMOS process, simulation results show that the center frequency of the Marr wavelet filter ranges from 63MHz to 142MHz by tuning supply voltage. The total power consumption is 69mW at 100MHz.

[Abstract] A digital bandgap reference that provides a programmable reference voltage output is presented. It uses the same idea as an analog bandgap circuit except that all the three analog operations namely differencing, scaling and addition are done in the digital domain after converting the operands the analog junction-diode voltages into numbers. Digital signal processing provides both precision and programmability. The computed result is converted back to obtain the analog output voltage. The voltage drop across one of the current-biased diodes is used as reference in performing both the analog to digital and digital to analog conversions. Both of these conversions are done in a short time period to ensure that the reference voltage remains constant. Thus the reference voltage value cancels and becomes immaterial. It also becomes easier to address issues like curvature correction in the digital domain. Simulation results are presented.

Session A3P-J: Analog and Mixed-Signal Circuits III

Chair: Valencia Koomson, *Tufts University*
Time: August 5, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] This paper presents an inverse Chebyshev filter for channel selection in the baseband section of an extravehicular activity (EVA) fully integrated radio receiver. The filter is synthesized from a 4th order doubly-terminated LC ladder prototype using a leap-frog structure in order to minimize the use of active components. The cutoff frequency of the filter is digitally controlled for different channel bandwidths through a binary weighted capacitor bank that allows tuning from 1.1 MHz to 2.28 MHz. The derivation of the filter specifications from the system level parameters of the EVA radio receiver is presented. Also, the impact of the channel selection filter in the overall receiver performance is discussed. The circuit is implemented using the IBM 0.18 µm standard process and post-layout simulations show a pass-band gain of -0.07 dB, an IIP3 of 38 dBm, adjacent channel rejection better than 50 dB and a noise figure of 30.2 dB. The filter operates from a 1.8 V power supply consuming 4.03 mA.

[Abstract] The limited power budgets of sensor networks necessitate in-network pre-processing to reduce communication overhead. The low power consumption of analog signal processing (ASP) is well-suited for this task. However, adoption of ASP is restrained by the longer design time relative to reconfigurable/reprogrammable digital processing. Our solution is to enable ASP reconfiguration through the use of a field-programmable analog array (FPAA), which allows wireless sensor network developers to rapidly prototype and test ASP designs. In this paper, we present an FPAA designed for use in wireless sensor networks, and we describe its incorporation and use within a sensor node.

[Abstract] This paper presents a design technique for generation of GHz ADC sampling clock phases from a low-cost low-frequency clock source. Jitter of order 0.1ps is enabled using a DLL-based frequency multiplication method. Nonidealities of the DLL approach are mitigated through digital background correction. Simulated results in a 180nm CMOS process are presented.

[Abstract] A high energy-efficiency capacitor switching scheme for a successive approximation register (SAR) analog-to-digital converter (ADC) is presented in this paper. The proposed switching technique achieves a zero energy dissipation in the first 2 comparison cycles and a 4X reduction in total capacitance used in the digital-to-analog converter (DAC), i.e., for the same total capacitance, the proposed technique can produce 2 additional bits of resolution than a conventional SAR. The proposed method can achieve 95\% savings in switching energy over a conventional SAR which is the highest reported in literature. The result has been verified through behavioral simulations.

[Abstract] In this paper, we introduce an analog-design assistant tool (ADA), which was used to generate a database of 56,280 three-MOSFET circuit topologies. Having setup ADA to provide analog designers with amplifier topologies, it identified 5,103 three-MOSFET amplifiers based on the selection criteria given to the software. As an illustration of ADA capability of helping with circuit optimization, the transconductances of the transistors of each amplifier are automatically optimized by solving a nonlinear optimization problem that is set to maximize gains of circuits. In addition, ADA provides closed-form expressions of gain, input impedance, output impedance and reverse gain. To demonstrate that ADA can be used to identify and optimize new circuits, a previously unknown three-transistor amplifier with a high DC gain of ~40 dB was randomly chosen and fully designed in a 0.13-µm standard CMOS technology. The simulation results obtained with BSIM models show that the circuit topology provided by ADA is accurate and realizable. Using ADA will enable designers to save hours of time and provide them with range of circuits that are customized for their need.

Session A3P-K: Analog-to-Digital Converters I

Chair: Vishal Saxena, *Boise State University*
Time: August 5, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] Conventional two steps ADC for CMOS image sensor requires full resolution noise performance in the first stage single slope ADC, leading to high power consumption and large chip area. This paper presents a 11-bit two steps single slope/successive approximation register (SAR) ADC scheme for CMOS image sensor applications. The first stage single slope ADC generates a 3-bit data and 1 redundant bit. The redundant bit is combined with the following 8-bit SAR ADC output code using a proposed error correction algorithm. Instead of requiring full resolution noise performance, the first stage single slope circuit of the proposed ADC can tolerate up to 3.125% quantization noise. With the proposed error correction mechanism, the power consumption and chip area of the single slope ADC are significantly reduced. The prototype ADC is fabricated using 0.18 um CMOS technology. The chip area of the proposed ADC is 7 um * 500 um. The measurement results show that the energy efficiency figure-of-merit (FOM) of the proposed ADC core is only 125 pJ/sample under 1.4 V power supply and the chip area efficiency is 84k um^2 cycles/sample.

[Abstract] This paper presents a sensitivity study to ionizing particles, which are caused by cosmic rays, on a particular combinatorial function of a 65 nm technology SAR ADC. A methodology for this study is exposed along with the simulation results. A geometrical visualization of the impacts shows the influence of the impact location effects on the function during operation. An ADC operating cycle analysis is done related to the impacts effects showing combinatorial and memorization errors.

[Abstract] A recently proposed method to reduce clock jitter effects in continuous-time Delta-Sigma modulators is to generate a return-to-zero feedback with a fixed-width pulse for active feedback. In practice, the pulse width is subject to noise effects causing jitter of the pulse width itself. Therefore, jitter of the pulse width, though not the clock, may still degrade the perfor-mance of Delta-Sigma modulators. In this brief, we investigate practical feasibility of the method. It is shown that jitter of the pulse width could be conditionally much smaller than that of the clock, which therefore reduces clock jitter effects. Also, the fixed-width pulse method is more effective compared to other reported methods under the same power supply noise.

[Abstract] This paper presents a 0.13µm SHA-less pipeline ADC with LMS calibration technique. The nonlinearity of the first three stages is calibrated with blind LMS algorithm. Opamps and switches are carefully considered and co-designed with the calibration system. Around 7LSB closed-loop nonlinearity of MDAC is achieved. Simulation shows the SNDR of the proposed ADC at 200MS/s sampling rate is 78dB with 3.13MHz input and 75dB with 83.13MHz input.

Session A3P-L: Analog-to-Digital Converters II

Chair: Vishal Saxena, *Boise State University*
Time: August 5, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] This paper presents a column-parallel continuous-time sigma delta (CTSD) ADC for mega pixel resolution CMOS image sensor (CIS). The sigma delta modulator is implemented with a 2nd order resistor/capacitor-based loop filter. The variable gain amplifier in the traditional column-parallel read-out circuit is merged into the front-end of the CTSD modulator. By programming the input resistance, the amplitude range of the input current can be tuned with 8 scales, which is equivalent to a traditional 2-bit pre-amplification function without consuming extra power and chip area. The test chip prototype is fabricated using 0.18 um CMOS process and the measurement result shows an ADC power consumption lower than 63.5 uW under 1.4 V power supply and 50 MHz clock frequency.

[Abstract] This paper presents a modified offset and noise tolerant technique for SAR ADC. With the coarse comparator adopted in the first (n-m-1) cycles and the fine comparator working in the rest (m+2) cycles, the tolerance capability of this technique is ±2^mLSB. A prototype 10b 100MS/s SAR ADC with this technique is presented under 0.13.m CMOS technology. At 1.2V supply and 100MS/s, the prototype SAR ADC achieves 9.56 bits ENOB and consumes 1.66mW energy, resulting in a FoM of 22fJ/conv.

[Abstract] An ultra-low-voltage switched-capacitor (SC) ΔΣ modulator operating at mere 0.25V supply voltage is presented. To facilitate noise shaping in subthreshold region, a novel two-stage inverter-based OTA with DC gain of 43dB is proposed. Also ultra-low-voltage switches and subthreshold comparator are exploited. The transistor-level simulation results show that with an oversampling ratio (OSR) of 64 and a sampling frequency (fs) of 1.28MHz under a 0.25V supply, the converter achieves 86.5dB SNDR over 10kHz bandwidth while consuming a total power of 33.8µW and yielding a figure of merit (FoM) of 97.8fJ/conversion-step.

[Abstract] Winner-Take-All (WTA) circuit chooses a winner input from a set of input signals. WTA circuits employ transistors that operate in the sub-threshold or weak inversion region. With technology scaling, sub-threshold circuits are prone to mismatch and process variations which degrade the performance of these circuits. This paper presents a novel WTA circuit that employs a CMOS double pair transistor as a translinear element that is more tolerant to mismatch and process variations. Monte Carlo simulations are used to compare the performance of the existing and the proposed topologies to estimate the effects of process and mismatch variations. Results show that the proposed circuit is able to reduce the range of variations by three orders of magnitude compared to original one for similar variations in the transistor parameters. The proposed element also shows better accuracy in replicating the maximum input current compared to the original circuit.

[Abstract] We report on a scheme to eliminate false codes generated due to switching delays among the output bits of an asynchronous parallel successive approximation analog-to-digital converter (SA-ADC) developed by Lin and Liu [1]. False output codes are eliminated by converting the binary outputs to Gray codes. A novel asynchronous parallel gray-to-binary converter is introduced to effectively reduce switching delays from 10.0 - 26.5 ns to 767 - 962 ps, when operating with a 50 kHz triangular input and 2V power supply. Simulated INL and DNL are less than ± 0.4 LSB and ± 0.45 LSB, respectively, at 800 µW of power consumption. Measurement results of the ADC, fabricated in 0.5-µm CMOS technology, show the efficacy of the proposed scheme to remove false codes.

Session A3P-M: Analog Circuit Design and Optimization

Chair: Igor Filanovsky, *University of Alberta*
Time: August 5, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] The methodology of designing of analog circuits, being based on applications of control theory is basis for constructing of optimum or quasi optimal algorithm of optimization. By a major criterion here, allowing to exposing the necessary structure of algorithm, there is a behavior of function of Lyapunov, which was defining for the process of optimization. Characteristics of function of Lyapunov and its derivative had been analyzed for searching of optimum structure of control vector and optimal algorithm. The flow diagram of quasi optimal algorithm was built on basic of generalized methodology. The properties of this algorithm demonstrate a great acceleration of the process in comparing to the traditional approach.

[Abstract] The design of Analog Mixed-Signal Systems-on-Chip (AMS-SoCs) presents difficult challenges given the number of design specifications that must be met. This situation is more aggravating in the presence of process variation effects for nanoscale technologies. Existing statistical techniques heavily rely on Monte-Carlo analysis for design parameters in an effort to mitigate the effects of process variation. Such methods, while accurate are often expensive and require extensive amount of simulations. In this paper we present a geo-statistical based metamodeling technique that can accurately take into account process variation and considerably reduces the amount of time for simulation. An illustration of the proposed technique is shown using a 180nm PLL design. The proposed technique achieves an accuracy of 0.7% and 0.33% for power consumption and locking time, respectively, and improves the run time by about 10 times.

[Abstract] This paper presents a 6th order, continuous time band-pass Sigma Delta Analog to Digital modulator in IBM 0.18 um CMOS technology. In order to decrease chip area we replace traditional RLC circuits, containing low quality factor spiral inductors with high quality factor, active inductor based resonators utilizing negative impedance circuits. We see a reduction in chip area and post processing needs are eliminated. Pad to pad simulation of the extracted layout in Cadence yields an enhanced SNDR of 70 dB and a power consumption of 29 mW. An extra active inductor resonator is included on chip for characterization. Our modulator occupies 0.5 mm2 of chip area without pads.

[Abstract] We present a large-scale Field Programmable Analog Array (FPAA) that enables floating-gate adaptive circuits using Floating-Gate(FG) based switch technology. We present a novel architecture technology that enables switch routing with FG elements for signals resulting from high voltage adapting FG elements. We present careful analysis and characterization of the FG structure, including programming ranges, electron tunneling paths, to show the indirect programming structure involving an nFET device can handle the resulting signals. We present experimental data for the basic adaptive structure and for a compiled AFGA.

[Abstract] This paper analyses the design trade-off of a high-output impedance current mirror structure used as a current-steering DAC in a sigma-delta modulation DAC with dynamic element matching. The aim is to provide a design strategy with transistor sizing guidelines leading to the achievement of high static linearity and high accuracy given specific accuracy, load resistance, and voltage swing requirement. Challenging factors limiting the circuit static linearity are described and shown. A test chip implemented in 180nm CMOS process has been designed and fabricated, with simulated results showing static linearity of a 16-bit DAC has been achieved.

Session A4L-A: Analog Design Techniques I

Chair: Dong Ha, *Virginia Tech*
Time: August 5, 2013, 16:00 - 17:40
Location: Barbie Tootle

[Abstract] Energy conversion efficiency is a key factor to be optimized when designing integrated charge pumps. We developed an analytic model that fully accounts for the effects of the parasitic capacitances intrinsic to on-chip implementations. This is applied to find the best possible efficiency in a given technology and to formulate a method for maximizing the efficiency under specified constraints.

[Abstract] This paper presents a z-domain model for voltage-doubler charge pumps that considers the variations of both input voltage and load current. We show how the model can be used to design an efficient control system for a typical charge pump. The application of the model is demonstrated through the circuit simulation of a regulated charge pump, designed to keep area and energy consumption low.

[Abstract] This work presents a temperature and process insensitive CMOS transistor only reference current generator. In the proposed scheme, the passive resistor used in the CMOS Widlar current source is replaced with a transistor resistor where the gate voltage is controlled so that the output current is insensitive to temperature variation. Furthermore, to maintain the temperature insensitivity under process variations, the transistor resistor gate bias circuits optimized for nominal, strong and weak process corners are built on-chip. The proposed reference current generator is designed using 0.5 µm CMOS SOI technology, where the operation is verified through circuit level simulations under nine different process corners. The 20 µA reference current shows a temperature coefficient of 39 ppm/°C within the temperature range of 25°C ~ 125°C for the nominal process corner.

[Abstract] A systematic design methodology utilizing piecewise curvature correction technique for the purpose of improving the temperature coefficient of bandgap references is presented. It is shown that the temperature dependency of the MOSFET's drain current depends on the transistor's operating region. Using this property, a multi-piecewise compensation technique by controlling the operating region of MOSFETs through their gate-source voltages is proposed. The technique offers several advantages including simplicity, and providing the designers with flexibility to employ a combination of piecewise currents to achieve maximum temperature stability. The technique is used to effectively reduce the temperature coefficient of a first-order BGR circuit.

[Abstract] The characterization of nonidealities in a CP-PLL is a challenge in modeling and simulation. In general the CP-PLL is implemented in a transistor-level simulation platform, including all nonidealities and parasitic effects. Due to the low-frequency and the high-frequency part of the CP-PLL, the simulation at transistor-level is time and computer resource consuming. Because of the triggered nature of the mixed-signal CP-PLL the event-driven model is an efficient modeling technique. In this paper an enhanced event-driven model is investigated, considering typical nonidealities. This model allows an efficient analysis and characterization of the non-ideality-effects. All results are validated by a transistor-level simulation.

Session A4L-B: Imaging and Wireless Sensors

Chair: Igor Filanovsky, *University of Alberta*
Time: August 5, 2013, 16:00 - 17:40
Location: Hayes Cape

[Abstract] This paper presents a review of energy harvesting image sensor designs in CMOS technology. Two CMOS image sensors with on-chip energy harvesting capability are presented. Quantitative comparison of power generation capacity of these two different topologies is provided. Both structures make use of the photoelectric conversion capability of the photodiode pixel array used for capturing the image and reconfigure the array to harvest the solar energy. The first pixel is an N-well type pixel while the second structure an isolated P-well type pixel. Both structures were fabricated and measurement results are presented in this paper.

[Abstract] A novel 96 × 96 30 um pitch mixed-signal readout integrated circuit (ROIC) with a pixel-level tunable bias control is demonstrated. The new ROIC is capable of providing a large bias voltage in both polarities on each individual pixel, independently. Also, an FPGA-based testbench has been developed. The unit cell consists of the CTIA integrator, two analog memories, one address selector, and one reference recover switch, built with 15 transistors and 3 capacitors. The test chip has been fabricated in 2P4M 0.35 um CMOS technology, where the bias voltage range is +/-5V and the output voltage swing is +/-3.9 V.

[Abstract] Analog sensor interfaces are used in wireless sensor nodes to perform sensor conditioning, event detection, and data reduction. The use of reconfigurable interfaces will enable applications developers to customize these sensor interfaces and to reconfigure them in the field. In this paper, we examine the energy cost of reconfiguring analog circuitry and how the requirements of wireless sensor nodes impact the design of reconfigurable analog systems.

[Abstract] With steady miniaturization of neuroprosthetic implants, testing the hermeticity of the device encapsulation requires unprecedented level of sensitivity. To this end, developing new sensors and associated readout circuitry has become an ineluctable part of research in this field. This paper presents the design of a readout scheme that is capable of interfacing with either resistive or capacitive sensors and performs signal processing based on `lock-in' technique to enhance the effective resolution. The design methodology focuses on low noise, high accuracy readout and adaptability to a wide range of baseline values and different sensitivity levels of various types of sensors. The circuit is being fabricated on 0.5μm Silicon-on-Sapphire process and experiment setup is currently being carried out.

[Abstract] We present an implementation of an auditory filter bank that decomposes the signal into 16 parallel bands according to the mel-scale from 150 Hz to 10 kHz. The integration of the proposed filter bank in a microsystem for acoustic source separation poses a stringent constraint on the linearity of the filter and dynamic range. The capacitive attenuation is used to increase the voltage range at the input and output of the filter bank. The simulation results demonstrate the harmonic distortion of the filter of -60 dB and dynamic range of 58 dB. The power consumption of the filter bank implemented in 0.5u m CMOS technology is 36 uW.

Session A4L-C: Special Session: Characterization of Nano Materials and Circuits

Chair: Nayla El-Kork, *KUSTAR*
Time: August 5, 2013, 16:00 - 17:40
Location: Cartoon Room I

[Abstract] The potential energies curves have been calculated for the 17 lowest quartet electronic states in the 2s+1Λ ± representation of the molecule VO via CASSCF. Multireference CI calculations were performed. The harmonic frequency ωe, the internuclear distance re and the electronic energy with respect to the ground state Te have been calculated for 16 electronic states. Ten electronic states have been studied here for the first time. The comparison of the investigated values with the theoretical and experimental results available in the literature shows a very good agreement

[Abstract] " A study of Local Surface Plasmon Resonance (LSPR) behavior of illuminated elliptical gold nanoplots is presented. We use finite element simulations that show the repartition of the electric field on the surface of an excited gold plot, and corresponding optical spectra. Such results are compared and with experiment (near field optical imaging) and previous work.

[Abstract] Near-threshold voltage provides savings in power, but it has a negative impact on delays, noise margin and yield. A removed metallic CNT approach to deal with such CNTs is used. Monte Carlo simulations have shown that with Vdd down to 0.5V, 0.72% of the cells are non-functional after M-CNTs are removed. Power saving is over 5X, while average delay increases by 3.5X as compared to 0.9V. Gated cell power supply technique is applied to eliminate the write failures. At 0.5V, the cell with gated power supply improves write performance and write EDP by 1.5X and 2.9X compared to non-gated cell.

[Abstract] In this research electrochemistry of carbon nanofibers (CNFs) has been investigated as part of a biosensor that is able to detect glucose at various environments. The electrical and chemical characteristics of dry and wet CNF are studied and found to be ohmic between -2 and +2 volts with a frequency range of 13 Hz to 850 kHz. The cyclic voltammetric (CV) results indicated that glucose oxidase GOx assembled on CNF exhibit a surface-confined process where electrode's electrochemical characteristic plays an important role. The tests are performed using a two and three-electrode analyzer, with positive results at glucose concentrations as low as 2 mM.

[Abstract] The unrelenting scaling of CMOS devices has brought their dimensions down to few tens of nanometers. In such sizes, the reliability margins drop ominously and the leakage power dissipation increases significantly. This paper presents a non-conventional transistor-sizing method for improving reliability by increasing the static noise margin, while simultaneously reducing the power consumption. Simulations results have been used to compare the static noise margin, the power consumption, and the performance of classical CMOS gates with the proposed scheme in the 22 nm technology. The results show that modifying the channel lengths of transistors in inverters and other gates can improve the noise margin by nearly 40% over the conventional one, while reducing the power consumption by 47%. The robustness (measured here in terms of noise margin) of the classical and the new gates are also compared when their transistors are subject to threshold voltage variations.

Session A4L-D: Special Session: Power Management and Energy Harvesting

Chair: Paul Furth, *New Mexico State University*
Time: August 5, 2013, 16:00 - 17:40
Location: Cartoon Room II

[Abstract] This paper presents a cross-regulation-free switched-capacitor (SC) DC-DC regulator that is able to simultaneously produce three different regulated output voltages for energy harvesting applications. With capacitor and power switch sharing, the proposed power stage can realize separate 2x, 3x and 4x outputs, while saving 3 flying capacitor and 9 power switches compared with using three independent single-output doubler, tripler and quadrupler. A sub-harmonic fixed on-time control scheme is developed not only to regulate all outputs, but also to improve the light-load regulator power efficiency, minimize the cross-regulation between three outputs, and provide predictable noise spectrum of all regulated outputs. Implemented in a standard 0.35um CMOS process, the proposed regulator can provide three regulated outputs of 2V, 3V and 4V under 1.1V input voltage, and deliver up to 15mA (2V), 12mA (3V), 2mA (4V) local currents. The proposed regulator also achieves a maximum power efficiency of 89.8%.

[Abstract] This paper presents a switched capacitor (SC) DC-DC converter using digital control method based on delta-sigma pulse frequency modulation (PFM) to accomplish a fast transient recovery time when output load changes rapidly. The DC-DC converter utilizes the first-order error feedback delta- sigma algorithm to control the switching frequency of the digitally controlled oscillator (DCO) using thermometer code. The load voltage of the SC DC-DC converter is regulated by the switching frequency of the DCO output based on the error between the load voltage and the reference voltage. The digital control method has two operation modes for fast transient recovery time; course and fine tuning modes to change the DCO's switching frequencies fast and accurately. The proposed converter accomplishes 72% power conversion efficiency, settling time of less than 460ns, and maximum deliverable output power of 230mW. The estimated total power consumption of the control loop is less than 0.82mW at 1.6V operation voltage.

[Abstract] A high-efficiency, high-dimming ratio LED driver, capable of driving two standard white LEDs, is designed using a synchronous boost converter and PWM controller. The LED current is sensed using voltage-mode feedback to maintain a constant load current. The output sense resistor in a conventional LED driver is replaced by the disconnect switch to increase efficiency. Lossless current-mode feedback, in which the inductor current is sensed via the on-resistance of the boost series switch, improves stability. Dimming control logic is implemented with a 10-bit counter and a 10-to-1 MUX, generating 10 dimming ratios ranging from 2:1 at a frequency of 625 kHz to 1024:1 at 610 Hz. The simulated efficiency of the LED driver alone is 86.1% and that of the LED driver with dimming control is 85.4%.

[Abstract] Electrostatic-based power generation is an attractive alternative to piezoelectric and electromagnetic techniques, as it can be integrated in mainstream silicon technologies while providing higher power densities through miniaturization. However, at present, the power output of reported electrostatic micro-generators does not meet the communication and computation requirements of wireless sensor nodes. This paper presents an overview of electrostatic vibration-based energy harvesting. The challenges in designing the MEMS-based energy harvester and the associated control and interface integrated circuits to guide the transfer of charge/energy to a reservoir unit are discussed.

[Abstract] Wireless microsensors add intelligence to otherwise inaccessible locations and large infrastructures, such as tiny crevices in hospitals, factories, and farms. These small devices, however, store little energy, so functionality is low or lifetime is short, or both. Luckily, harnessing ambient energy can replenish these microsystems, and because solar light generates considerably higher power density than motion, temperature, and radiation, photovoltaic (PV) systems are appealing options. Still, chip-sized CMOS PV cells produce only microwatts, and power-conditioning circuits consume some of that, leaving little energy for the sensor system. In view of this constraint, this paper shows that a 0.18-µm CMOS system is 6% more efficient with four stacked 1-mm2 PV cells than with one 4-mm2 cell. However, stacking P+"N Well cells, which is the only stackable PV structure, is 20% less efficient than one cell, so systems that draw power from one N+ or N well in substrate cell are better.

Session A4L-E: Communication and Signal Processing Circuits

Chair: Samuel Palermo, *Texas A&M University*
Time: August 5, 2013, 16:00 - 17:40
Location: Suzanne M. Scharer

[Abstract] This paper presents a 65nm 0.1-1.5GHz dual-mode Class-AB/Class-F CMOS PA for industry-specialized multi-standard applications. The highly efficient Class-AB/Class-F operations are achieved by controlling the bias voltages and the third harmonic component in the output load while maintaining the linearity. The Class-AB operation mode of the proposed PA has an output power above 19.5dBm with less than 1dB variation and a PAE between 25% and 28.6% over 0.1-1.5GHz. In the Class-F mode, the maximum output power of 24.2dBm and the peak PAE of 64% are achieved. Simulation results have demonstrated that the proposed Class-AB/Class-F PA is a good candidate for the dual-mode PA in the highly-integrated multi-standard transmitters.

[Abstract] This work presents a dynamic biasing topology capable of linearizing a Class-C power amplifier (PA). The topology utilizes a closed loop that senses the operating conditions of the “power device” by means of a scaled-down replica. The loop operates on the principle of keeping the conduction angle remarkably constant and thereby ensuring linearity. The work details some of the design considerations that should prove useful to a designer wanting to implement the topology in an RF integrated circuit. Measurement results from a fully functional low-frequency prototype bring merit to the topology.

[Abstract] In this work, a steady-state analysis and a fast optimisation approach based upon it are implemented to analyse the class-E PA. With this approach, the component values and performance of class-E PA with RFC and parallel-circuit load (PCL) are analysed and compared. One fast search approach is developed for various constrained/unconstrained optimisations. The analysis, fast optimisation approach and evaluation as well are implemented in Matlab©. The feasibility, flexibility and fastsimulation are shown by comparing the RFC and PCL for a 1 W class-E PA design. All the results show good match with ADS© harmonic balance.

[Abstract] The linear amplification using nonlinear components (LINC) is one of the most promising techniques that can simultaneously provide high efficiency and high linearity. However, it is sensitive to in-phase/quadrature imbalances in quadrature modulators (QMs), and to gain/phase mismatches between two PA paths. In this paper, we present an iterative calibration technique to compensate for the imbalances and mismatches, based on the observation that when the I/Q imbalances in the QM are ideally calibrated, the PA input signal has constant envelope, which allows the PA to be characterized as a linear gain model. It allows us to estimate the calibration parameters without modeling the nonlinear characteristics of the PAs. An adaptive implementation scheme is given. Simulation results demonstrate that the proposed technique accurately determines the calibration parameters, yielding significant performance improvement of the LINC transmitter.

[Abstract] In this paper, we propose a 2nd order fractional band reject filter (FBRF) transfer function. It is based on the concept of introducing a fractional capacitor (Cα) having impedance, Zα = 1/s^(α)Cα where 0 < α < 1. It is possible to achieve asymmetric slopes and large values of notch magnitude up to −60 dB using this filter. In addition, unlike integer order filter, independent control of slopes above and below the notch frequency can be achieved by simply changing the values of α. The operation of this filter is verified by plotting PSPICE simulation results for three different values of α = 0.1, 0.5, 0.8 and showing its comparison with experimental results.

Session A4L-F: Sensing and Measurement of Biological Signals

Chair: Hoda Abdel-Aty-Zohdy, *Oakland University*
Time: August 5, 2013, 16:00 - 17:40
Location: Rosa M. Ailabouni

[Abstract] A microcontroller-based wireless medical device was designed and developed to measure acceleration during head impacts in contact sports. This device is capable of measuring linear acceleration, time of occurrence, and duration of any form of impact or collision. In order to validate the acceleration values from the device, an experimental set-up was built to mimic head collisions. The focus of this paper is to elaborate the design and various techniques involved in experimental validation of the device.

[Abstract] In detecting disease and existence of certain molecules, a capacitive sensor can be used to detect binding of target molecules on to antibody in the sensor. This paper describes the design of a capacitive sensor which is capable of detecting as small as 10fF change in capacitance. The design is in a 0.18um CMOS process.

[Abstract] This paper presents the development of a Point-of-Care device centered on a three electrode Cu based sensor that uses Anodic Stripping Voltammetry (ASV) for rapid electrochemical measurement of Zn in serum. The sensor is read using a system built from commercially available embedded system parts in conjunction with custom analog circuitry. It is able to produce quantification results in approximately 6 minutes.

Session B1P-G: Digital Systems

Chair: Khaled Salama, *KAUST*
Time: August 6, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] Energy consumption of a vehicle depends on the nature of the road surface, grade and the vehicle parameters. Predictive control strategies that rely on this information can benefit significantly from the knowledge of these parameters. The paper proposes an online estimation strategy to simultaneously estimate the vehicle mass, road frictional coefficient and wind velocity for a Series-Parallel Hybrid vehicle. A P2 hybrid vehicle longitudinal model is developed and is used along with a two stage RLS algorithm to estimate the dynamic parameters. The estimation strategy uses inputs from the vehicle longitudinal accelerometer sensor for determining road grade along with other powertrain signals.

[Abstract] This paper reports cipher-destroying secret-key-emitting hardware Trojan against AES circuits in order to facilitate countermeasures against such Trojans. If an attacker-defined predetermined rule is satisfied in the AES core, the hardware Trojan is triggered and it sends half-encoded data from the encryption module to the decryption module via a Trojan path. As a result, plain text is directly delivered to the output port. Furthermore, if the hardware Trojan-inserted AES core is inputted with a predefined keyword, which is transferred to a controller via the Trojan path, a secret-key is directly outputted. To verify the threat of AES hardware Trojan, we evaluated the FPGA and ASIC implementation results from the Verilog language macro.

[Abstract] Testing reversible circuits is a challenging issue. A commonly used technology related fault model in reversible gate is missing control points of reversible gates. In this paper we address this type of fault in reversible adder/subtractor circuit and present an efficient way to detect and identify the location of the faults. The regular structure of adder/subtractor facilitates the testing of such circuits and we show that only three test vectors are sufficient to test for n-bit adder/subtractor with 100% fault coverage. Moreover, with proper sequence of input test vectors it is possible to find the fault location.

[Abstract] With the tremendous growth in VLSI technology in recent years, in deep submicron regime (DSM), the integration density of the transistors has reached billions causing the scaling of transistors to touch the subatomic dimension where laws of classical physics can not survive. Due to inherent information loss and other factors associated with irreversible computing, reversible circuits are becoming more and more important in terms of computing for present and future days. However, due to several factors, known synthesis approaches of classical Boolean logic like Karnaugh Map and Quinne-McCluskey method cannot be applied directly to synthesize a reversible logic. In this paper, we propose a stochastic procedure to synthesize a reversible circuit. This procedure is based on a modified version of classical Quinne-McCluskey method and is being used under the wrapper of two intelligent stochastic search techniques, Simulated Annealing and Ant Colony Optimization. The experimental results are quite encouraging.

[Abstract] Two new clock gated flip-flops are presented. The designs are based on new clock gating approaches to reduce the consumption of clock signal's switching power. They operate with no redundant clock cycles and have reduced number of transistors to minimize the overhead and to make it suitable for data signals with higher switching activity. The proposed flipflops are used to design 8-bit successive approximation register. This application has been designed up to the layout level with 1 V power supply in 90 nm CMOS technology and has been simulated using Spectre. Simulations with the inclusion of parasitics have shown the effectiveness of the new approaches on power consumption and transistor count.

Session B1P-H: Low Power Design and Test Techniques

Chair: Moataz AbdelWahab, *Nile University*
Time: August 6, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] CAM is a fast lookup hardware table. However, it causes significant power consumption. In this paper we propose a low power match-line architecture, called DML design, in which we combine the charge sharing and segmentation technique to largely reduce the CAM power dissipated in the ML switching activity. Our design uses two MLs to perform the search operation. By reducing the ML swing, our design can minimize the charge loss in the search operation. Based on TSMC 90nm technology, the simulation results show that our's can reduce the search energy consumption of the CAM by 84% compared to the conventional NOR-type CAM design.

[Abstract] In this paper, a design of high performance modulo 2^n+1 squarer is proposed. The primary improvement comes from the algorithm, circuit implementation, and implementation technology. The proposed design shows much better performance in terms of delay, power, and area comparing with existing designs. The design is implemented using carbon nanotube technology to compare the same circuit performance with the conventional CMOS technology. The proposed design shows that the critical path delay and rise time of modulo 2^8+1 squarer on CNT technology is 13.6 times and 9.3 times better than that of CMOS technology with a better PVT variation tolerance.

[Abstract] This paper introduces a new framework to construct fast and efficient pseudo-random (PN) sequence generation for bit scrambling, called a J-delayed and K-dimensional Linear Feedback Shift Register (JKLFSR). In the proposed framework, we generate the state of a J-shifted LFSR using one clock and K-bit multiple outputs of a LFSR each clock cycle for scrambling/descrambling of large coded bits using an output of LFSR. JKLFSR is highly relevant for the scrambling/descrambling process for a high-speed mass data transmission in an LTE-Advanced system, as it has fast computation and supports clock-based processing. In addition, we show that JKLFSR has an efficient performance theoretically in generating PN sequences. H/W simulation results verify the validity of the theory and demonstrate that we reduced the processing time used for generating PN sequences from (J + DL) clocks to (1 + DL/K) clocks as compared with a conventional LFSR, where DL denotes the length of a data stream.

[Abstract] Networks-on-chip has been seen as an interconnect solution for complex system but the performance and the energy dissipation still represent limiting factors for Multi-Processors Systems-on-Chip (MPSoC). The future handheld devices must support multimedia applications for long battery life but this type of application imposes heavy constraints in terms of energy and forces the designers to optimize all parts of the platform to achieve the desirable goals. The objective of this paper is to analyze and assess the energy dissipation for heterogeneous NoC-based MPSoC platform running a video application. It identifies bottlenecks for the entire platform. We showed that the energy dissipation appear to be the most critical factor for memory and caches not for the communication architecture as the common belief. Also, we propose a new modeling and simulation approach regarding the channel width and buffer sizing which have a strong impact on the performance and the overhead of the chip. We showed that there are some hot spots in the system regarding the channel width and buffer size must be optimized to get a better performance.

[Abstract] Advancements in computing technologies coupled with increased complexity of mobile applications lead to increased power consumption in mobile devices. However, battery technology cannot keep up with these trends thus making power management one of the foremost concerns in mobile devices. While system-level approaches to power management exist, the energy impact of applications on individual system components needs to be better understood for energy efficient system design. In this work, we develop a power modeling methodology for mobile devices using performance counters that overcomes the shortcomings of existing models and estimate power consumption of system components for numerous embedded applications. We further compare our power estimates with existing models and demonstrate the uniqueness of our model.

Session B1P-J: VLSI Design and CAD I

Chair: Nader Rafla, *Boise State University*
Co-Chair: Jinyong Chung, *Inha University*
Time: August 6, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] As the number of components in Field-Programmable-Systems-on-Chip (FPSoCs) increase, the interconnect schemes based on Network-on-Chip (NoC) approach are increasingly being used to overcome the deficiencies of the traditional bus- based and point-to-point interconnect schemes. The router is a key component that greatly impacts the performance and cost of an NoC. In this paper we present FLNR, a fast light-weight NoC router for FPGAs. FLNR is compared to other proposed routers based on three metrics: area, frequency and zero load latency. Synthesis results and zero load latency evaluations show that our router is significantly superior to widely referenced, previously proposed routers.

[Abstract] Power supply C4 (flip-chip) bonds are susceptible to failures due to electromigration caused by high on-chip temperatures, large currents and manufacturing variability. A single C4 bond failure can result in catastrophic failures in the power supply network and thus redundant bonds are naively added to the circuit to mitigate the impact of bond failures. We propose a method for improved redundant bond placement using an Integer Linear Program (ILP) that reduces the required number of redundant bonds by 33% while ensuring power supply integrity in the presence of a single-bond failure.

[Abstract] Since analog circuits are usually very sensitive, it is desirable to consider layout-induced parasitic effects early in a design flow. In a proposed layout-aware analog design methodology based on the use of parameterized 45-degree layouts, parasitics can be estimated in the circuit synthesis phase if models of extracted circuits can be generated from these layouts. In order to perform circuit extraction from parameterized 45-degree layouts, algorithms are required for dealing with parameterized 45-degree polygons and relevant constraints. In particular, algorithms for performing Boolean mask operations on parameterized 45-degree polygons are essential in the circuit extraction process. In this paper, an efficient approach is proposed for performing Boolean mask operations on parameterized 45-degree polygons. To the best of our knowledge, this paper is the first in the literature to present an approach for performing these operations.

[Abstract] Cell based self-timed synthesis of recursive carry lookahead adders (RCLA) utilizing generate, propagate and kill functions is described in this paper, and are compared with the recently proposed designs of self-timed section-carry based carry lookahead (SCBCLA) adders. From the simulation results corresponding to a 130nm CMOS process, it is found that with 2-bit CLA, the RCLA adder dissipates 20.2% less power than the SCBCLA adder. With 4-bit CLA, the RCLA adder reports power reduction by 16.5% than the SCBCLA adder. Further, for addition widths ranging from 32 to 64-bits, RCLA adders consume 19% less average power compared to SCBCLA adders.

Session B1P-K: VLSI Design and CAD II

Chair: Jinyong Chung, *Inha University*
Co-Chair: Nader Rafla, *Boise State University*
Time: August 6, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] Power consumption is one of the major issues in System-on-Chip (SoC) design with advanced semiconductor technologies for low power applications such as mobile phones. Recently, banking several 1-bit flip-flops has been proposed as a solution to reduce the power consumption in clock networks. For this purpose, to build an accurate power model for multi-bit flip-flop banks is required. However, it is an excessively time-consuming and sophisticated work due to a high number of pins. Therefore, we first propose a simplified power characterization method to reduce characterization time. Then an efficient power modeling is introduced to create an accurate state-dependent power model for multi-bit flip-flop banks. Experimental results show that the proposed characterization method allows to linearly increase CPU time with 1.3X per bit comparing with exponentially increasing CPU time by the traditional characterization method. In addition, the proposed power modeling provides an average error of 6% compared to SPICE simulation results.

[Abstract] Hardware security in Field Programmable Gate Arrays (FPGAs) which use Physically Unclonable Functions (PUFs) rely on the ability to produce a large number of unique frequencies. This paper explores the frequency uniqueness as it relates to the number of stages used to build a ring oscillator. The experimental results from Xilinx Spartan 2 FPGAs show that the three stage ring oscillators have the highest standard deviation in terms of the frequencies produced. Ring oscillators with five, seven, nine and eleven stages on the other hand have a much smaller standard deviation. Based on these experimental results, it is found that the number of stages in a ring oscillator plays a critical role in determining frequency uniqueness.

[Abstract] In this paper we analyze and compare 8 different SRAM cell topologies that are suitable for low power embedded memory design in terms of power consumption, static noise margin (SNM) and read and write delays. The circuit simulation and analysis were carried out using HSPICE for 45 nm technology node. The SNM of each cell is examined analytically using SLL (Seevinck, List and Lohstroh) method. Throughout the design and analysis VDD is kept at 1.2V. For the determination of Read and Write Margin of SRAM cells, the cell ratio is kept at 3 and the pull up ratio is kept at 2 throughout the design. Our results will enable memory circuit designers to choose the appropriate SRAM cell for the required SNM and power consumption.

[Abstract] The wide use of Field Programmable Gate Arrays (FPGAs) in critical applications including, military and airborne applications require fault free operation of the FPGA. In FPGAs, faults can occur in the memory resources, logic blocks, or the interconnects. In this paper, memory faults including Stuck-at, Transition, Address Decoder, Incorrect Read, Deceptive Read Destructive, and Data Retention Faults are analyzed using an optimized March C- algorithm. In order to evaluate the effectiveness of this algorithm, a novel Built-in Self Test (BIST) technique to test the embedded SRAM memory of the FPGA is proposed. The proposed technique reduces the test time by approximately half as compared to previously published schemes. The FPGA is modeled in VHDL at the equivalent gate level and the simulations results are generated using ModelSim.

Session B1P-L: Advances in Power Systems and Power Electronics

Chair: Ayman Fayed, *Iowa State University*
Co-Chair: Hoi Lee, *University of Texas, Dallas*
Time: August 6, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] Relative stability of the inner-current loop with slope compensation for peak-current mode controlled PWM dc- dc converters operating in CCM is analyzed. Expressions for required compensation slope and control current level to achieve a specified margin of stability are derived. Design procedure and Saber Sketch simulation results for a buck converter with the inner-current loop are presented to validate the theory presented.

[Abstract] The low-dropout voltage regulator (LDO) is more efficient than other regulator topologies; however it suffers from instability, which necessitates an off-chip capacitor to ensure a stable output. This work presents an alternative topology, removing the external capacitor, thus allowing greater system integration. The proposed Current Amplifier Hybrid Compensation (CAHC) scheme implements an active compensation system and maintains both a fast transient response and full range AC stability. The 1.2V LDO voltage regulator was designed and simulated in 0.35um CMOS, and consumed 61uA of quiescent current with a dropout voltage of less than 200mV. Simulations demonstrate that the proposed architecture overcomes the load transient and AC stability issues encountered in other regulators.

[Abstract] This paper describes the implementation of a monitoring system to determine the efficiency of energy production generated by a set of six photovoltaic panels, interconnected grid home in Bogota Colombia. The system is easy to use and enables the visualization of different signals acquired with sensors to measure temperature, solar radiation, voltage and DC current produced by the panel, the AC output of the inverter, the power generated by PV modules network and delivered power

[Abstract] This paper presents an optimal controller in order to achieve trajectory tracking for nonlinear systems and mini- mization of a quadratic cost functional. The synthesized optimal control law comes from solving the Hamilton-Jacobi-Bellman equation for state-dependent coefficient factorized nonlinear sys- tems. An important characteristic of an optimal control scheme is that stability margins are a priori guaranteed and besides the controller synthesis allows to incorporate physical constraints for states and control inputs. The proposed control scheme is used for ensuring an efficient power flow exchange between different sources in a microgrid by using power converters. The signal references to be tracked by the control system are considered to be established by an energy management system in accordance to the amount of energy to be transfered, and taking into account variables such as energy availability from the sources, the weather, the price of electric power, the cost of fuel, among others. The effectiveness of the proposed optimal approach is illustrated via simulations.

[Abstract] In radio-frequency (RF) switched-mode tuned power amplifiers (PA), the RF amplitude at the output of PA is a direct and linear function of the supply voltage provided by voltage regulator module (VRM). This phenomenon has been utilized effectively in order to obtain high efficiency amplitude modulated power amplifiers. The presence of capacitor voltage ripple at the output of VRM adversely affects the modulation signal. Consequently, the signal at the output of PA may also suffer from distortion resulting in reduction in efficiency. In this paper, a two-phase buck converter is considered and the effect of ripple suppression is analyzed. The main advantage of the two-phase converter is that by changing the number of phases and hence, the duty cycle, amplitude modulation can be achieved with significant reduction in ripple and improvement in peak-to-average-power ratio. Further, the functionality of class-E power amplifier is presented in brief and used as a load to the VRM. Simulation results obtained using SABER circuit simulator are also presented and few concluding remarks are provided.

[Abstract] Faraday rotation (FR) is a useful optical technique to investigate magnetic properties of solid and liquid samples. FR refers to magnetically induced birefringence whereby a substance rotates the polarization of a light beam passing through it, in the presence of a magnetic field. While FR experiments commonly employ either a DC or an AC magnetic field, obstacles exist for some samples with these setups. Overcoming some of these difficulties, a pulsed field setup has been designed and tested that allows for investigating magnetic response to short intense fields on the order of 1.5 Tesla and lasting 30 to 50 milliseconds.

Session B1P-M: Power Management and Energy Harvesting Techniques

Chair: Hoi Lee, *University of Texas, Dallas*
Co-Chair: Ayman Fayed, *Iowa State University*
Time: August 6, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] A calibration technique to maximize the power harvest of passive wireless microsystems is proposed. We show that both the impedance and resonant frequency of the transformer matching network are sensitive to process spread and load variation, and can be calibrated by tuning a shunt varactor at the secondary winding of the transformer to maximize power transfer from the antenna to the transformer and power efficiency of the voltage multiplier. An ultra-low power current tuning technique and a maximum peak amplitude detection technique to automatically allocate the optimal tuning capacitance at which maximum power harvest exists. The proposed transformer matching network is designed in IBM CMRF8SF 130 nm 1.2 V CMOS technology and its effectiveness is validated using post-layout simulation.

[Abstract] This paper develops a state-variable approach to modeling wireless power transfer (WPT) networks in order to accommodate nonlinear loads. A four-coil WPT system is presented in a simplified three-coil representation. The state-variable model with nonlinearities suppressed was validated against a linear model. Simulations were then performed using the state-variable model with rectified and filtered dc output applied to resistive and constant-power loads.

[Abstract] A design has been made for a four-coil wireless power transfer network that appears capable of wireless transfer of power at 100kHz over midrange distances (1-2m) with good efficiency. The design is presented as well as the effect of varying the transmitter-to-receiver separation. The design appears feasible, and experimental implementation is expected to follow.

[Abstract] A power conditioning circuit for an electromagnetic energy harvesting device which is designed to harvest energy from the suspension of a freight train is presented in this paper. The electromagnetic transducer, which converts linear vibrations into electricity, is briefly discussed in this paper. After the output features of the transducer are studied, a buck-boost converter is designed to present a constant 10 ohm load to a three-phase full-wave rectifier. This converter charges a 4-cell LiFePO4 battery pack. The working principles and efficiency of the circuit are analyzed and tested for the application purpose.

[Abstract] With today's drastic increase in energy demand, it becomes more and more important to use alternative green technologies. Solar, wind, and hydroelectricity are popular choices, because they are abundant and cause low pollution. One big challenge however is how to manage these new energy resources within the traditional electricity grid. Today's smart home technologies and devices offer a variety of house appliances with embedded sensors. Through Internet websites or ad hoc applications, customers are able to monitor household appliances and receive data from the sensors in real time. However, users are not suggested what measures to take to save energy and money. This paper discusses the design of a new power management system. A new hardware design is developed to implement the proposed management energy solution. The new design consists of a bidirectional DC-DC converter and a battery charger/discharger circuit. By adopting this approach for smart grid systems, we provide a management solution to optimized energy distribution and usage.

Session B2L-A: Analog Design Techniques II

Chair: Valencia Koomson, *Tufts University*
Time: August 6, 2013, 10:10 - 11:50
Location: Barbie Tootle

[Abstract] This paper presents the design of a current-mode CMOS logarithmic amplifier, which by design is insensitive to ambient temperature variations. Its operational current ranges over 100fA - 100nA, which covers the full range of sub-threshold region. Unlike conventional logarithmic amplifiers, the proposed approach directly produces a current signal as a logarithmic function of the input current. The core of the proposed circuit is translinear ohm's law principle, which is implemented by a floating-voltage source and a pseudo-linear resistive element within a translinear loop. The temperature sensitive parameters are reduced using a translinear-based resistive cancelation technique. Measured results from prototypes fabricated in a 0.5µm CMOS process show that the amplifier exhibits an input dynamic range of 120dB and a temperature sensitivity of 230 ppm/°K.

[Abstract] Inner-product is an important computation primitive involved in pattern classifiers and support vector machines. Its complexity in mathematical computation causes tremendous resources cost and low energy efficiency when it is implemented in digital VLSI circuit. Many analog computational circuits have been investigated to tackle the issue. In our previous work, an efficient piecewise linear (PWL) approximation technique named as margin propagation (MP) has been successfully synthesized into various log-domain computations. We have also verified that MP based computation can be easily mapped into analog circuit implementation. The operation of the MP circuits requires only addition, subtraction and threshold operations and hence is independent of transistor biasing (weak, moderate and strong inversion). In this paper, we extend MP based PWL approximation circuit to inner-product computation. Measured results from prototype MP circuits fabricated in a 0.5μm standard CMOS process validate the functionality of the approximation circuit in a bias-scalable manner.

[Abstract] This paper presents a new concept for reducing on-resistance of high-voltage drivers based on stacked MOSFETs for various supply voltages. A theory to calculate gate voltages of an N-stacked CMOS driver to drive the maximum drain current at a minimum on-resistance is introduced. According to the calculated gate voltages, a circuit design methodology is described to generate these voltages. The principle is applied on a 2-stack CMOS driver in 65-nm with a nominal voltage of the I/O-devices of 2.5 V. For various supply voltages, simulations show an improvement of 27%-86% reduction of the initial on-resistance and approximately 16%-83% improved rise and fall times of the output signal at a load capacitance of 150 pF if compared to previous work. The principle can be applied to N-stack driver transistors.

[Abstract] A high-temperature comparator with rail-to-rail input voltage range is presented. The design uses a 0.5-um silicon-on-insulator (SOI) technology. The rail-to-rail operation is achieved using two folded-cascode differential amplifiers operating in parallel as an input stage. The output of the appropriate amplifier is connected to the comparator output through a logic-controlled analog multiplexer. The simulations show that the comparator remains operational over the full rail-to-rail common-mode input voltage range, with somewhat degraded performance for input voltages close to either supply voltage.

Session B2L-B: VLSI Design Reliability

Chair: Shantanu Chakrabartty, *Michigan State University*
Time: August 6, 2013, 10:10 - 11:50
Location: Hayes Cape

[Abstract] This paper has analyzed the conventional glitch-free clock multiplexers. An improved glitch-free clock switching circuit is proposed, which introduces fault-tolerant function that is able to switch away from a failed clock, and adds configurable bit that controls the switching clock edge. It is quite suitable used as a global clock multiplexer in FPGA. This switching circuit achieves three basic functions: clock select, clock enable, and clock disable. As the configurable low-level triggered latch is proposed, switching time is reduced by 1/3 compared to the double D flip-flops type clock multiplexer. This proposed switching circuit operates at 100 MHz with 17uW power consumption using TSMC 0.13um CMOS process parameters with a supply voltage of 1.5V.

[Abstract] This paper describes a technique that exploits the process variation in Field Programmable Gate Arrays (FPGAs) in order to generate varying frequencies using asynchronous ring oscillators. To study its feasibility, Physical Unclonable Functions (PUFs) are implemented on FPGAs for generating unique signatures based on different frequencies generated from oscillators. The variation in frequencies generated from identically laid-out oscillators across the device can generate unique signatures, which is used in device authentication and cryptographic applications

[Abstract] Transistors in nanometric technologies are increasingly susceptible to faults due to physical limitations. Since the constituent gates of a logic circuit actually have different failure rates, the assumption of constant gate failure rate in existing reliability evaluation and fault tolerant design is not desirable. This paper analyzes transient faults in CMOS logic gates at transistor level and proposes a mathematical model. Examples based on the benchmark circuit are provided to demonstrate the efficiency of the proposed model in both reliability evaluation and fault tolerant design.

[Abstract] Reliability is a crucial factor in modern processors, which are designed in deep sub-micron (DSM) technologies and perform numerous tasks at high speed in less time. Modern DSM technologies are ever more vulnerable to soft errors, which can propagate in pipeline processors and may lead to malfunctioning. Contemporary soft error mitigation techniques introduce redundancy in intermediate registers alone, which addresses soft error occurrence in hardware registers only. However, in modern DSM technologies soft error can equally affect combinational circuits, hence in pipeline processors data paths also requires soft error mitigation. In this paper we propose a soft error mitigation technique in pipeline processors that addresses soft error in data paths. We utilized temporal redundancy in data path along with automatic repeat request (ARQ) protocol in all pipeline stages. Our novel ARQ based technique detects soft errors in the data path to process the reliable data to the successive stages of the pipeline. Our synthesis results show that our implementation 50% better in terms of latency and requires 1.53 times lesser area overhead compared to best state-of-art techniques.

[Abstract] We propose a high level methodology for Finite State Machine (FSM) protection. As the proliferation of electronic devices that process sensitive data continues so do the potential attack vectors to circumvent them. These attack vectors include side-channel attacks that use physical byproducts to reconstruct the internal operation of a device. The methodology, validated using preliminary hardware synthesis results, removes the correlation between common attack models and both underlying FSM logic as well as the associated power consumption.

Session B2L-C: Delta-Sigma Modulators

Chair: Vishal Saxena, *Boise State University*
Time: August 6, 2013, 10:10 - 11:50
Location: Cartoon Room I

[Abstract] Currently, less-than-one-cycle loop delay is the key factor to impede higher clock rate and wide bandwidth continuous-time oversampling modulators. In this paper, a new method to develop a beyond-one-cycle delay CTDSM based on the proper rational NTF synthesis is proposed without an extra fast path . Also, further loop delay extending will be implemented by a fully s-domain deviation. Compared with the traditional impulse invariant way in DT-CT mapping, this new method shows a much simpler work. In the end, the paper discusses time-interleaved implementations in the proposed beyond-one cycle delay modulators, including offset, gain and sampling time error mismatches between channels.

[Abstract] In this paper, we present a hybrid operational amplifier frequency compensation topology to maximize unity-gain bandwidth particularly for use in continuous-time delta-sigma modulators. Unlike well-known existing compensation topologies, the proposed compensation topology and UGBW maximization technique provide both a maximum UGBW and an adequate phase margin, due to the appropriate non-dominant pole and zero positions. The proposed topology performance is validated by SPICE simulation using 28nm CMOS device models.

[Abstract] This paper presents a design methodology to synthesize band-pass continuous-time Sigma-Delta (SD) modulators with a widely programmable notch frequency for the efficient digitization of radio-frequency signals in the next generation of software-defined-radio mobile systems. The presented modulator architectures are based on a fourth-order loop filter " implemented with two LC-based resonators " and a finite- impulsive-response feedback loop to increase their flexibility and degrees of freedom, considering three different cases for the digital-to-analog converter waveform, namely: a return-to-zero, a non-return-to-zero and a raised-cosine waveform. In all cases, the notch frequency can be reconfigured from 0.1fs to 0.4fs, while keeping the noise shaping performance, the stability and low sensitivity to circuit-element tolerances. This feature can be combined with undersampling techniques to achieve an efficient and robust digitization of 0.5-to-5GHz signals with scalable resolution and programmable signal bandwidth.

[Abstract] A continuous-time CCO-based ADC has been implemented in 0.13um CMOS technology. Two important techniques are incorporated: a V/I converter with two different size PMOS differential pairs crossly-coupled to achieve non-linearity cancellation, and a stack structure with V/I converter and the CCO sharing currents to achieve low power consumption. In this design, no high voltage device have been used and all the blocks used are digital in nature thus scalable except the V/I converter. This prototype ADC achieves a peak SNDR/SFDR of 60.3 dB/71 dB over a bandwidth of 5 MHz, and dissipates overall power of only 1.2 mW.

Session B2L-D: Special Session: University and Industry Training in the Art of Electronics

Chair: Steven Bibyk, *Ohio State University*
Time: August 6, 2013, 10:10 - 11:50
Location: Cartoon Room II

[Abstract] Hands-on learning has proven to be very effective in motivating electrical engineering students to study foundation courses. The advent of student-owned, functionally robust, portable test and measurement equipment, now offers fertile ground for developing innovative pedagogy to more fully engage and inspire students. In this paper we discuss two examples of how student-owned test and measurement instrumentation is impacting the electrical engineering curriculum at RIT: in a Freshman Practicum course with a flipped lab and in a Certificate Program in Mechatronics to enable the required laboratory content to be delivered online.

[Abstract] Education technology for electronic hardware testing was combined in the form of an analog/mixed signal development kit with miniaturized testing instrumentation to explore oscillator and PLL designs, operating at audio frequencies. Even so, the principles of analog design for Software Defined Radios can be demonstrated.

Session B2L-E: Radio Frequency Integrated Circuits

Chair: Nathan Neihart, *Iowa State*
Co-Chair: Mona Hella, *Rensselaer Polytechnic Institute*
Time: August 6, 2013, 10:10 - 11:50
Location: Suzanne M. Scharer

[Abstract] This paper presents a two-tone system to control the center frequency and bandwidth of an RLC tank in front-end LNAs. The control mechanism is based on the characteristic of an RLC tank, which induces a phase difference between the two frequencies. The proposed system is implemented on chip in the TSMC 0.18 μm CMOS technology. The LNA's centre frequency and bandwidth were set at 2.45 GHz and 60 MHz, respectively. Precisions of 0.2% for centre frequency control and 8% for the bandwidth control were achieved. The two-tones phase delay principle can be generalized to tuning based on any information signal containing two tones with related phases and known frequencies.

[Abstract] A feedback-based active interference suppression technique employing harmonic rejection mixers (HRMs) for enhancing linearity in a broadband channelizer is proposed. In the approach, an interferer is down-converted to baseband, low-pass filtered and then up-converted, where it is subtracted from the input. Using previously reported HRMs capable of LO frequency synthesis in both the down-conversion and up-conversion paths, wideband interference cancellation is achieved without the use of a wide tuning range PLL. Limitation on the maximum achievable interference rejection due to unwanted interaction between inband and out-of-band harmonics is identified. An approach based on a 2-step up-conversion in the feedback path is proposed to remove this limitation. The effectiveness of the proposed technique is verified through simulation.

[Abstract] In this paper, the oscillation frequency and waveform amplitude of a high frequency differential ring oscillator are analyzed and derived with a new platform. The obtained equations describe the nonlinear dependence of amplitude and frequency on the tail current, number of delay cell stages, and transistor sizes. The accuracies of the obtained equations are verified by the Cadence Spectre simulation results and experimental data. Compared with currently available expressions, the obtained equations show significantly improved accuracies; therefore they can be used to guide and facilitate high frequency differential oscillator design in submicron CMOS technology. The derivation platform can also be used to analyze other ring oscillator topologies.

[Abstract] This paper presents a design for a highly-linear power amplifier " based on GaN HEMT- with an output power excess of 9W, and an ultra-broad bandwidth extending from 0.3 to 3.7 GHz (170%). Different design techniques are adopted to achieve a flat power gain of 9.5 ± 1 dB over the entire operating bandwidth. Sixth and fifth order low pass matching circuits are designed for input and output matching, respectively, providing optimal fundamental and harmonic impedances within more than 3 octaves of operation. The designed power amplifier exhibits a small signal gain more than 9.5-dB, an input/output return loss better than 10 dB within the operation bandwidth. Second and third-harmonic inter-modulation distortions are far below -36dBc and -45dBc @ 3GHz, respectively, at an input power of 30-dBm over the entire frequency band, while achieving a power added efficiency (PAE) better than 25%. At a frequency spacing of 160 KHz, a maximum value of the output OIP2 and OIP3 are found to be greater than 50-dBm, and 60-dBm, respectively.

[Abstract] A 780-MHz low power RF transceiver for wireless nodes in IoT (Internet of Things) applications was designed and implemented in 65nm Si CMOS process. Direct-Digital modulation and regeneration configured receiver are adopted in the RF transceiver. Measurement shows that the transceiver can provide a data rate from 100Kbps to 1Mbps (peak data rate can be up to 2Mbps). With a 1.2 V DC supply, the transmitter can present 3 emission levels (-9dBm,-1dBm, 4dBm) and the corresponding power consumption is from 4.3 to 9.6mW. The receiver can present -65dBm sensitivity at a BER of 0.001 with 3.75mW power consumption. The chip size is 1mm2, and the whole transceiver is integrated in high level with minimized external components.

Session B2L-F: Bio-Inspired Green Technologies

Chair: Hoda Abdel-Aty-Zohdy, *Oakland University*
Time: August 6, 2013, 10:10 - 11:50
Location: Rosa M. Ailabouni

[Abstract] In this work we will present an overview of the memristor device and the microfabrication approach for this device. We describe possible integration with CMOS circuit proposed by researchers [1]. This proved the memristor neuromorphic circuit exhibited behavior analogous to STDP in which the changes in current measured through the memristor caused by changing memductance of artificial neurons were strikingly similar in shape to post synaptic current changes from rat hippocampal neurons. This study proved memristor based neuromorphic circuits exhibit STDP and may be capable of emulating learning processes and as fabrication techniques become more advanced, neuromorphic circuits can potentially reach physiological synaptic density values of up to 10^10 synapse/cm^2.

[Abstract] In this paper, the HIV-1 reduced order infection model based on real data is controlled by different control Lyapunov function laws. we studied the performance and stability of HIV-1 dynamic response. Constructing of Lyapunov function is investigated and the proof of global stability is provided. The control laws are designed to damp the oscillation of transient response and stabilize the reduced model to prevent progressing HIV-1 to AIDS.

[Abstract] In this paper, we use the Extended Kalman Filter (EKF) to ensure that the measured data of an implementable biological model is accurate amidst noisy signals. A simplified circuit model of the retina is designed in order to validate how the EKF can be used to ensure that the model's voltage measurements are accurate. The results are compared with those of a Kalman Filter by calculating and comparing their Root Mean Square Error. Results show that the EKF has higher measuring accuracy and, therefore, could be utilized to ensure the accuracy of measurements in biological models.

[Abstract] The analysis of analog circuits containing feedback has long been confusing due to incomplete definitions of fundamental terms such as loop gain, open loop gain, and port impedance with feedback zeroed, Z0'. In this paper, following a driving point impedance perspective, a unified model is developed that evolves into the Black's block diagram to properly identify the feedback analysis properties.

[Abstract] Wavelet transform is favorably used for compressing and filtering complex signals from chemical sensors for classifications. Daubechies 4 transform (D$) is used and found to be more accurate especially with chemical mixtures, while being fairly simple to implement, and effectively preprocess data from 32 sensors, and then outputs the result to a Spiking Neural Network (SNN) processing chip for chemical classification. The system features SPI bus for data input and output. It accepts 32 bit fixed point value inputs for faster processing using bit shifts and adds for multiplication. The system has been designed to be modular and capable of being used on other potential applications. Experimental measurements of mixed gases including IEDs are presented. This paper presents the design evaluated on a VHDL platform, to be implemented on a tiny chip, for fabrication through MOSIS 0.5 um CMOS technology. D4 had more capability than Haar transform especially with gas mixtures, as with 0.1% of TATP in Acetonitrile. Experimental results are presented with good sensitivity, stability, and tolerance.

Session B3L-A: Analog Design Techniques III

Chair: Igor Filanovsky, *University of Alberta*
Time: August 6, 2013, 13:10 - 14:50
Location: Barbie Tootle

[Abstract] This paper focuses on the design of two nondelaying cascaded SC integrators. Given the importance of good settling in SC filters, a design method is presented which optimizes power consumption for a given settling accuracy. Another issue is also addressed here concerning a possible excitation case that might lead to settling "hesitation" in two nondelaying cascaded SC integrators which affects settling accuracy. Circuit simulations confirm the analytical methods and simulations. The proposed analytical equations can be easily embedded into behavioral models used for large system's simulations in early design stages.

[Abstract] Passive mixers became an essential component of SAW-less receivers. It is well known that the passive mixer behaves as a switched-capacitor circuit (SC) but to our knowledge, there is no reported analysis of the mixer impedance that accounts for is behavior. In this paper we present for the first time a novel formula for passive mixer output impedance using SC techniques. We prove that the lower limit of the mixer impedance is proportional to the switched capacitor resistor 1/(FLOC) different from the previously reported mixer switch ON resistance. We also explain that the equation is useful in estimating output bandwidth in voltage mode mixers and blocker filtering in voltage and current mode passive mixers.

[Abstract] This paper deals with the design of a power efficient switching regulators intended for linear power amplifiers employing envelope tracking techniques in wideband wireless standards. The bottlenecks in existing envelope tracking solutions involve a trade-off between ripple voltage, slew rate and bandwidth. The slew rate limitation is identified as the main challenge, then a 'bang-bang' slew-enhancement technique is proposed. This approach enables the use of efficient supply modulators in wideband power amplifiers. The proposed scheme does not significantly degrade PA efficiency and preserves the stability of the switching regulator. The prototype has been implemented using the TSMC 0.18 µm technology; schematic simulation results in Cadence® are presented to demonstrate the feasibility of the proposed techniques.

[Abstract] In this paper, we present a tunable continuous-time band-pass sigma-delta (ΣΔ) analog-to-digital converter (ADC). Our design is suitable for multi-standard multi-user applications. Additionally, the tunability advantage enhances the obtainable resolution while reducing the power consumption by only operating in the desired bandwidth from the reserved bandwidth required for ADC's application. Our simulation results demonstrate that a relatively high SNR can be obtained using the designed ΣΔ ADC. We provide an implementation of the designed ADC using Gm-C circuits with 0:18 m IBM CMOS technology. The circuit operates with 8MHz clock frequency and achieves 57.6dB Signal to Noise and Distortion Ratio (SNDR) with 20kHz bandwidth. At the mentioned clock frequency and 1.5V supply level, the circuit consumes less than 1mW power. Our HSPICE simulation results are in very good agreement with our simulated model based on second order modified all-pass transfer functions. The effective number of bits obtained from our implemented ADC was observed to be ENOB=9.28 bits.

[Abstract] A lot of work has been done to identify the right stress pattern specific to each IO interface. Tradeoffs between test-time and test coverage must be made depending on the test goals. APGC can speed up the test and validation execution time by at least 500 times compared to software, while offering comparable BER margin measurement.

Session B3L-B: VLSI Design, Routing, and Testing

Chair: Nader Rafla, *Boise State University*
Time: August 6, 2013, 13:10 - 14:50
Location: Hayes Cape

[Abstract] In this paper, we propose a basic crosstalk avoidance router using two area usage restrictions. They are "a wide pitch restriction" and "a bounded area restriction". The wide pitch restriction means that the router using only wider pitch than the minimum pitch from the process technology rule. The bounded area restriction means that a router only executed inside minimum bounding box with some redundancy area of a net. According to the experimental results of some circuits including practical, our proposed router achieved the higher routability results in shorter execution time than those of the conventional maze router.

[Abstract] Resilient system is used to eliminate the voltage/frequency margin for further power reduction/performance improvement. With replacing critical flip-flops (FFs) with error detection sequential (EDS) circuits and the occurring of error-path circuits, resilient system brings in new challenges for the path delay testing. In this paper, three scan EDS designs are analyzed and compared. Then a novel OR-tree delay testing method is proposed and experimental comparison is made showing our method's higher efficiency than a baseline method.

[Abstract] A key component of integrated optic design is waveguide routing; however, unlike VLSI, where signal nets are routed with metal layers and vias, photonic waveguides are fabricated in planar substrates. For many applications, our studies show that the waveguide routing problem can be formulated as planar channel routing. Signal losses become a major factor due to the insertion losses of planar waveguide crossings. Channel routing must therefore take into account these losses. This paper investigates methods for adapting traditional VLSI channel routing techniques for integrated optics --- specifically, a technique based on left-edge-style track assignment. We show how incorporating waveguide crossing constraints into the underlying constraint model affects the routing solution, and describe the necessary modifications and extensions to the routing technique to properly exploit optical technology. We implement the channel router, describe the experimental results, and compare the cost of solutions with respect to waveguide crossings, corresponding to signal loss, and channel height.

[Abstract] This paper presents a generic variable-latency design methodology, which includes timing analysis, delay test input generation, design of a completion prediction unit for logic computation latency, and a clock gating scheme. Our experiments based on on the 45nm Nangate open cell library and the des MCNC benchmark circuit show that, for a clock gating occurrence probability 6.25%, our technique leads to maximum 8.29%, 9.96%, and 9.18% area reduction, and 27.54%, 28.08%, and 29.93% power reduction with a prediction unit of 4, 5, and 6 inputs, predicting the top 1, 2, and 4 timing-critical paths, respectively.

[Abstract] The need for faster digital circuitry has turned the researchers to alternative number systems and arithmetic level modifications. One such number system being used is the Residue Number System (RNS). With computationally fast addition, subtraction and multiplication it has become widely used in many vast areas of Digital Image Processing (DSP). The drawback to using RNS is that it has several computationally slow and resource intense operations, most notably, scaling and conversion. This paper presents a novel implementation of three moduli set scaling system and the constant scaling factor. The main difference of the proposed system to existing scaling systems includes elimination of the overhead conversion system and employing modular reducers in implementation of the design. Many algorithms for fast scaling in RNS exist, but this paper will focus on developing a particular algorithm using adder based techniques.

Session B3L-C: Special Session: High-Precision and High-Speed Data Converters I

Chair: Samuel Palermo, *Texas A&M University*
Time: August 6, 2013, 13:10 - 14:50
Location: Cartoon Room I

[Abstract] This paper describes a background calibration technique that linearizes pipelined ADCs by correcting for errors in the digital domain. This also relaxes the requirements for the analog components and enables power and area savings. The calibration technique does not require a separate reference ADC that samples the input, nor the generation of digital correlation signals or extra analog calibration components. The calibration technique is robust and easily implementable in any digital technology. The implementation of the digital calibration algorithm requires minimal digital resources and less than 1% of the overall ADC power consumption.

[Abstract] The paper presents a digital background calibration technique for pipelined ADC in low voltage condition. The calibration removes the interstage gain error which is significant in pipelined ADCs.

[Abstract] Capacitor mismatch and finite op-amp gain are two main error sources for high-resolution pipelined ADCs. This paper presents a high-efficiency digital calibration technique for multi-bit/stage pipeline ADCs.

[Abstract] This paper presents a 9-bit 125-MS/s switched-current pipelined analog-to-digital converter (ADC) with low transmission error and small channel charge injection. To decrease the transmission error, a current mirror with op feedback is used. Furthermore, both dummy switch and offset current cancellation are adopted to reduce the channel charge injection. As the proposed pipelined ADC is implemented in TSMC 1P6M 0.18-µm CMOS technology, the simulation results show that the signal-to-noise and distortion (SNDR), differential nonlinearity, integral nonlinearity, and power consumption are 55.56 dB, -0.21~+0.19 LSB, -0.1~+0.37 LSB, and 45.5 mW, respectively, at the input frequency of 5MHz, sampling rate of 125 MS/s, and the supply voltage of 1.8 V. Notify that the figure of merit of the proposed pipelined ADC is about 0.78pJ/conversion at the operational current range of -20µA~+20µA.

[Abstract] A digital calibration technique to linearize the residue amplifier in pipelined SAR ADC based on Independent Component Analysis (ICA) is presented. The proposed technique utilizes a single, one-bit pseudorandom noise (PN) to simultaneously identify all coefficients of a correction polynomial. Behavioral simulation results demonstrate the effectiveness of the technique, in which the SNDR and SFDR performance of a 12-bit pipelined SAR ADC is improved from 54 dB and 69 dB to 72 dB and 100 dB, respectively. Some circuit design details are included for the PN injection circuit as well as the digital calibration logic.

Session B3L-D: Special Session: Advancing the Frontiers of Solar Energy

Chair: Michael Soderstrand, *Synapse International*
Time: August 6, 2013, 13:10 - 14:50
Location: Cartoon Room II

[Abstract] Volunteers converted an old frame chicken coop into an energy efficient solar-based sustainable home using recycled and donated parts along with purchased items and services funded from periodic yard sales. It was built for less than $10 per square foot and uses less than 500 KWH of power per month. Earth Connections community center is an extremely energy efficient building featuring a solar assisted geothermal system of plastic tubing embedded in the ground connecting thermal collectors on the roof. The final case study is in mobile solar energy " an electric golf cart whose batteries are recharged by solar photo-voltaic panels.

[Abstract] Several utility-scale photovoltaic (PV) power plants have been built in North America in recent years. These plants typically range in size from a few megawatts to tens of megawatts and connect either to the utility's distribution or transmission systems where technical interconnection requirements tend to be quite different. This paper provides an overview of key technical requirements for distribution and transmission system interconnections and how these requirements affect the design of the plant.

[Abstract] The highest efficiencies in solar power systems (25%) are achieved in Concentrated Solar Power (CSP) systems using a two-axis tracking parabolic dish collector (PDC) with a Stirling engine. Unfortunately, such systems are very costly. An alternative system makes use of an array of small inexpensive mirrors each directing the sunlight to a single optical fiber. The optical fibers from each mirror transport the light to a central receiving unit where the heat drives the Stirling engine. In addition, a propane or natural gas heating element can augment the solar energy when clouds come by or during the evening hours.

[Abstract] In this paper, the path planning strategy for solar powered UAVs at low altitude is examined including the weather factor in energy harvesting. The designed path will maximize the difference between the collected energy and the consumed energy, named net energy, when flying from the specified initial point to the final point. A weather map providing information such as regional precipitation is utilized to predict the solar spectral density for the concerned areas. We propose a graph based approach which divides the concerned areas into small grids to evaluate the solar spectral density corresponding to the local weather and then build the energy intensity distribution map as a function of coordinates. The Bellman-Ford algorithm is utilized to find the optimal path which yields maximum net energy at terminal point. Simulation results for level flight are presented.

[Abstract] The design of a multijunction photovoltaic system, particularly the choice of the individual bandgaps, is sensitive to the specific operating conditions of the system. Laboratory characterization is typically carried out at a standard temperature, such as 25 ºC, using a standard solar spectrum, such as an AM1.5 direct spectrum. In reality, the system should be designed for operation at its anticipated temperature of operation, taking into account the spectral variation of the solar radiation over the course of the day and year. In this paper, the effects of such variations in operating conditions on the performance of different designs are examined.

Session B3L-E: RF/Optical Devices and Circuits

Chair: Mona Hella, *Rensselaer Polytechnic Institute*
Co-Chair: Nathan Neihart, *Iowa State*
Time: August 6, 2013, 13:10 - 14:50
Location: Suzanne M. Scharer

[Abstract] Micro-fabricated calorimeters have been extensively used for determination of thermo chemical values and reaction kinetic studies. However, micro-fabricated calorimeters as power sensors have been mostly unexplored. In this context, miniaturization of an absolute flow calorimeter capable of measuring RF power is proposed. This novel implementation using micro-fabrication is capable of measuring power from 100 μW to 100 mW at frequencies from DC to at least 12 GHz. In this paper, a micro-fabricated flow calorimeter is demonstrated and several initial test results, such as DC power measurement and the impact of flow rate on heat transferring, are reported. The obtained results will play an important role in performing RF power measurements in the future.

[Abstract] This paper presents a novel high efficiency RF to DC converter for RFID applications. The proposed circuit is designed in 90 nm CMOS technology using single source RF. It exploits an internal Vth cancellation technique along with a leakage current reducer. The circuit performs well in the low input power threshold. The Simulation results at frequency of 920MHz show that the PCE has improved compared to the conventional rectifier using diode connected and Vth cancellation techniques. The measured PCE is 36.3% at -14.3dBm and can be improved to 54.5% with an impedance matching network between the source and rectifiers' input.

[Abstract] We describe a new integrated rapidly tunable optical delay line optimized for optical coherence tomography (OCT) systems. The integrated system uses a planar waveguide and echelle gratings combined with a specially designed micro-electromechanical system (MEMS) mirror. These components are all fabricated on the same die, thus enabling a very compact and cost effective device. The delay line system has a simulated scanning speed of more than 10 kHz and can provide a continuously tunable variable delay difference of 6.7 ps. The whole system fits on a chip of 12 mm by 8 mm.

[Abstract] A 10-Gb/s integrated limiting receiver for silicon photonics interconnects is proposed with detailed system level and circuit level design and analysis. Silicon photonics devices fabricated in silicon-on-insulator can be seamlessly integrated with standard CMOS process, which allows compact system integration and significantly lower power dissipation. By taking the advantages of low parasitic capacitance of the on-chip Ge detector and adopting bandwidth extension techniques, a total bandwidth of 7.2 GHz with 87 mW power consumption is obtained in a 130 n m CMOS process. The final differential output signal has a peak-to-peak swing of about 1.2 V and a peak-to-peak jitter of 14.3 ps and 9.8 ps for 10-Gb/s PRBS7 data with an average received optical power of -17 dBm and 0 dBm, respectively.

[Abstract] This work presents the design and simulated performance of a variable bandwidth, power-scalable optical receiver front-end in 65 nm CMOS technology. The proposed receiver front-end includes a transimpedance amplifier (TIA) and 3-stage post-amplifier with an offset compensation loop. The proposed transimpedance amplifier is based on the shunt feedback topology while the post amplifier and the offset-compensation loop use the Cherry-Hooper inverter-based topology. In order to make the receiver power and bandwidth scalable a binary-weighted current-controlling MOSFET array and a tunable resistance bank are also proposed. The receiver front-end can vary the supported data rate from 1.25 Gb/s to 20 Gb/s with proportional power dissipation and constant gain of ~75 dBΩ. The overall power dissipation varies from 0.32 mW to 13.5 mW as the data rate scales maintaining an energy per bit lower than 700 fJ at all data rates. The variable 3 dB bandwidth is from 0.85 GHz to 13.5 GHz with input referred noise density from 8.46 pA/√(Hz) to 18 pA/√(Hz).

Session B3L-F: Carbon Nanotube-Based Sensors and Beyond

Chair: Nayla El-Kork, *KUSTAR*
Time: August 6, 2013, 13:10 - 14:50
Location: Rosa M. Ailabouni

[Abstract] This paper introduces a method to combine temperature, gas and pressure sensor to a system on a chip. The sensing elements are single walled carbon nanotubes (SWCNT). CNT has excellent resistance changes when the condition changes. Thus, based the I-V curve, the resistance changes are measured. There is a typical issue using CNT to measure the temperature and the gas since both factors have effects to the resistance. This paper provides an interesting method to fix this problem.

[Abstract] Carbon nanotubes have been widely studied for their applications in sensors due to their promising physical and chemical properties. In this paper, we explore the potential of applying carbon nanotubes to gas sensing equipment. The sensor uses an antenna to detect change in return loss from normal operating frequency on exposure to different polar and non-polar gases. Carbon nanotubes help amplify this shift to improve the gas sensitivity. The presented study shows that carbon nanotubes can provide a frequency shift in return loss that can identify various gases. Simulation results from ANSYS High Frequency Simulation Software provide proof of the concept while experimental results from three gases have shown repeatable frequency shifts.

[Abstract] Unavailability of suitable simulation models poses a particularly difficult problem in the field of CMOS analog circuit design for deep cryogenic applications: the performance of the design cannot be verified prior to fabrication. Therefore, the first generation circuits previously reported by the authors for the purpose of reading out Single Electron Transistor (SET) signals- while operating immersed in liquid helium- were equipped with numerous external controls to ensure its proper functionality. In this paper we address the issue of external manual biasing and present a novel approach to achieve self-regulated automatic tuning- one of the most important requirement for future stand-alone, self-sufficient SET readout circuitry. The proposed scheme is mismatch insensitive, does not compromise the speed and adds very little power overhead to the previous designs.

[Abstract] Devices like solar cells and displays require high quality polycrystalline-Si (pc-Si) thin films, which are grown by high temperature crystallization of thin films of amorphous silicon (a-Si) on expensive substrates. Recently, pulsed laser annealing appears to be an effective way for crystallization of thin films on low cost substrates with high precision. This paper presents heat transfer simulation of very thin silicon (Si) film using COMSOL Multiphysics. The results show that higher power density can melt the film at shorter times compared to lower power density. The annealing depth and temperature at any depth can be precisely controlled by optimizing heat source power density, pulse width and exposure time. Therefore, it is possible to crystallize Si films by controlled melting without melting the substrate.

[Abstract] Reducing the size of metal-semiconductor (M-S) contacts to sub 20 nm results in a deviation of the interface barrier characteristics from the those predicted by the conventional theory of (M-S) contacts. This is attributed to the enhancement of the electric field at the interface due to the charge confinement in the nano metal particle. We introduce analytical analysis and finite element simulations for calculating the interface parameters. The significant electric field enhancement and the reduction of the barrier thickness account for the reversed rectification behavior compared to the conventional I-V data of M-S junctions.

Session B4P-G: Linear and Non-Linear Circuits and Systems

Chair: Hari Reddy, *California State Long Beach*
Time: August 6, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] The complete analytical model for dual or six port directional coupler is developed, and closed form equations using operational parameters are presented for the first time using transformers. Six-port coupler using the model developed is designed and simulated with frequency domain simulator Ansoft Designer for verification. Final design is implemented and measured with network analyzer. Analytical, simulation and measurement results are compared and agreement has been values. Matlab GUI to design six-port directional couplers has been developed for academic and commercial use with implementation of the analytical model developed in this paper.

[Abstract] The appropriate linear dynamic modeling of continuous"time filters (CTFs) with automatic tuning loops should be obtained to assure stability in case an improved design of the loop controllers is to be carried out. With this aim, starting from a general and systematic analysis in order to obtain an equivalent small"signal linearized incremental model, from which transfer functions between output variables and control voltages are derived, the subsequent design of compensated loops with enhanced stability and dynamic performance is required. This systematic procedure allows obtaining improved controllers for the two involved control loops. However, CTFs with automatic tuning loops are nonlinear feedback systems with potential instability. What is more, nonlinear phenomena, which cannot be predicted by a design-oriented small signal modeling approach, are observed in this kind of tuning systems. The purpose of this work is to highlight that when control parameters are varied, the system could present different kinds of dynamical nonlinear phenomena such as bifurcations and chaotic behavior, which cannot be predicted by the small signal design-oriented model.

[Abstract] In most phase locked loops, an obvious trade-off exists between settling time, output jitter and power consumption. However, dependence of jitter on settling time is commonly ignored while evaluating PLL designs. In this paper, the tradeoffs between settling time and jitter is analyzed for different types of All-Digital PLLs (ADPLLs). Based on these analytical results, a Figure of Merit (FoM) for evaluating PLLs, which takes settling time into consideration, is suggested. Also, a 2.4-GHz Direct-Digital Synthesis based AD-PLL model, which combines phase detection switching, adaptive gain and FSM based mechanism, is explored for simultaneous optimization of PLL performance parameters.

[Abstract] We focus on the frequency analysis of LTV systems within the larger context of 2-D analog filtering. The available techniques for characterizing 2-D analog filters are explored. The frequency analysis of 2-D analog circuits and systems, based on the classical two-dimensional Laplace transform (2DLT), is invigorated. The 2DLT technique leads to the development of a bifrequency theory for autonomous dynamic systems. The contents of existing literature are complemented more than duplicated.

Session B4P-H: Linear and Non-Linear Systems

Chair: Samuel Palermo, *Texas A&M University*
Time: August 6, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] We analyze properties of two singularly perturbed nonlinear systems with mixed-mode and chaotic oscillations and propose two op-amp RC circuits for the systems. The three-variable mathematical models of both systems (with cubic nonlinearities) are linked to the second Newton's law $d^2x/dt^2=F(t,x,dx/dt)/m$, with $F(t,x,dx/dt)$ containing a memory term. This allows further to use a scalar equation $x'=f(x)+\int y(\tau,\int z(\theta,x)d\theta)d\tau$ as a base to design the circuits. The mixed-mode and chaotic responses as well as bifurcation diagrams of the circuits are obtained through Spice and Matlab simulations,

[Abstract] Divide-by-3 injection-locked frequency dividers with a direct forcing of the synchronization signal are modeled and analyzed. The locking mechanism underlying their operation is investigated and analytical equations are derived to predict the locking range as a function of the circuit parameters. The derived results are in good agreement with simulation results obtained by using BSIM3 models of active devices in 0.13um technology.

[Abstract] A comprehensive methodology of analysis of Injection-Locked Frequency Dividers (ILFDs) allows us not only to estimate the locking range, the amplitude and the phase of the locked oscillations and their stability, but also to investigate the transition from the locking mode to the pulling mode, that happens in proximity of the boundaries of the locking region. We highlight that there exists a border region where the two modes of operation can coexist and the occurrence of one mode, or the other, depends only on the initial conditions. Numerical simulations confirm analytical predictions.

[Abstract] This paper presents a floating inductor implementation technique using active components. Floating inductor is an integral part of switching voltage regulator. Implementation of floating inductor is a primary bottleneck of on-chip implementation of switching regulator. In current CMOS circuit design, the implementation of the passive inductor is either external to the chip or fabricated as a part of the package. If it is incorporated within the chip, the passive inductor occupies very large chip area. In addition, passive inductors are not electrically tunable, which makes them unattractive for reconfigurable system-on-a-chip (SOC) designs. In contrast, an active device based floating inductor can be inserted within the chip. This new approach adapts the use of both positive and negative current conveyors. The proposed circuit allows the inductance value to be adjusted electronically by changing the bias current Io of the current conveyor. Design of the circuit is demonstrated using 0.5µm technology on Cadence Virtuoso with a +3.3V supply voltage. Simulation results are provided to verify the proposed design. The proposed the design can be tuned further for nanoscale environment.

Session B4P-J: RF Active and Passive Circuits

Chair: Vishal Saxena, *Boise State University*
Time: August 6, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] This paper presents a novel reconfigurable tri-band BPF with two-state frequency responses, where tri-band and dual-band bandpass characteristics can be conveniently switched by turning pin diodes on and off. The filter can operate as a tri-band BPF with center frequencies 900 MHz, 2.45 GHz and 3.5 GHz for GSM and WiMAX applications. On the other hand, it can operate only at 2.45 GHz and 3.5 GHz for (WiMAX) rejecting 900 MHz GSM signals. The design proposes simple resonance microstrip structures integrable with pin diodes. Bias circuits are designed and optimized with precisely selected practical lumped components. The proposed filter is simulated, optimized, and fabricated using low loss Teflon substrate. The filter provides significant size reduction and superior enhancement in insertion losses.

[Abstract] This paper presents a 2.4GHz/5.25GHz dual band two-stage differential low noise amplifier (LNA) with a variable gain which is implemented with 0.18-um CMOS technology. In the proposed differential LNA, two cascode pairs are used to have low current and high isolation; and that two current-reused paths are presented to have low power consumption. Besides, the variable gain is completed by adjusting the gate voltages of MOSFETs, M3 and M7. Furthermore, a capacitor C2 is added to the gate of transistor M2 to have a stable bias voltage by filtering out the RF signal; and that a differential mode is considered to have good linearity and high gain. The simulation results present that the gain varies from 16.66 dB to 19.89 dB at 2.4 GHz, whereas the gain varies from 2.63 dB to 16.33 dB at 5.25 GHz.

[Abstract] This paper presents a low power regulator design for RFID application using 65nm CMOS technology. The design consists of two parts: a reference generator with temperature compensation, and a low power LDO regulator. Most of MOSFET transistors in the design operate at subthreshold region for low power dissipation. Simulation results show that the proposed regulator is capable of operating within a wide range of supply voltage (from 1.1V to 2.5V) and temperature (from -30°C to 50°C), with the total quiescent current of as low as 63.8nA at room temperature.

[Abstract] This paper deals with an analytical methodology to synthesize microstrip input and output (I/O) matching networks for class F-1 PAs up to the third harmonic using short stubs. Physical dimensions of the microstrip are determined by means of T-parameters. To verify the proposed method, a GaN class F-1 PA was designed at 2.5 GHz. Experimental results show high correlation with simulated data.

[Abstract] A novel design of an on-chip dual-band Wilkinson power divider (DWPD) working at 24 and 77 GHz (K- and W-band) in 65 nm CMOS technology is presented in this paper. The proposed structure is composed of two on-chip inductors and five capacitors. It has the following advantages: (1) constructing a quasi λ/4 transmission line by LC networks, the divider could operate in two frequency bands; (2) as only two inductors are needed in the design, the chip area is remarkably compact , with a die size of only 200 μm × 450 μm, and (3) the structure is symmetrical. Rigorous analysis and equations are given. With the new method, the miniaturized DWPD demonstrates an excellent performance: S11, S22, S23 and S33 are all suppressed down to -15 dB, and the insertion loss is below -1.5 dB at both frequencies.

Session B4P-K: RF/Analog Design and Modeling

Chair: Sleiman Bou-Sleiman, *Intel Cooperation*
Time: August 6, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] The paper describes a Track and Hold Amplifier (THA) suitable for RF sampling and Software Defined Radio receivers where high speed and high resolution are required. The reported THA is based on two main techniques: one for minimizing the differential droop rate and one for improving the HD3 in track mode. Measurements results show that the adopted solutions are both effective. In the desired input band around 1GHz, at the desired sub-sampling frequency (0.5GS/s) the THA provides a linearity compatible with 12-bit (SFDR). Moreover at the maximum achievable sampling frequency (1.5GS/s) the performances are quite constant and the resolution is compatible with 11-bit (SFDR) up to an input frequency of 1GHz.

[Abstract] This work presents a frequency synthesizer architecture that can be used in cognitive radio applications. It generates carrier frequencies that are distributed into sixteen continuous sub-bands covering the entire supported frequency range. The proposed architecture covers a frequency range between 350 MHz and 6.25 GHz. The new architecture incorporates a voltage controlled oscillator (VCO) realized in 0.13µm CMOS technology with varactors and a switched inductor in order to achieve a simulated tuning range from 4.75 GHz to 6.25 GHz (27.3%) and from 3.25 GHz to 4.25 GHz (26.7%). The loop bandwidth of the phase locked loop (PLL) is 891 KHz whereas the switching time between bands is 5.75 ns. At 5.5 GHz, the simulated synthesizer phase noise is of -111 dBc/Hz at a 1 MHz offset frequency.

[Abstract] This paper presents a reconfigurable receiver model whose purpose is to enable the study of reconfiguration strategies for future energy-aware and adaptive transceivers. This model is based on Figure of Merits of measured circuits. To account for real-life RF interference mechanisms, a link quality estimator is also provided. We show that adapting the receiver performance to the channel conditions can lead to considerable power saving. The models proposed can easily be implemented in a wireless network simulation in order to validate the value of a reconfigurable architecture in real-world deployment scenarios.

[Abstract] We review and analyze the critical features of ultra-short range wireless links. These features will be required for advancing NoC and SoC integration to the next level, as transistor scaling and hetero-integration on silicon substrates are expected to reach their full potential by the end of the decade. Based on published transceiver data, the scalable wireless NoCs for multi-core processors and reconfigurable networks for SoCs are within reach of Si/SiGe BiCMOS technology in the next few technology generations. However, before such THz-band CMOS wireless transceivers can become reality and work efficiently, compact high-gain on-chip antennas, high-density on-chip inductors with magnetic cores, and tunable-gain LNAs/PAs that can lower power consumption will be necessary.

Session B4P-L: Devices and Circuits Techniques

Chair: Malgorzata Chrzanowska-Jeske, *Portland State University*
Time: August 6, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] FinFETs are being adopted as an alternative to nanoscale classical MOSFET for digital circuits. The double-gate (DG) FinFET gives rise to a rich design space using various configurations of the gates. Existing research study the DG FinFET for digital design. However, the effectiveness of the various DG FinFET configurations for the analog design has not received much attention. In this paper, we compare the DG FinFET parameters including transconductance (g_m), output resistance (r_0), open-circuit gain ($g_m \times r_0$), transition frequency (f_T) including the most important issue, "nanoscale variability", which are important for analog design. The following three configurations for a fully depleted SOI DG FinFET are analyzed: shorted-gate, independent-gate, and low-power, for both strong inversion and subthreshold operations. Using the results obtained, we present guidelines for DG FinFET based analog design.

[Abstract] A multiplier is one of the basic building blocks of digital systems. Transistor based implementations, face many limitations due to heat dissipation, high power consumption and current leakage. Quantum-dot Cellular Automata (QCA), an emerging nanotechnology, is a better alternative that soles these problems. However, QCA circuit timing relies on its layout; but this can be solved by utilizing the asynchronous NULL Convention Logic (NCL) design methodology. This paper presents the design f a QCA asynchronous multiplier circuit. Simulations verify the performance of the designed multiplier

[Abstract] Process variations are of great concern in deep sub-micron technology. Early prediction of their effects on the circuit performance and parametric yield is extremely useful. Due to the increase of the design complexity in today's microprocessor, a demand for the high level design has increased. Therefore, in this paper, we propose the timing analysis model so that the impact of process variations is taken into account during high level synthesis.

[Abstract] we present a novel design strategy to reduce the impact of radiation-induced single event transients (SET) on logic circuits. This design style achieves SET mitigation by Strengthening the sensitive node using a likeness to feedback techniques. We have analyzed several techniques from hardening radiation at transistor level to a single event transient in 7nm FinFET devices. Simulation results have shown the proposed method has higher soft error robustness than the existing ones.

[Abstract] A Dual Control Gate Floating Gate Transistor (DCG-FGT) is a new device used in the circuit design. This component is a floating gate transistor. In this paper, we propose a retention study of floating gate charge. We demonstrate experimentally that the floating charge loss over time is very low.

Session B5L-A: Nyquist-Rate Data Converters

Chair: Vishal Saxena, *Boise State University*
Time: August 6, 2013, 16:00 - 17:40
Location: Barbie Tootle

[Abstract] new architecture of the time-to-digital converter(TDC) achieves adjustable sub-ps-level resolution with high linearity in ms-level dynamic range. To achieve sub-ps-level resolution with cyclic time domain successive approximation (CTDSA) within a clock cycle, the propagation delay difference is implemented by digitally controlling both the unit load capacitors and the discharge current of the load capacitance. The proposed CTDSA achieves 610 fs resolution and 5 ns dynamic range. The total simulated power consumption is 63.3 mW with 3 V supply. The design was simulated using a 0.35 µm CMOS process.

[Abstract] This work presents a semi-digital cyclic ADC with time-mode residue voltage generation. In the proposed scheme, the conventional switched-capacitor MDAC is replaced with a time-mode circuit which generates the residue voltage by controlling the charge and discharge interval of a capacitor. As a result, a semi-digital cyclic ADC can be realized using simple circuit components including capacitors, comparators, DC current source, and digital logics. Without the amplifier, the analog blocks can operate under a lower supply voltage that leads to reduced power consumption. Furthermore, a compact ADC can be realized by using small sized capacitors. An 8-bit, 500kS/s cyclic ADC is realized using CMOS 0.35µm technology, where the power consumption is 36.7µW.

Session B5L-B: Digital Circuits

Chair: Nader Rafla, *Boise State University*
Time: August 6, 2013, 16:00 - 17:40
Location: Hayes Cape

[Abstract] Asynchronous paradigms are a way to deal with hard problems in newer technologies. Among the templates for ensuring efficient asynchronous design, Null Convention Logic (NCL) appears as a fast and relatively low area and power option enabling semi-custom design. This work propos-es a new asynchronous logic template, NCL+, which is a mod-ification of NCL to support the return-to-one protocol. A basic library of NCL+ standard-cells, with different driving strengths enables comparison between NCL and NCL+. While no significant differences in area arise, results suggest that a trade-off of power versus forward propagation delay exists. Accordingly, NCL+ provides more power efficiency and NCL provides smaller forward propagation delays.

[Abstract] Power Supply Networks (PSN) are susceptible to electromigration failure and increased resistance due to high on-chip temperatures and large power supply currents. Joule heating, which leads to increased localized interconnect temperatures and higher resistivity in the PSN interconnect, exacerbates this reliability problem and is only expected to worsen in future technologies. The best method of reducing interconnect Joule heating is by reducing the RMS current within the interconnect. Consequently, we propose a gradient-based decoupling capacitance placement method to reduce the magnitude of the current spikes in the interconnect. Our experiments show that our propose approach can reduce interconnect temperatures by 12.5 K which results in a 4.7% decrease in resistivity and an increase of 66.3% in electromigration lifetime.

[Abstract] Many signal processing systems, particularly in the multimedia and telecommunication domains, are synthesized to execute data-intensive applications: their cost related aspects " namely power consumption, performance, and chip area " are heavily influenced, if not dominated, by the data transfer and storage aspects. In such applications, hierarchical memory organizations reduce energy consumption by exploiting the non-uniformity of memory accesses and assigning the frequently accessed data to low levels of the hierarchy. Moreover, within a given level, power can be reduced by memory partitioning " whose principle is to divide the address space in several smaller blocks, and to map these blocks to physical memory banks. This paper addresses the problem of energy-aware banking of on-chip memories for data-intensive applications, proposing a technique that is guided by the intensity of memory accesses within the array space of signals.

[Abstract] A CAM-based Information Detection Hardware System for fast exact pattern matching is implemented on hardware system with FPGA and ASIC. The system has simple structure, does not employ any Central Processor Unit (CPU) as well as complicated computations. We take advantages of Content Addressable Memory (CAM) which has an ability of parallel multi-match mode for designing the system. The system is applied for fast pattern matching with various required search patterns without using search principles. In this paper, the authors present the system for exact pattern matching on 2-D data.

[Abstract] The paper discusses the use of extensible processing platforms for the design of high-performance systems which combine fast parallel operations over data streams in programmable logic and problem-specific software running in advanced RISC machine. The streams contain information that needs to be analyzed and filtered. The main idea is to digitalize frequently changed data from numerous sensors and to represent each data item in form of a binary vector. It is shown that many analysis and filtering problems can be solved through Hamming weight counting for the vectors and comparison of the results with pre-given bounds (thresholds). The proposed architecture takes advantages from fixed plus variable computations and implements novel methods. The results of experiments and evaluations of the architecture in two Zynq-based prototyping boards are also presented.

Session B5L-C: Special Session: High-Precision and High-Speed Data Converters II

Chair: Samuel Palermo, *Texas A&M University*
Time: August 6, 2013, 16:00 - 17:40
Location: Cartoon Room I

[Abstract] Time-interleaving several identical A/D converters enhances the overall conversion speed in a power-economical way. However, mismatches between individual channels in such schemes degrade the overall dynamic range of the converter. Several algorithms to mitigate such effects are discussed with special emphasis on an adaptive signal-conditioning algorithm. The algorithm is further extended towards a hardware-friendly implementation using interpolation filters. Behavioral simulations corroborating the same are presented.

[Abstract] Continuous-time delta sigma (CT-\Delta\Sigma) ADCs are gaining wider adoption in data conversion systems primarily aided by their robustness to mismatch in nano-scale CMOS technologies and inherent anti-alias filtering. In past, several techniques have been employed to achieve wider conversion bandwidths by either scaling the designs to a lower technology node or by adopting architectures with lower oversampling ratios (OSR). Cascaded, or MASH, CT-\Delta\Sigma ADCs have been explored to achieve conversion bandwidths by cascading lower order \Delta\Sigma loops followed by a digital coarse quantization noise canceling filter (NCF). Another technique which has recently been explored is to increase the quantizer sampling rate, in a given technology node, by absorbing excess loop-delay (ELD) greater than one clock cycle (T_{s}) in the loop. As a step towards combing the two techniques, we propose a systematic design method to synthesize 3-2 MASH CT-\Delta\Sigma modulators to achieve higher conversion bandwidths, BW\geq40MHz in a 130-nm CMOS technology.

[Abstract] This paper presents the study of ADC resolution and bandwidth requirement tradeoffs for high-speed data communications. The results indicate that increasing the sampling frequency slightly by 20% to 40% above the symbol-rate frequency can lead to a lower ADC resolution requirement. This can potentially reduce the ADC power consumption greatly and improve the overall system power efficiency.

[Abstract] We present a study of accuracy and timing limitations in current-steering digital-to-analog converters (DACs). Effects of limited output impedance and device mismatches on the DAC performance are discussed and observed for a 10-bit DAC operating at 4GS/s. These limitations are also studied across process technology.

Session B5L-D: Special Session: RF-FPGA Circuits and Systems for Enhancing Access to Radio Spectrum (CAS-EARS)

Chair: Arjuna Madanayake, *University of Akron & University of Calgary*
Co-Chair: Vijay Devabhaktuni, *University of Toledo*
Time: August 6, 2013, 16:00 - 17:40
Location: Cartoon Room II

[Abstract] We propose a technique with clear guidelines to design a compact planar ultra-wideband (UWB) Wilkinson power divider (WPD) for enhanced-access to the radio spectrum (EARS) applications. The design procedure is accomplished by replacing the uniform transmission lines in each arm of the conventional power divider with varying-impedance profiles governed by a truncated Fourier series. While such non-uniform transmission lines (NTLs) are obtained through the even mode analysis, three isolation resistors are optimized in the odd mode circuit to achieve proper isolation and output ports matching over the frequency range of interest. An equal split WPD is designed, simulated, and measured.

[Abstract] Cognitive radio has emerged as an effective method for relieving the current problem of spectral crowding. One primary challenge in the field of cognitive radio design is the realization of highly frequency agile RF building blocks. This paper presents a new technique for realizing a multi-band low noise amplifier, reviews methods for realizing wide-band power amplifiers, and a new method for extending the tuning range of the voltage controlled oscillator. In addition, this paper presents a nonlinear analysis of concurrent multi-band mixers which will aid in future cognitive radio frequency planning.

[Abstract] This paper presents the design of a broadband, 1.6-3 GHz, 10W class-J power amplifier (PA). Analytical expressions of theoretical current and voltage waveforms as well as the fundamental and second harmonic impedance derivations are provided. Taking into account the extrinsic parasitic elements and the nonlinear drain-source capacitance of the packaged RF power transistor, an external output matching network is designed to provide the proper impedances on the design space to the transistor current source plane. Source-pulling of the transistor led to the design a broadband input matching network. The designed amplifier exhibits greater than 60% efficiency and almost 40 dBm output power over 1.4 GHz frequency bandwidth.

[Abstract] Recently, several researchers have discovered the need for radios to use description techniques for the objects in the wireless realm. The concept of RF field-programmable analog array (FPAA) was also proposed recently and the lack of hardware abstractions was identified as a problem. We propose a hardware abstraction for RF FPAAs, which enables an open RF-digital interface. We advance the concept of wireless thin clients. These clients are connected to the cloud using the open RF-digital interface. We describe the architecture of a comprehensive wireless ontology.

[Abstract] This paper gives a review of the recent progress made in realizing highly-tunable high-Q evanescent-mode tunable filters for reconfigurable radio front-end. Several practical considerations, such as power handling, noise and vibration perturbations are subsequently considered. A novel design that uses planar tuning elements, such as surface mount solid-state varactors, is also introduced. These high performance tunable RF components are expected to make a significant impact on the development of reconfigurable RF systems.

Session B5L-E: Analog and RF Circuit Techniques

Chair: Valencia Koomson, *Tufts University*
Time: August 6, 2013, 16:00 - 17:40
Location: Suzanne M. Scharer

[Abstract] Low phase noise oscillators are critical to signal recognition and separation in poor reception conditions. Typically the choice is between a large, high performance hybrid oscillator or a lower performance integrated solution. It is possible to use integrated circuit components to construct a high performance oscillator, but only with great attention to detail. Every IC component has to be optimized in parallel to balance the constraints of spiral inductors, metal-insulatormetal (MIM) capacitors, somewhat lossy varactors, and active devices with breakdown limitations. Physical implementation is critical; some locations are insensitive to trace resistance, other areas are sensitive to even tiedown placement. This paper is intended to discuss, and demonstrate the last mile of integrated circuit VCO design for robust systems, which is less discussed, but maybe just as important as innovative circuit approaches.

[Abstract] A new high speed, and low power ADC architecture and its circuit implementation is introduced in this paper. Proposed ADC takes the advantage of low power characteristic of SAR ADCs and combines it with high speed operation of pipeline ADCs to realize a high throughput energy efficient ADC. By unrolling the feedback loop of SAR ADC and delaying the analog signal the binary search algorithm is implemented in pipeline mode. The analog delay is implemented using time interleaved sampling scheme. Since no residue amplifier is required in the proposed ADC, significant high speed yet low power operation can be achieved simultaneously. A 6-bit, 1.5- GS/s ADC is designed based on this concept in a 65nm CMOS process. Simulations confirm that the proposed ADC achieves an SNDR of 35.63dB, ENOB of 5.63, and FoM of 78fJ/conv-step for a Nyquist rate input frequency while consuming 5.8mW from a single 1.2V power supply.

[Abstract] In this paper, we describe an operational current-to-frequency converter that has a large open-loop conversion, which is meant for use in negative feedback circuit-configurations akin to operational amplifier circuits. The feedback network dominates the closed-loop transfer characteristics in this configuration. This provides ability to trade gain for improving linearity and reducing process, voltage and temperature variations. The idea here is to provide a building block to configure ADCs with different resolutions over a wide range of sampling rates below 1 GHz. We present the architecture of such a device and its achievable performance via simulations using the models of a typical 65nm process technology.

[Abstract] An analysis and design method for a 10-GHz ring voltage-controlled oscillator (VCO) are proposed. By using a detailed small-signal equivalent circuit model, the delay of the current mode logic buffer circuit and the minimum limit of the number of those used in the VCO are evaluated. We set the transconductance generator in a MOSFET model as a function of drain current and obtained the current dependence of the oscillation frequency of the VCO. To confirm the validity of the design method, we compared the measured and estimated oscillation frequency of the VCO fabricated with the 65-nm MOSFET process. The agreement between the measurements and calculations is good enough, confirming the validity of the method.

[Abstract] This preliminary study reviews important features of the injection locked Synchronous Oscillator (SO), which is a multifunctional network to synchronize, track, and amplify a reference signal. The SO can reduce the phase noise and the acquisition time of the system. The Coherent Phase-Locked Synchronous Oscillator (CPSO) is then presented and analyzed as a modified phase-locked loop (PLL) where the voltage controlled oscillator (VCO) in a conventional PLL is replaced by a voltage controlled SO (VSO) for wireless applications. The CPSO not only retains all the properties of the SO, but also gives the coherency as to provide zero phase shift across the frequency locking range. To demonstrate the feasibility of CPSO, phase plane trajectories are plotted to analyze the phase behavior of the system. The behavior of the system with respect to phase noise reduction has also been analyzed.

Session B5L-F: Memristors, DG-MOSFETS and Graphine FETs

Chair: Reyad El-Khazali, *Khalifa University*
Time: August 6, 2013, 16:00 - 17:40
Location: Rosa M. Ailabouni

[Abstract] The use of memristors as nanoscale programmable resistors allows the realization of compact tunable analog components such as tunable gain amplifiers. However, since the memristor's resistance depends on the signal through it, the design of such tunable memristor-based components should account for this memristor resistance change. In this paper, we analyze the effect of the memristor resistance change on the gain of the differential pair amplifier and demonstrate its dependence on the amplifier parameters and the signal frequency.

[Abstract] This paper proposes a two-level framework for memristor based mixed-signal design exploration. First, a Verilog-A memristor model is proposed which is not source-type dependent and has advantages over existing SPICE memristor models. It includes the threshold-type behavior and nonlinear dynamics while retaining memristor parameters that are useful for circuit design. Second, a POlynomial Metamodel integrated Verilog-AMS (Verilog-AMS-POM) is proposed to enable fast circuit-accurate system-level design space exploration of such circuits. The metamodeling technique is proposed to assist their design, modeling, and higher-level integration. A memristor based programmable Schmitt trigger oscillator is presented as a case study. Polynomial metamodels are created to facilitate the analysis and verification of the programmable oscillator. The coefficients of determination of the proposed metamodels demonstrate excellent fidelity. Verilog-AMS-POM simulation achieves over 30,000X speedup compared to SPICE simulations.

[Abstract] In this paper, we propose the use of Double Gate MOSFET (DG-MOSFET) in the design of Charge Pump Phase Frequency Detectors (PFD)s in 32 nm and 45 nm DG MOSFET technologies. The DG-MOSFETs are used to design the universal NOR gate which is the only building block for the PFD. The DG-MOSFET NOR gate consists of half the transistor count compared to NOR gate designed in conventional CMOS. Thus 2 transistors make up the DG-MOSFET 2-input NOR gate as opposed to 4 needed in conventional CMOS. This reduction in transistor count makes the PFD area efficient. The reduced transistor count also lowers the parasitic capacitances which enhances speed. Here, we have demonstrated that for tiny phase errors of 60 ps and 80 ps the rise time of the output of a DG-MOSFET based PFD reaches the desired threshold of logic 'HIGH' required to initiate the charge pump switches that follows the PFD, whereas it fails for conventional CMOS, in 32 nm and 45 nm technologies respectively. The DG-MOSFET thus finds application as a better alternative to conventional CMOS for dead zone avoidance in Phase Locked Loops.

[Abstract] In this work, we present a novel structure of Graphene NanoRibbon Field-Effect Transistor (GNR FET) to reduce short channel effects. In this structure, two side metal gates with lower work-function than the main gate are used in a conventional double-gate (DG) GNR FET topology to provide virtual extensions to source/drain regions while these are biased constant, independent of the main gate. The proposed GNRFET structure improves drain-induced barrier lowering (DIBL), which can reduce the short-channel effects (SCE) in device performance such as on/off current ratio, off-state current and subthreshold slope to make it a more suitable configuration than the normal GNR FET for digital integrated circuit design.

[Abstract] Semiconductor nanoparticles are getting significant attention due to their diverse applications in optoelectronics, photovoltaics, photonics, transparent electronics and other nanoelectronic devices. Zinc Oxide (ZnO) is one of the promising nanoparticles with a unique set of material, physical, optical, electrical and thermal properties. This paper investigates diverse potential applications and unique properties of ZnO nanoparticles. The analysis reveals that ZnO can be easily used as an n-type heavily doped oxide semiconductor and its bandgap is wide enough for various applications. We have performed a set of analysis to study the electronic, optical, thermal and material properties of ZnO to understand its behavior at nanoscale dimension and its potential roles in different devices.

Session C1P-G: Design and Analysis of Communications and Wireless Systems

Chair: Sami Muhaidat, *Khalifa University of Science, Technology & Research*
Time: August 7, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] In this paper, we investigate the channel estimation algorithm for medium-voltage, long haul power line communication (PLC) system in the IEEE 1901 standard. To improve the overall performance, we employ a dual Gaussian interpolation method working on the amplitude and phase domain simultaneously, a major difference from the conventional schemes using the real and imaginary part. Meanwhile, to mitigate the effect of impulsive noise, a notorious impairment in PLC transmission, we propose an impulsiveness detection/cancellation method using unused null subcarriers. Extensive simulation results indicate improved performance than the conventional inter-polators in an impulsive environment. The channel models proposed by the open power-line communication European research alliance (OPERA) are utilized for simulation. The hardware architecture is also presented together with its achievable performance.

[Abstract] This paper describes an FM-UWB transceiver system which employs M-PSK modulated subcarriers for high throughput data transmission. Compared to conventional 2-FSK FM-UWB transceivers, the proposed M-PSK FM-UWB transceiver can increase data rate with minimal increment of RF front-end complexity. A regenerative FM demodulator followed by a low-frequency M-PSK demodulator enables low-power low-cost receiver design with enhanced energy efficiency. Simulation results show that the 8-PSK 3.5-4GHz FM-UWB transceiver system successfully modulates and demodulates 8-PSK data, achieving three time the energy efficiency of the conventional FM-UWB system.

[Abstract] One of the most prominent challenges in Wireless Sensor Network (WSN) is target localization. As majority of the decisions made in navigation and path planning are dependent on current information available, target localization is one of the fundamental requirements. This paper presents accuracy studies on target localization using the Time Difference of Arrival (TDOA) method. Some of the fundamental advantages in the presented method are its simplicity through requiring only four reference nodes, tolerating errors in node positioning and time differences. Simulations results show that proposed TDOA method outperforms the centroid TDOA method in different test environments, with an average localization error of 2.36 m.

[Abstract] Neurodegenerative diseases in our ageing population in recent time have been a deep concern for the medical practitioners. Neurodegeneration is the cause of progressive loss of structure or function of neurons, including neural death. Many neurodegenerative diseases including Parkinson's, Alzheimer's, and Huntington's occur as a result of neurodegenerative processes. Human gait impairment is one of the indicators of the progression of neurodegenerative diseases. We propose to use a noninvasive technique to wirelessly monitor patients suffering from neural disorders. Our system using Received Signal Strength Indicator (RSSI) can be deployed in the patient's residence and can be used for the early detection of gait impairment that may be a precursor to other neural diseases.

[Abstract] This paper proposes a bit-wise matrix-vector multiplication in the optimization of a proposed low density parity check (LDPC) encoder. Investigation of this proposed architecture is done by implementing five code lengths using one IEEE 802.16e standard code rate. It is shown that the proposed architecture outperforms other works in terms of information throughput ranging from 0.23 to 8 times higher. In term of ratio of throughput per area, the proposed method exceeds other works in the range of 1 to 6.5 times higher.

Session C1P-H: Bio-Systems

Chair: Khaled Salama, *KAUST*
Time: August 7, 2013, 9:00 – 10:10
Location: Great Hall Meeting Room

[Abstract] A simplified expression for the current-excited step response of the Cole impedance model which significantly reduces the numerical complexity required to extract the impedance parameters using a nonlinear least squares fitting is presented. MATLAB simulations show reductions in extraction times up to 47.5%, without reducing extraction accuracy and are verified experimentally on an ideal Cole-model and fruits used as the Cole impedances showing less than 2% relative error between simulated responses (using the extracted impedance parameters) and the experimental results over the entire dataset.

[Abstract] An inductive link using an on-chip stacked square receiver coil is presented. An SOS (silicon on sapphire) process is employed to enhance the biocompatibility and to ensure the maximum power transfer. The capacitor used to build the LC tank for the receiver coil is also integrated on chip. With a carrier frequency of approximately 13MHz, the power module was able to reach 21% power transfer efficiency. With no requirement for external capacitors, this finding has shown the potential of fully integrated components with ultra-small size in the application of energy transfer in the field of biomedical implants.

[Abstract] This paper presents two highly efficient charge pump designs, one positive and one negative, used in a distributed bio-implant with completely integrated capacitors. The system is designed using silicon-on-sapphire (SOS) technology CMOS transistors to triple the voltage swing available at the chip-scale implant. The high power efficiency and high voltage conversion ratio of the system is obtained by selectively controlling the transistor switches in the current path to reduce the reverse current flow. The proposed charge pump design achieves a power efficiency of 83.3% and voltage conversion ratio of 0.95 for a 3 V, 2 MHz input signal and load of 2.5 mA.

Session C1P-J: Sensors for Biological Applications

Chair: Khaled Salama, *KAUST*
Time: August 7, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] The striatum is believed to be the main input station of the basal ganglia. No biophysical network model existed in NEURON of a dorsal lateral striatal medium spiny neuron (MSN) that included NMDA and AMPA receptors. A model of the striatum that includes these receptors simulating in-vivo electrophysiological behavior is presented. A single compartment MSN (scMSN) model was created by enhancing an existing single compartment striatal output neuron model with NMDA and AMPA receptor models. The models concentration ratio and respective activation and deactivation time constants were fit to existing electrophysiological data. The entire scMSN model was validated against pre-existing whole neuron experimental data generated by direct current injection into the soma and excitation resulting from cortical stimulation. The developed biophysical simulation allows for simulated neurotransmitter input and produces accurate action potential output.

[Abstract] This research introduces a new type of chemical-biological sensor platform. This sensor platform detects different types of chemical or biological agents without the use of probes, wires, active components, or a battery. An interrogator transmits power through radio frequency waves to the embedded device. The embedded device sends back a portion of the power through radio frequency waves with altered amplitude and phase. The characteristics of the received signal contain the information about the agent of interest. The sensor device has a functionalized surface which aids in selectivity to the analyte of interest.

[Abstract] The occurrence of charge imbalance during the electrical stimulation of neurons can potentially corrode electrodes and damage cells. In this paper, we introduce a circuit solution suitable for measuring stimulation imbalances when voltage swings over three or more times the maximum voltage supply for the technology (3.3V). The proposed topology uses a current mirror connected in series to the stimulator to charge sampling capacitors, isolating the readout input from the high voltage stimulator output. The circuit was designed for Silanna Silicon-on-Sapphire 0.5um/FC process. Simulation results indicates that the technique is suitable for detecting imbalances <100nA for a milliampere stimulation current.

[Abstract] The paper presents a microcontroller based, real-time breath sampling system capable of selectively sampling over multiple breath cycles, only the deep alveolar air that is known to contain the Volatile Organic Compounds (VOC) of clinical/diagnostic interest.

[Abstract] A lower power consumption temperature sensor that operates on low power supply voltage with power supply voltage insensitive improvement is presented in this paper. Compare to conventional four-transistor temperature sensor, which has the power supply voltage sensitive problem, the linearity error of the proposed structure is reduced under the power supply variation. The proposed temperature sensor is designed in TSMC 90nm 1P9M process and the normal power supply voltage is 1V. The simulation results show the linearity error of the proposed circuit is 0.29°C under normal power supply voltage 1V with low power consumption 29μW under. The linearity errors are 0.99°C and 2.8°C under the 10% variation of power supply voltage.

Session C1P-K: Digital Signal Processing Techniques I

Chair: Hari Reddy, *California State Long Beach*
Time: August 7, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] This paper proposes an efficient method for continuous adaptive feedback cancellation (AFC) in digital hearing aids. The AFC is achieved by two filters: an adaptive filter to model and track variations in the acoustic feedback path, and a piecewise-fixed filter for feedback neutralization. The proposed method employs a delay-based technique where an appropriate delay is inserted in the signal flow path and an extended-length filter is used for the AFC. An efficient strategy is proposed to check when the AFC filter reaches the optimal solution. Furthermore, the proposed strategy can detect when there is a strong perturbation in the acoustic path, and hence AFC filter is reinitialized. The computer simulations are carried out to demonstrate the effectiveness of the proposed method. We observe that, as compared with the conventional method, the proposed method gives robust performance even in the case of a strong perturbation in the acoustic path.

[Abstract] When speed considerations are critical, FFT-based implementations of cyclic convolution need to be considered. FFT-based implementations of purely integer cyclic convolution can be affected by floating point round-off errors potentially leading to an incorrect integer result. To alleviate this problem we are proposing the use of our sectioned algorithm, which is suitable for parallel-recursive, as well as serial-recursive implementations. Because of the shorter subsections length, the round-off errors are not as severe as when doing a direct full-length implementation. The attainment of the exact integer results was confirmed using C++, MATLAB and the FFTW to perform the shorter cyclic sub-convolutions.

[Abstract] Digital mobile systems must function with low power, small size and weight, and low cost. High-performance desktop microprocessors, with built-in floating point hardware, are not suitable in these cases. For embedded systems, it can be advantageous to implement these calculations with fixed point arithmetic instead. We present an automated fixed-point data path synthesis tool FpSynt for designing embedded applications in fixed-point domain with sufficient accuracy for most applications.

[Abstract] Based on fast convolution algorithm, this paper proposes improved parallel FIR filter structures for linear-phase FIR filters where the number of taps is a multiple of parallelism. The proposed parallel FIR structures not only use fast convolution algorithm to reduce the number of subfilter, but also exploit the symmetric (or antisymmetric) coefficients of linear-phase FIR filter to reduce half the number of multiplications in subfilter section at the expense of additional adders in preprocessing and postprocessing blocks

[Abstract] A design approach is presented for 2-D digital filters possessing approximate quadrantal magnitude symmetry without the constraint of the denominator having only 1-D separable factors. To ensure the BIBO stability of the filter, the planar least square inverse stabilization approach is employed. It is illustrated through design examples that the proposed approach results in filters with sharper transition band and lower error relative to the given filter specifications. Also, for certain cases, it is shown that a lower order non-separable denominator design can achieve the same result as a higher order separable denominator design, thus providing savings in the number of multipliers. Finally, 2-D VLSI realizations without global broadcast are presented for the optimized transfer function with non-separable denominator factors and approximate quadrantal symmetry.

Session C1P-L: Digital Signal Processing Techniques II

Chair: Genevieve Sapijaszko, *Devry University*
Time: August 7, 2013, 9:00 - 10:10
Location: Great Hall Meeting Room

[Abstract] This paper presents a conflict-free ROM addressing scheme for generating the TF tables. Basically, the conventional (N/2)-words ROM table for the Radix-2 Memory-Based FFT (MBFFT) processor with single process element (PE) is equally partitioned into 2p sub-tables allowing all 2p PEs to simultaneously access the twiddle factors without causing any conflict. This study presents the use of MBFFT processor with 4 parallel PEs. Result show that the proposed scheme can reduce the chip area of DVB-T2 applications by 18.85%. The hardware reduction is of significance.

[Abstract] Radio-frequency (RF) two-dimensional (2-D) infinite impulse response (IIR) space-time planewave frequency-planar beam digital filters have potential applications in ultra-wideband (UWB) directional filtering of propagating electromagnetic far-field plane-waves. Such plane-wave filters achieve highly directional digital RF beamforming for aperture array applications. The phase response of emerging 2-D beam filters which are designed using the concept of frequency planar resonant network prototypes is studied in this paper. The high frequency phase non-linearities are quantified and compensated using a real-time FFT based multirate phase rotator architecture.

[Abstract] A simple and efficient method to design multiplierless two-stage comb-based decimation filters is presented. The proposed scheme takes advantage of the Chebyshev sharpening, recently introduced in literature, to obtain higher selectivity in comparison to traditional comb filters. The resulting filter has better magnitude response characteristics and fewer Additions Per Output Sample (APOS) with respect to other two-stage comb-based filters available in literature.

[Abstract] A Digital Down Converter (DDC) using four times intermediate frequency sampling is analyzed to simplify the required hardware. The DDC is controlled by a two bit counter. One bit controls the mixer, implemented as a two input multiplexer. The other counter bit controls data flow in direct and transposed form finite impulse response (FIR) filters. The resulting FIR filters significantly reduce the number of multipliers and adders required while still allowing additional filter reduction techniques to be applied.

[Abstract] Recently the Quadratic Modified Fermat Number Transform (QMFNT) was extended to the Modified Discrete Fourier Transform (MDFT) to enable overlap-add FFT block processing to be implemented without zero padding. The MDFT was then extended into two dimensions and published results described how the 2-D extension manages two-dimensional wrap around effects. This paper investigates how the modularity of these transforms can be used to achieve fault tolerant designs that strive to achieve minimal hardware redundancy. Fault tolerant designs are presented for both the MNT and the MDFT and the resulting efficiencies of the two designs are analyzed and compared.

Session C2L-A: Phase Locked Loops

Chair: Chung-Chih Hung, *National Chiao Tung University*
Time: August 7, 2013, 10:10 - 11:50
Location: Barbie Tootle

[Abstract] Adding Voltage controlled Oscillators (VCOs) in parallel is equivalent to making transistors larger, in the sense that they consume more power but noise is lowered. This work looks at the task of adding VCOs together for on-the-fly data rate switching for use in a Phase-Locked Loop (PLL) architecture and clock and Data Recovery (CDR) systems. The purpose of this is to be able to reduce power at the expense of higher jitter if lower data rates are required, and respond to changing requirements quickly and reconfigure to receive higher rate data by reducing jitter and raising power.

[Abstract] A new technique to achieve high jitter tolerance and fast frequency acquisition with low logic latency for MIPI Low Latency Interface (MIPI LLI) applications is proposed. The proposed tracked oversampling CDR increases the allowable phase difference between the recovered and embedded reference clock up to 1.25 UI. The CDR loop gain can be adjusted based on the digitally estimated phase difference, resulting in short acquisition time (≤ 1 baud period) and high jitter tolerance (167-UIp-p 100-kHz jitter). Utilizing a bit selector with an edge tracking finite state machine (FSM) instead of an elastic FIFO, the logic latency less than 2 baud periods is achieved. The core circuit is implemented using a 65nm CMOS technology. It consumes 4.7mW from a 1.2V power supply at 5.8Gb/s.

[Abstract] An architecture that compensates the sensitivity to process variation of the phase noise performance of a ring voltage-controlled oscillator (VCO) is presented. The architecture consists of a VCO subdivided into 10, individually activated sub-VCOs whose outputs are connected together through pass-transistor switches. By varying the number of active sub-VCOs, per-die tuning of phase-noise and power dissipation is enabled. Monte-Carlo simulations in ST 90nm CMOS show a 36 % reduction in the worst case and 41 % reduction in the average power dissipation of a design required to satisfy the same phase noise specification. Measured results show that phase noise can be traded-off against power dissipation on a per-die basis. The technique is also applicable to multi-rate wireline systems in which different data rates require different jitter specifications.

[Abstract] This paper presents a frequency synthesizer system with random pulsewidth matching technique and a sub-sampling charge pump. Through the randomization and average of the pulsewidth and the reduction of current mismatch, the frequency synthesizer can reduce the ripples on the control voltage of the voltage-controlled oscillator in order to reduce the reference spur at the output of the phase-locked loop. A random clock generator is used to perform a random selection control. To demonstrate the effectiveness of the proposed spur-reduction techniques, a 2.5 GHz to 2.7 GHz FLPLL was designed and fabricated using a TSMC 90-nm CMOS process. The proposed circuit can achieve a phase noise of"114 dBc/Hz at an offset frequency of 1 MHz and reference spurs below"74 dBc.

Session C2L-B: Computer Arithmetic and Cryptography

Chair: George Purdy, *University of Cincinnati*
Time: August 7, 2013, 10:10 - 11:50
Location: Hayes Cape

[Abstract] This work contributes to the modular multiplication operation C=A*B mod M, the basis of many public-key cryptosystems including RSA and Elliptic Curve Cryptography (ECC). We use the Residue Number System (RNS) to speed up long wordlength modular multiplication. The RNS leads to a highly parallel algorithm which we exploit with a massively parallel hardware implementation capable of exceptionally low latency. This paper presents architecture for this scheme consisting of a scalable array of identical processing elements.

[Abstract] A circuit is vulnerable if a Trojan state appears, a verification process is needed to ensure the circuit is robust over temperature and process. Circuit-level continuation methods finding all DC operating points are summarized in this work. The discussion of where to apply continuation methods in the circuit and the minimum requirement of simulation step in a circuit will be shown

[Abstract] DNA computing is an attractive alternative to traditional computing technologies due to DNA's large storage capacity, massive parallelism, and energy efficiency for computation. Massive parallelism, in particular, makes DNA attractive for cryptographic applications. However, since DNA computing is based on bio-molecular reactions, it is not error free. A main source of errors is false hybridizations between unintended sequences. An efficient way to minimize these errors is to design error-resistant DNA sequences. We have used simulated annealing to generate error-resistant DNA sequences. Our simulations show that the sequences generated by this approach are superior to sequences generated by other techniques previously reported in the literature.

[Abstract] A Newton-Raphson algorithm based, an efficient, accurate and reconfigurable kth-root root design and verification system is introduced. The design and verification system generates Verilog HDL design code and required control signals for application-specific operations. The design can be used for multi-purpose arithmetic operations based on an assigned k value, such as division for k=1, square root for k=2, cube root for k=3 and so on. The generated hardware can be used as a standalone design or can be implemented into a larger system by using a hand shake signal. This could make this design and verification tool suitable for new or ongoing projects. This tool generates Verilog RTL code and its testbench that can be implemented in FPGAs and VLSI systems. The proposed design tool can increase productivity by reducing design and verification time. Several case studies have been implemented on Xilinx Virtex-5 FPGAs. The designed system uses MATLAB-based verification and reporting for fast and accurate design evaluation.

[Abstract] Forth is a flexible language used in embedded systems. In this paper we present a novel soft core that executes native Forth, including floating-point operations, and uses branch prediction for fast execution. The core is designed to be a replacement of an embedded controller running Forth in a VM. The branch prediction architecture was created specifically for literal, call-returns, and jump instructions, which occur most frequently in Forth. Our benchmarks show that these improvements are significant to speeding up overall execution time.

Session C2L-C: Special Session: Reversible Computing

Chair: Himanshu Thapliyal, *University of South Florida*
Time: August 7, 2013, 10:10 - 11:50
Location: Cartoon Room I

[Abstract] LLogic gates rendered in digital circuit diagrams refer both to abstract logical transformations of Boolean variables and to the physical structures and processes that realize these transformations. The logical and physical aspects are related in a manner that has implications for energy efficient computing; Landauer's Principle (LP) imposes efficiency limits on gates that irreversibly discard information but imposes no such limits on gates that do not. In this paper, we explore the logical-physical link and its dissipative consequences from a fundamental perspective. We provide a systematic characterization of this link, and use the resulting framework to clarify necessary conditions for physically reversible operation of logically reversible and logically irreversible gates in circuit environments.

[Abstract] While reversible logic increasingly finds useful application as an emerging technology for various areas, the design of corresponding circuit structures still is in its infancy. Most of the existing approaches for synthesis or optimization are applicable for relatively small functions only. Hardware description languages enable to overcome this limitation. Combined with hierarchical synthesis schemes, they enable the specification and realization of complex logic as a reversible circuit. On the other side, the resulting synthesis schemes lead to further challenges, e.g. a significant increase in the number of additional circuit signals. In this paper, we provide an overview on the design of reversible circuits through the hardware description language SyReC. This includes a summary of the recently made accomplishments as well as a discussion of challenges still to be addressed.

[Abstract] Conservative reversible logic gate is a reversible logic gate that is reversible in nature and also satisfy the property that there are equal number of 1s in the outputs as in the inputs. In this work, we present a new class of nxn (n inputs and n outputs) conservative reversible logic gate named SCRL (Super Conservative Reversible Logic) gate for the design of reversible quantum circuits. The proposed SCRL gate has 1 control input depending on the value of which it can swap any two n -1 data inputs, hence is superior to the existing Fredkin gate. In reversible circuits, the constant input bits that are used to realize different logic functions are referred to as ancilla inputs, while the outputs that are neither primary inputs nor contribute to any useful computations are referred to as garbage outputs. As Ancilla inputs and garbage outputs are overhead bits in a reversible circuit, they need to be minimized. Barrel shifter forms an integral component of many computing systems. As an example of using the proposed SCRL gate to design efficient reversible quantum circuits, the design of reversible barrel shifter with zero ancilla inputs and zero garbage outputs is illustrated.

[Abstract] Heat generation limits the performance of computing systems, ultimately dictated by the thermodynamic necessity to expel energy into the environment proportionally to information loss in the computing process. We develop models to track the irreversible bit erasures in standard binary adders, presenting a methodology to estimate the bounds for components on various levels of design abstraction. The approach can be used to quantify the logical reversibility of a design and direct the optimization efforts for higher degree of energy conservation.

[Abstract] Recently reversible circuit testing has become an important issue for researchers. In the process of design, synthesis or template matching, failures can happen due to erroneous replacements or incorrect cascading of gates. In this paper, we present testing such errors modeled as gate and wire replacement faults, which can also handle most frequently addressed errors like missing gate and control points appearance or disappearance. Here, we propose three testing schemes based on Boolean Satisfiability (SAT) formulation and compare their efficiencies. In particular, we present the design of a Reversible Test Miter, which, along with backtracking, can easily detect such faults. We show that a smaller test set can be derived from the reversible test miter, increasing fault coverage and speed of testing.

Session C2L-D: Special Session: Self-Healing and Self-Adaptive Circuits and Systems

Chair: Abhilash Goyal, *Oracle*
Time: August 7, 2013, 10:10 - 11:50
Location: Cartoon Room II

[Abstract] New 2-channel Time-Interleaved ADC mismatch identification & correction algorithm using I/Q signal processing. Performance verified on actual TI-ADC hardware.

[Abstract] Increasing run-time failure rates in nanoscale memory has emerged as a major design challenge. The problem is more severe in case of low-voltage low-power memory due to reduced design margin. Application of Error Correction Code (ECC) is a well-known approach to tolerate run-time failures in memory. Traditionally, a uniform worst-case protection using ECC is used for all blocks in a large memory array. However, with both spatial and temporal shift in intrinsic reliability of a memory block, such uniform protection can be unattractive in terms of either ECC overhead or protection level or both. We propose a novel reconfigurable ECC approach, which can adapt, in space and time, to varying reliability of memory blocks by using an ECC that can provide the right amount of protection for each block at a given time. It tracks the reliability of the block with respect to read/write/access/hold failures and provides adaptive protection at optimal overhead. We show that such an approach is extremely effective for nanoscale lowvoltage memory in diverse application domains.

[Abstract] Frequency division duplex (FDD) transceivers employing the direct-conversion radio architecture are known to suffer from transmitter-receiver signal leakage problems. The presence of such leakage signal can impose stringent linearity requirements in receiver components that are difficult to fulfill in practice. Good example is second-order intermodulation distortion (IM2) due to transmitter leakage signal, stemming from finite IIP2 of receiver mixers, falling directly on top of the weak received signal. This paper carries out detailed modeling and proposes a dynamic cancellation technique for such TX-RX leakage, enabling sufficient TX-RX isolation in FDD mode without any extra analog/RF filtering. The technique is based on creating a replica of the undesired transmitter leakage signal and subtracting it from the down-converted signal in the receiver path, taking also the essential transmitter nonidealities into account. Simulation results show that the proposed method is able to effectively push transmitter leakage induced IM2 below the receiver noise floor.

[Abstract] We propose post-manufacture testing and tuning algorithms for MIMO systems assembled from devices across diverse process corners. These algorithms allow such systems to operate across the widest range of channel conditions as possible while minimizing power consumption (performance maximization also maximizes manufacturing yield). To further save power consumption in the field, real-time tuning algorithms are proposed that dynamically trade off available performance slack in MIMO designs, across the relevant signal modulation and MIMO modes to save power consumption.

[Abstract] A drain-switching charge pump (CP) design is presented with near perfect current matching and extended flat current response over a range of process, voltage, and temperature variations. Current mismatch is compensated dynamically without the need for a replica charge pump or extended digitally-assisted calibration routines. The selfregulated circuit uses several simple yet effective feedback mechanisms to overcome the basic shortcomings of nanometer devices and reduced power supplies. The circuit is designed in 90nm CMOS and simulated extensively using Monte Carlo analysis while sweeping the operating temperature to provide statistically relevant operating conditions. The proposed design achieves near perfect current matching at output voltages between 0.16V and 0.98V for temperatures ranging from -30 to 90 degrees Celsius and a power supply between 1.08V and 1.32V.

Session C2L-E: Digital Signal Processing-Media and Control

Chair: Wasfy Mikhael, *University of Central Florida*
Co-Chair: Steven Bibyk, *Ohio State University*
Time: August 7, 2013, 10:10 - 11:50
Location: Suzanne M. Scharer

[Abstract] Spatial domain facial recognition Modular IMage Principal Component Analysis (MIMPCA) has an improved recognition rate compared to the conventional PCA. In the MPCA, face images are divided into smaller sub-images and the PCA approach is applied to each of these sub-images. In this work, the Transform Domain implementation of MPCA is presented. The facial image has two representations. The Two Dimensional MPCA (TD " 2D " MPCA) and the Diagonal matrix MPCA (TD " Dia " MPCA). The sub-images are processed using both non-overlapping and overlapping windows. All the test results, for noise free and noisy images, using ORL, Yale and FERET databases achieved; 99.5%, 99.58% and 97.42% recognition accuracy respectively. Transform Domain implementations yield, computational and storage savings of at least 42% and 99.92%, respectively, compared to spatial domain. Sample results are given.

[Abstract] Automation is common in many industries. Some tasks, such as object measurement, can easily be automated. The equipment required to perform automated measurements may be cost prohibitive and may prevent widespread deployment in automated point of sale kiosks or product inspection applications. This paper focuses on the development of an optical measurement device that is inexpensive relative to existing systems. The device consists of an image sensor, a microcontroller, and several laser line projectors. The hardware design and configuration of the device is discussed along with the algorithms used to process the captured images and perform the measurement tasks. The conclusion includes a discussion of the performance of the optical measurement device.

[Abstract] Face and hand gesture recognition is one of the most challenging topics in computer vision. In this paper, a novel algorithm presenting a new 2D representation of histogram of oriented gradients is proposed, where each bin represents a range of angles dealt with in a separate layer employing 2DPCA. This method maintains the spatial relation between pixels which enhance the recognition accuracy. In addition it can be applied on either face or hand gesture images. Experimental results confirm excellent properties of the proposed algorithm and promotes it for real time applications

[Abstract] This paper presents an original speaker recognition system that utilizes a quantized spectral covariance matrix on the input to a two-dimensional Principal Component Analysis (2DPCA) function. Eigenvoice algorithm is used as a classifying tool and is generated by the features of a group of speakers. The proposed system is selective in acquiring acoustic parameters and leads to a significant decrease in storage requirements. The system is robust in a noisy environment with recognition rates as high as 92% at 0dB SNR. Concatenated vowels that make up the speech signal are extracted from the TIMIT database and the noise environment is acquired from the NOIZEOUS database.

[Abstract] This paper presents the design and implementation of an embedded digital control system for a novel acoustophoretic separation technique. Our goal is to design, build, and test a high-frequency, high-power, and high-efficiency ultrasound driver for an acoustophoretic separator The device needs to be able to efficiently transfer electrical energy into acoustical energy with minimum losses and be able to drive the low impedance of a typical piezo-electric transducer. The proposed new platform technology provides an innovative solution that consists of a large volume flow rate acoustophoretic phase separator based on ultrasonic standing waves with the benefit of having no consumables, no generated waste, and a low cost of energy. The technology is efficient at removal of particles of greatly varying sizes, including separation of micron and sub-micron sized particles. The proposed embedded digital control system (drive system) utilizes a TMS320F28335 digital signal processor / controller chip [2] at its core.

Session C2L-F: Advances in Communications and Wireless Systems

Chair: Sami Muhaidat, *Khalifa University of Science, Technology & Research*
Time: August 7, 2013, 10:10 - 11:50
Location: Rosa M. Ailabouni

[Abstract] This paper presents a novel algorithm for residual phase estimation in wireless OFDM systems, including the carrier frequency offset (CFO) and the sampling frequency offset (SFO). The subcarriers are partitioned into several regions which exhibit pairwise correlations. The phase increment between successive OFDM blocks is exploited which can be estimated by two estimators with different computational loads. Numerical results of estimation variance are presented. Simulations indicate performance improvement of the proposed technique over several conventional schemes in a multipath channel.

[Abstract] A new broadcast format is presented for the atomic-clock time-code signal broadcast by the National Institute of Standards of Technology (NIST) from station WWVB in Fort Collins, Colorado. The new broadcast format, based on BPSK modulation that is added to the existing amplitude-modulation (AM), offers many new features and provides several orders of magnitude of improvement in reception robustness, without impacting existing AM receivers that are based on envelope-detection. Additionally, a digital receiver architecture, amenable to integration in a CMOS system-on-chip (SoC), is proposed, which relies on digital signal processing, thereby eliminating the need for the crystal filter and other passive components found in existing receives.

[Abstract] SAW-less FDD receivers have become the state-of-the-art architecture in multiband receivers. They eliminate the SAW filter between the low-noise amplifier and the direct-conversion mixer. Large TX leakage signals hit the mixer which imposes challenging linearity requirements. Second order intercept point (IIP2) was intensively studied in 3G receivers. In this paper, we derive the IIP2 specification for LTE receivers and report the simulated and measured correction factors needed to estimate the modulated carrier 2nd order distortion using the conventional 2-tone test.

[Abstract] In this paper, we propose a synthesizable LDPC decoder IP core for the WiMAX system with high parallelism and enhanced error-correcting performance. The proposed fully-parallel layered decoder architecture can fully support multi-mode decoding specified in WiMAX with 12~24 clock cycles for processing one iteration. By applying the 3-state processing schedule, it achieves twice parallelism with minor circuit area increase compared to state-of-the-art work, thus results in 46.8% improvement in power efficiency.

[Abstract] The random demodulator architecture is a compressive sensing based receiver that allows the reconstruction of frequency-sparse signals from measurements acquired at a rate below the signal's Nyquist rate. This in turn results in tremendous power savings in receivers because of the direct correlation between the power consumption of analog-to-digital converters (ADCs) in communication receivers and the sampling rate at which these ADCs operate. In this thesis, we propose design techniques for a robust and efficient random demodulator. The resetting mechanism can pose challenges in practical settings that can degrade the performance of the random demodulator. We propose practical approaches to mitigate the effect of resetting and propose resetting schemes that provide robust performance.

Session C3L-A: SAR Analog-to-Digital Converters

Chair: Vishal Saxena, *Boise State University*
Time: August 7, 2013, 13:10 - 14:50
Location: Barbie Tootle

[Abstract] This paper presents a low-power 10-bit 64MS/s successive approximation register (SAR) analog-to-digital converter (ADC) for Built-In Self Test (BIST) that uses a monotonic capacitor switching and variable clock period method for single input condition. To achieve high speed, a non-fixed clock time technique is used to reduce not only peak current but also die area. The technique removes conversion time waste and extends the SAR operation speed over 64MHz easily. Compared to the converters that use the conventional procedure, maximum peak current and DAC driver's area are reduced by about 33.8% and 25.2%, respectively. Single input ADC generally limits the resolution unlike the differential input ADC. However, the proposed ADC in this paper achieves high resolution and accuracy with a single input signal. The prototype was designed using 0.13 um single poly 6 metal standard CMOS technology. Using 1.2V supply and the sampling rate of 64 MS/s, the ADC achieves a SNDR of 50.2 dB and consumes 1.325 mW. The ADC core occupies an active area of only 185u m X210u m.

[Abstract] This paper presents a new radix-3 successive approximation register (SAR) analog-to-digital converter (ADC). Our proposed radix-3 SAR ADC can generate 1.6N binary bits during N comparison cycles. The radix-3 SAR ADC is 60% faster than the conventional radix-2 SAR ADC. Our prototypes are implemented with 4 and 7 ternary bits using 180nm CMOS technology. They can achieve a signal-to-quantization-noise ratio(SQNR) of 39 dB and 66 dB which are equivalent to 6.2 and 10.7 binary bits respectively.

[Abstract] This paper presents a new energy efficient supply boosted (SB) successive approximation register (SAR) type analog-to-digital converter (ADC) designed in a high-Vth CMOS process. Supply boosting technique (SBT) improves input common mode range and minimum operation voltage of mixed- signal circuits even when threshold voltages are in the order of the supply voltage. A 10-bit SB- SAR ADC was designed and fabricated in a standard 0.5 µm, 5V, 2P3M, CMOS process in which threshold voltages of NMOS and PMOS devices are +0.8V and -0.9V, respectively. Fabricated SB-SAR ADC achieves effective number of bits (ENOB) of 8.24, power consumption of 6µW from a 1.2Volt supply. Measured figure of merit (FoM) was 163fJ and 196fJ per conversion-step for sampling rates of 80KS/s and 100KS/s, respectively.

[Abstract] This paper presents a 12-bit 50-MS/s successive-approximation (SAR) analog-to digital (ADC) with high power efficiency. By splitting MSB capacitors an efficient step switching scheme is proposed to reduce average switching energy of the capacitive DAC by 93.75% as compared to conventional method. The settling time is partially optimized in half of the conversion steps. Prototype is designed in a 65-nm CMOS technology and the power consumption is 2.0mW under a 1.2-V power supply.

Session C3L-B: Real Time Systems

Chair: Abhilash Goyal, *Oracle*
Time: August 7, 2013, 13:10 - 14:50
Location: Hayes Cape

[Abstract] A bird and bat monitoring system has been developed that uses marine radar, IR camera and acoustic recorders for wind farm applications. IR video recording is used to monitor birds and bats activity which will be useful for wildlife biologists in developing mitigation techniques to minimize impact of wind turbines on birds and bats. In order to process nocturnal migration data that is recorded from one hour after sun set to one hour before the sun rise requires high speed computations. IR video processing is computationally intensive. A parallel processing approach and use of GPU is proposed to process IR video data that will meet real time requirements. This paper examines the parallel implementation of the IR video processing on GPU. We achieved the real time requirements and the necessary performance for analyzing IR with size 704x480.

[Abstract] This paper describes a dedicated architecture for real-time imaging using the Total Focusing Method (TFM) and an advanced acquisition technique called the Full Matrix Capture (FMC). The architecture was entirely described using VHDL language and implemented on a V5FX70T Xilinx FPGA for the control part and a V5SX95T Xilinx FPGA for the acquisition part. The architecture is able to perform real-time FMC-TFM imaging at a maximum frame rate of 73 frames/s and a maximum resolution of 128x128 pixels, which is sufficient as a performance for a real-time imaging with a good characterization of defects in the non destructive evaluation context.

[Abstract] Light Detection and Ranging (LiDAR) sensors are used for acquiring high density topographical data with extremely high spatial resolution. Many LiDAR-based applications, e.g. unmanned autonomous ground and air vehicles require real-time processing capabilities for navigation. The processing of the massive LiDAR data is time consuming due to the magnitude of the data produced and also due to the computationally iterative nature of the algorithms. Graphics Processing Units (GPU) consist of massively parallel cores, have high memory bandwidth and are being widely used as specialized hardware accelerators. A GPU-based parallel LiDAR processing algorithm is implemented with GPU specific memory architecture optimizations. The GPU implementation in this study significantly reduces the processing time of the LiDAR data as compared to CPU-based implementation.

[Abstract] A design for a portable and accurate wireless electroencephalograph system is proposed. Using digital signal processing techniques, the neuronal function of the brain can be acquired and processed into meaningful representations of brain activity. The system described utilizes circuits and systems which can be connected to wirelessly transmit digitized brainwaves via Bluetooth for an end application. In this way, the system is portable, and modular in terms of the device to which it can interface. This design serves as a platform for applications using Brain Computer Interface, which has become a popular extension of EEG systems in modern research.

[Abstract] We present an architecture of microsystem designed for blind source separation that directly interfaces the four microphone miniature array. The proposed architecture implements the source separation algorithm in a unique framework that combines wavefront sensing, subband signal processing and independent component analysis. The spatial gradients are computed in continuous-time domain, with the 16-channel subband signal decomposition of the three spatial gradient signals. In each band, we perform linear static independent component analysis, initialized by the fullband signal solution. We demonstrate that with the proposed system architecture the additional 4dB in the separation performance can be achieved.

Session C3L-C: Image Processing and Interpretation

Chair: Annajirao Garimella,, *Intel Inc.*
Time: August 7, 2013, 13:10 - 14:50
Location: Cartoon Room I

[Abstract] In this paper, we propose a low-pass filtering process aiming at removing noise and artifacts generated by histogram equalization, while preserving the image signal variations. The filtering is made to provide different levels of smoothing strength by means of cascading stages of simple low-pass filters. A weak smoothing given by the first stage is applied to all the pixels, including those in edge regions, and the pixels located in the flattest regions are processed successively by all the filtering stages to get the strongest smoothing. A binary mask is used in each stage, except the first one, in order to shield pixels in non-homogeneous regions from over-smoothing. Simple algorithms are developed to generate the masks from the input image. The results of the simulation demonstrated that the proposed filtering leads to a good quality of the contrast enhancement in varieties of images and requires a low computation complexity.

[Abstract] Face recognition in deity images is a challenging problem. Most of the existing face recognition methods are very sensitive to pose and illumination changes. This paper proposes a new technique for deity face recognition which is suitable for pose and illumination changes. The proposed approach uses Schur decomposition to speedup PCA computations and doubly modified hausdorff distance for measuring similarity between different face edge maps. In addition, this paper introduces a new dataset named as Indian DEity dataSet (IDES) for face recognition which contains a collection of face images of Indian Deities. Performances of the proposed method for deity face recognition are experimented with IDES dataset.

[Abstract] In this paper, a novel line segmentation algorithm is proposed as an extension to our previous works, i.e., line detection using multilayer [1] and generalized [2] Fourier methods. First, a multilayer Fourier-based Radon transform (RT-MLFRFT) is applied to detect the location and the orientation of the straight lines. Afterwards, a set of windows-of-interest in spatial domain is designed to decompose the complex Radon space to a number of Radon spaces with a single transparent butterfly. This is to eliminate the effect of the neighbour RT peaks and guarantee the correct segment detection. Experimental results shows that the proposed method enjoys superior performance compared with existing similar representative works.

[Abstract] A facial recognition technique employing Subimages Histogram Intensity (NHI) is presented in this paper. The algorithm has attractive properties with respect to storage requirements and computational complexity in both the training and testing modes, which make the technique particularly suitable for large data bases. The new algorithm is applied to ORL, Yale and FERET data bases. The experimental results confirm the significant reduction in the storage and computational requirements compared with recently reported techniques, without sacrificing the recognition accuracy.

[Abstract] The Hough Transform (HT) is one of the most widely used feature extraction techniques in real-time applications, like lane departure warning, surveillance etc. Most existing HT implementations are serial in nature, resulting in high computation time. Recently, we proposed the Additive Hough Transform (AHT), which achieves angle and block level parallelism in HT computation. In this paper, we evaluate the performance gains offered by AHT in both serial and parallel configurations by implementing it on different computing platforms such as multicore processors, GPUs and FPGAs. It is shown that AHT offers significant performance gains over existing implementations of the HT in both serial and parallel configurations on a wide range of embedded platforms.

Session C3L-D: Special Session: Verification and Trusted Mixed Signal Electronics Development

Chair: Greg Creech, *Ohio State University*
Co-Chair: Steven Bibyk, *Ohio State University*
Time: August 7, 2013, 13:10 - 14:50
Location: Cartoon Room II

[Abstract] This paper proposes an improved ASIC design flow for the automotive ASIC development. Using a FPGA based hardware prototype verification step, the improved design flow enables the test of entire design in a running automotive module with different operating conditions, helps to find out issues before the tape out. The proposed design flow can largely increase the confidence level in the tape out, decrease the development time, reduce the risk of multiple re-spin cycles, and lead to a better cost efficiency in the automotive ASIC development.

[Abstract] As electronic systems evolve and become exceedingly more complex, their development is often the result of multiple development teams working separately. This introduces the threat that during design and integration processes, Integrated Circuits (ICs) are susceptible to the insertion of malicious attack functionality by enemies. To address these challenges, ECI has developed EDAptive® Syscape™, which can be utilized to model design flows as well as store results produced at different stages of development and verification, thereby providing protection against insider threat.

[Abstract] The Large Hadron Collider at CERN is presently in a two year shutdown for upgrades. Among the upgrades include insertion of a new detector in the ATLAS experiment called the Diamond Beam Monitor. Included in the DBM is a radiation hard application specific integrated circuit, the Hitbus chip platform, to allow the DBM to trigger its own readout. Intellectual property (IP) from several collaborating institutes were gathered and combined with new custom blocks to create the platform. We present the design, verification, performance, experiences from the collaborative process, and results from an irradiation with 24 GeV protons to 115 Mrad.

[Abstract] Trusted design and verification presents new challenges for the case of using Intellectual Property (IP) in mixed signal systems. A Digitally Controlled Oscillator (DCO) subcomponent of a Phase-Locked Loop (PLL) is utilized as an example through which the presented verification principles may be applied to PLL tests on the Texas Instruments Analog System Lab Kit Pro (TI ASLK Pro). A VHDL model has also been developed, incorporating Assertion-Based Verification (ABV) as a means for trusted verification of the design.

Session C3L-E: Digital Signal Processing I

Chair: Ying Liu, *University of Central Florida*
Time: August 7, 2013, 13:10 - 14:50
Location: Suzanne M. Scharer

[Abstract] This paper presents the initial results of analysis of nonlinear spectral features for detecting deception in speech. These features are derived from spectral energy on a Bark scale either directly or using the psychoacoustic masking property of human speech perception. Truthful and deceptive speech utterances are established a posteriori by a male speaker under jeopardy. Test results using a neural network with (a) bands of spectral energy, and (b) perceptually significant bands of energy, both at Bark bands, as input features show the viability of the two feature sets in distinguishing between truthful and deceptive speech.

[Abstract] This paper presents novel no recursive comb structure with a very small pass band droop, where the decimation factor is power of two. The simple multiplierless compensator which works at low rate compensates for the passband droop. The compensation filter remains the same for all values of the decimation factors and the number of the cascaded comb filters K. Last p stages of the nonrecursive structure have six cascaded filters for all values of M and K. The first folding band has an improved attenuation. The other folding bands are either improved or equal to those of the original comb, which depends on the value of p. Method is illustrated with examples and the comparison with one recently proposed method, is also provided.

[Abstract] A denoising method using computational auditory scene analysis (CASA) for a wearable stethoscope is proposed in this paper. The denoising method imitates human ears to analyze the ambient auditory scene so that it can separate the heart sound signal from unwanted ambient noise. Simulation results show that the method greatly improves the signal noise ratio of the heart sound signal after denoising.

[Abstract] This paper proposes an entropy based audio watermarking scheme using singular value decomposition (SVD) and log-polar transformation (LPT) for copyright protection of audio data. In our proposed scheme, initially the original audio is segmented into non-overlapping frames and discrete cosine transformation (DCT) is applied to each frame. Watermark information is embedded into LPT components of the largest singular value obtained from DCT sub band with highest entropy value of each frame by quantization. Simulation results demonstrate the robustness of the hidden watermark for different attacks. The comparison analysis shows that the proposed method has superior performance than the state-of-the-art watermarking methods reported recently.

Session C3L-F: Wireless Systems I

Chair: Sami Muhaidat, *Khalifa University of Science, Technology & Research*
Time: August 7, 2013, 13:10 - 14:50
Location: Rosa M. Ailabouni

[Abstract] In this paper, we propose a brand new communication concept, called as "vision communication" based on LED array and image sensor. This system consists of LED array as a transmitter and digital device which include image sensor such as CCD and CMOS as receiver. In order to transmit data, the proposed communication scheme simultaneously uses the digital image processing and optical wireless communication scheme. Therefore, the cognitive communication scheme is possible with the help of recognition techniques used in vision system. By using LED array as transmitter, the increase of data rate is possible similar to MIMO skills used in traditional wireless communications. In addition, image sensor makes it possible to spatially separate the optical noises such as sun light and ambient lights in communication environment. Through experiment based on practical test bed system, we confirm the validity of the proposed vision communications based on LED array and image sensor.

[Abstract] With intentional compressed amplifier operation to achieve higher energy efficiencies, it is constructive to revisit the concept of amplifier gain because when an amplifier operates in compression the output signal is no longer directly proportional to the input signal. Two approaches to the concept of gain, slope-gain and ratiometric gain, are examined in this nonlinear regime. These measures are shown to match at small signal levels and diverge as amplifier compression increases. Slope-gain characteristics relate directly to output waveform distortion, and hence to amplifier linearizer design. Gain measured by power differenced in dB, widely used in RF engineering standard practice, is shown to be a ratiometric measure and not directly applicable to linearizer design.

[Abstract] This paper presents a study on the outage performance analysis of basic receive diversity combining schemes in terms of outage probability and average outage duration over Nakagami-0.5 fading channels. Recent attention has been given to Nakagami-0.5 fading channel as a special case of Nakakgami-m fading channel with m = 0.5 and as a worst-case (severe) fading scenario. Closed-form expressions for outage probability and average outage duration are derived for selection combining (SC), equal gain combining (EGC) and maximal-ratio combining (MRC) diversity schemes. The expressions derived are numerically evaluated to study the effect of diversity order and multipath intensity profile (MIP) on the system performance.

Session C4P-G: Hardware/Software Co-Design

Chair: Abhilash Goyal, *Oracle*
Time: August 7, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] A new algorithm to accelerate the execution of floating point division for the final quotient is presented in this paper. In this algorithm, the quotient of each step is predicted and then the final quotient is achieved by accumulating all the predicted quotients. If the prediction is correct, the number of iterations can be reduced and thus the speed increases. Generally, about 5 iterations are needed to reach a final quotient, but the number of this iteration could be bigger or smaller depending on the accuracy of the prediction, the capacity of the accumulated quotient, the comparison with the result register, the number of fractions and the required remainder set by users. In addition, the proposed method only takes up 0.4% to 6% area on a Field-Programmable-Gate-Arrays (FPGA) chip which is quite small. The study also shows that if there are more values in Look-Up-Table (LUT), the final quotient can be found faster with only fewer iterations. By extending more bits for quotient (the bit width of original quotient is 5-bits), we accelerated the procedure to achieve the final quotient and the needed number of additions is significantly reduced.

[Abstract] Hardware and Software co-design has become one of the main methodologies in modern embedded systems. The partitioning step, i.e. to decide which components of the system should be implemented in hardware and which ones in software, is the most important step in the embedded systems. Since the costs and delays of the final design strongly depend on partitioning results, there is a need to get an accurate estimate for hardware area, delay and power. However, accurate delay estimation methods are slow as they need a scheduling step. In this paper, we propose a reliable delay estimation method to be used within the partitioning step prior to the scheduling step.

[Abstract] Function profiling is crucial for optimized embedded software which needs to have resource constraint, low level power consumption and real-time ability. In this work, we provide a fast and reliable solution by utilizing an instruction set simulator named QEMU and creating an analyzer tool. We developed a tracing module inside the simulator to trace execution information of software in run-time and log to the log file. Our implementation takes advantages of the dynamic binary translation of QEMU to keep its speed fast. After that, the analyzer tool analyzes the log file and creates a function profile. We implemented this methodology for ARM architecture, and evaluated many kinds of embedded applications.

[Abstract] Blömmer, Otto, and Seifert presented a fault attack on elliptic curve scalar multiplication called the Sign Change Attack, which causes a fault that changes the sign of the accumulation point. As the use of a sign bit for an extended integer is highly unlikely, this appears to be a highly selective manipulation of the key stream. Here we describe two plausible fault attacks on a smart card implementation of elliptic curve cryptography.

Session C4P-H: System Architectures and Hardware/Software Co-Design

Chair: Abhilash Goyal, *Oracle*
Time: August 7, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] Foggy image enhancement is an important branch of digital image processing, which significantly benefits traffic and outdoor visual systems. To overcome the shortcomings of the existing foggy image enhancement algorithms, we have developed a method that combines Principal Component Analysis (PCA), Multi-Scale Retinex (MSR) and Global Histogram Equalization (GHE). Initially, a PCA transform is applied to the foggy image to split the input image into a luminance and two chrominance components. In the second step, the luminance and the chrominance components are individually enhanced by MSR and GHE, respectively. In the final stage, an inverse PCA is applied to combine the results of the three channels into a new RGB image. Experimental results show that the proposed method can effectively be used to remove the image degradation captured in foggy weather and enhance the sharpness of the image.

[Abstract] Ultrasonic signal processing applications require huge amounts of data to be processed. Further, high computational performance is essential to meet the real-time requirements. Compression of the signal helps to reduce the data size and storage requirements as well as allow for rapid transmission of data to remote locations. High signal fidelity is significant in many of practical applications like ultrasound medical imaging and nondestructive testing. In this study, we discuss two methods for ultrasonic signal compression which offer high signal fidelity " Discrete Wavelet Transform and signal decimation with the Nyquist rate limit. The compression algorithm is implemented on a reconfigurable system-on-chip platform using programmable hardware logic as well as in software using an embedded processor. The implementation details and the performance of the compression algorithms on both the hardware and software are analyzed in this paper.

[Abstract] A universal software defined wireless platform and a specific method for its application is proposed here to perform field test measurements for performance evaluation of communications system. The platform implements every application, starting from the transmitter and receiver of wireless link, the virtual measurement instruments for the baseband signals and the performance evaluation algorithm, purely in software which solution offers high level of flexibility, and it provides an easy and cheap solution for performance testing. Since a PXI-based HW platform is also included in the solution proposed here, every physical RF analog signals generated or processed in software can be recovered. Both the analog RF output and input of the transceiver are available, therefore real field tests can be performed, even more, the performance of a communications system can be evaluated in a real operating network. In this paper the performance of FM-DCSK wireless communications system, operated in the 2.4-GHz ISM band, is evaluated based on real field tests using PXI platform. A systematic method for validation of system implemented on the PXI HW is provided.

[Abstract] This study introduces a mobile ultrasonic signal processing system using an Android smartphone for remote ultrasonic testing and imaging applications. The smartphone receives the ultrasonic data using the Bluetooth connection from a data acquisition and communication unit (DACU). We developed two computational intense signal processing algorithms which are processed by the Android smartphone to explore the smartphone computing capabilities for ultrasonic testing applications. In particular, Split Spectrum Processing (SSP) and Chirplet Signal Decomposition (CSD) algorithms are considered for benchmarking and signal analysis. The analyzed data is displayed in real-time on the screen and streamed to a central location via Wi-Fi or cellular data networks for storage and further data analysis.

[Abstract] This paper describes the design of a custom robotic system that will be used for clinical evaluation of upper-limb motor performance. The system consists of a mechatronic component that is central to capturing of motor inputs, and a software component that constitutes various user interface applications. The focus of this paper is to elaborate the design of the mechatronic component and how it integrates with other elements of the system.

Session C4P-J: Image Processing I

Chair: Genevieve Sapijaszko, *Devry University*
Time: August 7, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] This paper presents a unique camera-based Forward Collision Warning (FCW) and Lane Departure Warning (LDW) systems to improve the safety of road vehicle transportation. The video used in the algorithm is captured by an in-car camera. Initially, a Support Vector Machine (SVM) classifier is applied to the first frame of the video to locate the moving vehicle of interest in front of the host vehicle. Following this step, two separate warning systems, namely FCW and LDW are designed. For the FCW, the Time to Collision (TTC) is determined through the scale change method, and the FCW system will be activated when TTC is less than a predefined threshold value. For the LDW system, the lane position information is analyzed and the warning is triggered if there is a lane departure without the use of blinkers. The proposed camera based system can provide advantages over the traditional radar/laser based warning systems, in which both the LDW and the FCW information cannot be provided with the same system. Furthermore, the proposed system provides additional flexibility at a lower cost.

[Abstract] In this paper a new approach to lane marker detection problem is introduced as a significant complement for a semi/fully autonomous driver assistance system. The method incorporates advance line detection using multilayer fractional Fourier transform (MLFRFT) and the-state-of-art advance lane detector (ALD). Experimental results have shown a considerable reduction in computational complexity while increasing the detection accuracy.

[Abstract] In this paper, a novel image fusion algorithm based primarily on an improved multi-scale coefficient decomposition framework is proposed. The proposed framework uses a combination of non-subsampled contourlet and wavelet transforms for the initial multi-scale decompositions. The decomposed multi-scale coefficients are then fused twice using various local activity measures. Experimental results show that the proposed approach performs better or in par with the existing state-of-the art image fusion algorithms in terms of quantitative and qualitative results. In addition, the proposed image fusion algorithm can produce high quality fused images even with computationally inexpensive two-scale decomposition.

[Abstract] High Efficiency Video Coding (HEVC) is the currently developing video coding standard by the MPEG and ITU organizations. Unlike previous video codec standards, HEVC employs variable block size integer DCT/IDCT to conduct spatial redundancy compression. In this paper, a novel 2-D IDCT VLSI architecture for HEVC standard is presented. Using adaptive block size scheduling scheme, the proposed architecture supports variable block size IDCT from 4×4 to 32×32 pixels with low hardware overhead while keeping the highest performance. Using TSMC 65nm 1P9M technology, the synthesis result shows that the 2-D architecture achieves the maximum work frequency at 400MHz and the hardware cost is about 112.5K Gates. Experimental results show that the proposed architecture is able to deal with real-time adaptive HEVC IDCT of 4K×2K (4096×2048)@30fps video sequence at 179.4MHz. In consequence, it offers a cost-effective solution for the future UHD applications.

[Abstract] Presently, there is an undeniable need for novel transform coding techniques promising improved reconstruction and reduced computational complexity in the field of image and data compression. Discrete Tchebichef transform (DTT), though possessing valuable properties like energy compaction, is a potentially unexploited polynomial-based orthogonal transform, compared to the much popular Discrete Cosine transform (DCT). Specifically, integer DCT is widely used in the field of video compression in view of its ease of computation and acceptable performance. However, specific features of the image, such as the structure and content, profoundly influence the quality of the reconstructed image after decompression. This paper focuses on identifying areas where integer DTT might be an alternative to integer DCT for image compression. An integer-transform for the fast computation of 8×8 DTT that reduces the computational complexity significantly is proposed. The image compression performance of integer DTT and integer DCT are evaluated and compared.

Session C4P-K: Image Processing II

Chair: Genevieve Sapijaszko, *Devry University*
Time: August 7, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] We report on the JPEG tolerance of proposed digital watermarking that uses the morphological wavelet transform based on max-plus algebra. We investigated the image quality and tolerance against graphical data compression attack of an image during the digital-watermarking contest. As a result, the embedded data could be completely extracted. The PSNR was 54.66 dB. Additional graphical data compression was done to reduce the file size to 1/20 or less of the original picture image and the error rate was reduced to 0%, and the PSNR was 54.35 dB. The processing time was confirmed to be about 148.6 times faster than that of conventional algorithms.

[Abstract] This paper proposes an analytical design method for 2D zero-phase recursive filters with a circularly-symmetric frequency response. The design is based on a maximally-flat low-pass prototype filter, whose transfer function is transformed using a specific 1D to 2D frequency mapping. An efficient pre-warping is applied before using the bilinear transform, which allows to obtain filters having a central frequency close to the frequency plane margins, and still with an accurate circular shape, without any distortions. Finally the general filter matrices are obtained. The filter is adjustable in the sense that its bandwidth is specified by a parameter which appears explicitly in the filter coefficients.

[Abstract] Fingerprint image quality heavily influences the recognition rate for fingerprint identification/verification systems. A low-quality fingerprint image may consists of broken ridges, scars, smears, falsely conglutinated ridges, poor ridge and valley contrast, etc. In this paper, we propose a novel and effective three-stage scheme to enhance low-quality fingerprint images. The first-stage enhancement is performed by an oriented linear anisotropic diffusion filter with a local ridge orientation estimation that differs from traditional estimation method. The second-stage enhancement is obtained by an oriented local ridge compensation filter, followed by the third-stage enhancement with a novel angular filter. We compare the proposed method with two existing methods. The results show that the proposed method can improve the quality of the fingerprint images with a lower computational cost.

[Abstract] A novel algorithm for human activity recognition is presented in this paper. This approach is based on a new 2D representation for the Histogram of Oriented Optical Flow (2DHOOF) describing the motion of the actor's contour, where one multi-layer 2D-histogram per video sequence is constructed. Each histogram layer consists of 2D bins (layers) that represent different range of angles. Applying our 2DHOOF features descriptors on the actor's contour reduces the storage requirement and the computation complexity since a sparse optical flow is calculated instead of dense optical flow.

Session C4P-L: Design and Analysis of Control Systems, Mechatronics, and Robotics

Chair: Moataz AbdelWahab, *Nile University*
Co-Chair: Hari Reddy, *California State Long Beach*
Time: August 7, 2013, 14:50 - 16:00
Location: Great Hall Meeting Room

[Abstract] In this paper we present a comparison of two methods to control the reading frequency of a First In First Out (FIFO) memory. The first method is based on the monitoring of its filling level and the other uses the synthesis of the writing frequency to generate and control the reading frequency. These control systems are used in data communication protocol justification architecture for tributary signal demapping.

[Abstract] In this paper, a technique for designing a Ball and Beam System controller based on a nonlinear backstepping design is presented. A control law is developed, and asymptotic stability based on a Lyapunov stability criterion is satisfied. The goal is to design a controller for the ball position with the least overall energy consumption and minimum overshoot. In order to illustrate the efficiency of the proposed control strategy, the simulations are demonstrated and compared with [1]. The results show that the nonlinear backstepping design gives a smoother performance and needs less input magnitude compared to the LQR design. Moreover, the robustness of the proposed design with respect to parameter variations and different reference inputs is examined, and the simulations validated the control scheme.

[Abstract] This paper introduces a technique for choosing a desirable reference temperature profile that is used with an adaptive one step ahead (OSA) and a weighted one step ahead (WOSA) controllers for controlling the indoor air temperature of a building. It also presents the results of a simulation study that compares the performance of the above controllers without and with optimization, and demonstrates better performance for the latter.

Session C5L-A: Wireless Systems II

Chair: Sami Muhaidat, *Khalifa University of Science, Technology & Research*
Time: August 7, 2013, 16:00 - 17:40
Location: Barbie Tootle

[Abstract] Wireless electrocardiogram (ECG) systems are responsible to collect and transmit the vital signals of cardiac patients wirelessly to medical centers for diagnostic and therapeutic purposes. In this paper compressed sensing procedure is applied in ECG signals to provide a robust high-resolution QRS detection algorithm in the hospitals and medical centers with high probability and enough accuracy. Our simulation results for two records of ECG signals show an increment of 10% for sensitivity as well as 12% for the prediction level and good detection accuracy. The proposed algorithm also achieves significantly better detection rate in comparison with Empirical Mode Decomposition (EMD) method.

[Abstract] Opportunistic dynamic access to unused spectrum bands without harmful interference to licensed users can be achieved by several methods. Most of these methods consider static spectrum sensors. Recently,researches focus on mobile spectrum sensors. In this work, we consider the impact of acceleration on the performance of spectrum sensing of a mobile sensor, we found that changing acceleration drastically affect the spatio-temporal diversity results in improving detection performance.

[Abstract] This paper introduces a generalized fully digital hardware implementation of 1-D, 2-D and 3-D multiscroll chaos through sawtooth nonlinearities in a 3rd order ODE with the Euler approximation, wherein low-significance bits pass all NIST SP. 800-22 tests. The low-significance bits show good performance as spreading code for multiple-access DS-CDMA in AWGN and multipath environments, equivalent to Gold codes. This system capitalizes on complex nonlinear dynamics afforded by multiscroll chaos to provide higher security than conventional codes with the same BER performance demonstrated experimentally on a Xilinx Virtex 4 FPGA with logic utilization less than 1.25% and throughput up to 10.92 Gbits/s.

[Abstract] In this paper we propose two new detection schemes for space-time block coded (STBC) systems in flat Rayleigh fading channels under the combined impairments of imperfect channel state information (CSI) and carrier frequency offset (CFO). First, we propose a detector consists of a maximal ratio combiner (MRC) which combines the signal from all the receive antennas to yield maximum signal-to-noise ratio (SNR) along with a maximum likelihood (ML) detector. Then, we design a minimum mean square error (MMSE) detector which optimizes the output in terms of minimum bit error rate (BER). Analysis of the relative performance of the proposed detectors with the conventional methods is done by simulation for different modulation schemes and in the presence of multiple estimation error variances. It is shown that the proposed detectors can outperform the conventional detectors in terms of BER.

Session C5L-B: System Architectures

Chair: Abhilash Goyal, *Oracle*
Time: August 7, 2013, 16:00 - 17:40
Location: Hayes Cape

[Abstract] This paper presents an on-chip partial decoupling architecture with variable nMOS gate capacitance as a PAA countermeasure. The preferred form of the countermeasure consists of a decoupling switch, primary gate capacitor, and a bank of secondary gate capacitors connected randomly. This provides a low overhead and low complexity means of decoupling a sensitive cryptographic module from the power supply. The use of the secondary capacitors serves to mix and hide indirectly leaked information from previous cycles. Test simulations targeting an AES Sbox module were performed using 65 nm technology. Initial results showed that the proposed countermeasure protects against CPA attacks.

[Abstract] Statically scheduled scientific computing problems represent a large set of problems which requires intensive amount of computation. The common feature characteristics of this set of problems could be used to optimize an architecture, where the utilization exceeds 90% of the peak performance. The proposed architecture is an array of reconfigurable NISC (No Instruction Set Computer) processing elements (PE) connected by a reconfigurable NOC (Network On Chip). An optimized data path for a group of problems is suggested. The control of each PE is reconfigurable to customize for each application so as the NOC. The architecture is simulated using a tile of 64 PEs to run LU decomposition algorithm of a dense matrix, and the results show a performance of 177 GFLOPS, which outperforms the GPU NVIDIA 6800 & 7800 implementations and the OpenMP parallel programming multicore solution using an Intel core 2 quad cpu with four processors cores.

[Abstract] A ROM-less direct digital synthesizer architecture is presented in this paper. This architecture eliminates the ROM based phase to sine wave amplitude converter, which is a bottleneck for pushing clock frequencies to gigahertz range. The design consists of a 16-bit phase accumulator, a set of 18 band pass finite impulse response filters, a 12-bit digital to analog converter and a low pass filter to produce a sine wave with frequencies ranging from 36 MHz to 72 MHz with a resolution of 3.05 KHz and a 55dB spur free dynamic range. The same hardware can be used to achieve output frequency ranging from hertz to gigahertz by changing the clock frequency.A resolution of 0.05 Hz can be achieved by using a 32-bit phase accumulator. This design was simulated on Xilinx system generator and mapped on to Virtex-6 FPGA.

[Abstract] Rank modulation is a new data representation method for flash memories that uses the relative orders of memory cell levels. With this innovative approach, flash memory reliability and storage capacity are improved at the same time. Previous rank modulation hardware used winner-take-all circuits for rank determination. A new rank determination strategy is proposed, which is inspired by ramp data converters. The WTA is replaced by current-mode comparators and digital memories. Unlike with data converters, the linearity and absolute values of the conversions do not matter, so long as the relative ranks can be determined reliably.

[Abstract] This paper presents an extensive and careful study of the timing results for a software implementation of the NIST-recommended elliptic curves over prime fields. We have designed and simulated the important field operations and point operations on NIST-recommended elliptic curves over prime fields in C++ based on the MIRACL library for the purpose of optimized speed and efficiency. Specific experiments are conducted to study the data dependency relationship between input parameters (i.e., plaintext to encode) and output results (i.e., encoded message), and we found that the timing output is only contingent on the bit length of the input, regardless of the randomicity (random or fixed) of the input. We believe the work of this paper can provide more accurate and comprehensive information when we compare the performance of a software implementation of NIST prime elliptic curves with the corresponding hardware implementation under different circumstances, such as worst-case scenario or average-case scenario.

Session C5L-C: Image Embedding Compression and Analysis

Chair: Annajirao Garimella, *Intel Inc.*
Time: August 7, 2013, 16:00 - 17:40
Location: Cartoon Room I

[Abstract] This paper presents an strategy for watermarking on color images using a mobile phone. In the proposed scheme a digital watermark is inserted into a color image and can be retrieved after a digital-analog (D/A) and analog-digital (A/D) conversion process. Moreover, the proposed system is able to detect the watermarks after desycronization attacks such as rotation, scaling and translation. For the detection, the Neyman-Pearson criterion is utilized for the selection of a threshold, which consists in minimizing the overall error probability when the watermark is not actually present. Experimentation results show the effectiveness of the proposed approach.

[Abstract] A novel compressive sampling scheme suitable for highly scalable hardware implementations is presented. The prototype design is implemented in a 0.18µm standard CMOS technology and utilizes compressed acquisition to boost the overall power efficiency. Specialized pixels, convenient for Comparator-Based Switched Capacitor readout are developed for this purpose. A custom measurement matrix generation algorithm is implemented which reduces in-pixel hardware complexity and performs measurement matrix generation in a single clock cycle. Column-Parallel Differential Cyclic-ADCs based on the Zero-Crossing Detection (ZCD) technique are used to convert the analog image measurements. Physical IC design issues such as the device noise, mismatch and non-linearity, are analyzed and their effects on compressed image acquisition are discussed. The final simulation results show that the proposed 256×256 pixels architecture consumes 1.45mW at 250fps and 26.2mW at 8000fps. The architecture can easily be scaled towards newer technology nodes and higher image resolutions.

[Abstract] Privacy-protecting technology is essential in this surveillance society. Furthermore, the scale of surveillance systems becomes more diverse. Therefore, scrambling private information in an image can be a solution to simplifying a system. We propose an image-scrambling method for bitmap and JPEG formatted images. Our method enables access control by providing keys to authorized individuals. The image's format is retained. Experimental results suggest that scramble level can be controlled linearly by using parameters. We also developed a demo system for this method and confirm that this method can be applied to embedded systems such as those equipped with surveillance cameras.

[Abstract] The main purpose of steganography is to hide the presence of communication process. Transparency is referred to the ability to avoid suspicion about the existence of a secret message. Several steganographic systems using digital images as host signals have been proposed. However, some of them such as frequency transform-based are computationally expensive. In this paper, a low complexity steganographic system for digital images is proposed. The core of the proposed system is an adaptation of the interpolation-error expansion technique. From experimental results the high perceptual and statistical transparency of the proposed scheme are shown. Moreover, the proposed system embedding rate is similar and some times outperforms the frequency transform-based embedding rate with lower computational complexity.

Session C5L-D: Low Power Datapath Design

Chair: Wasfy Mikhael, *University of Central Florida*
Time: August 7, 2013, 16:00 - 17:40
Location: Cartoon Room II

[Abstract] This paper focuses on improving the performance of non-restoring division by reducing the delay. To improve its performance, two new approaches are proposed here. For the first proposed approach, a novel method to find a quotient bit for every iteration, which hides the total delay of the multiplexer with dual path calculation is presented. Secondly, a new method uses the modified Most Significant Carry (MSC) generator, which determines the sign of each remainder faster than a carry lookahead adder, which reduces the total delay.

[Abstract] A new fused floating-point magnitude unit to compute the square-root of the sum of two squares is proposed. Conventionally, the magnitude computation is executed by discrete serial or parallel floating-point units with conventional floating-point multiplication, squares, addition, and square-root units. The proposed fused floating-point magnitude design has an enhanced exponent unit because the exponent processes of the sum-of-squares and square-root can be merged. Moreover, normalization to make the exponent an even number is not necessary for the fused magnitude unit. Normalization and rounding processing between the squares, addition and square-root computations are eliminated. This paper compares the fused magnitude unit with the conventional discrete floating-point magnitude units. Compared with the discrete parallel magnitude unit with conventional floating-point squarers, an adder, and a square-root unit, the fused floating-point magnitude unit has 24% less area, 24% less latency, and 27% less power consumption (26% less in the pipeline model).

[Abstract] Proposed innovation gives a faster, lower depth, lower power and lower area solution for addition. The paper describes two novel static gates developed for 4-bit Majority Carry Generate (MCG) and Majority Carry Propagate (MCP) operation in a single gate depth. Derivation of a novel 72-bit CL2A within 6 gate-depth, using MCG, MCP and a novel sparse5 (5x2n) algorithm with a variable sparse is described. Implementation of a novel 64-bit CL3A within 5 gate-depth, by extending CL2A with progressive sparse 1+30 + 31 + 32 +…3n algorithm is described. Silicon evaluation of an 8-bit application for the CL2A is presented in 32nm. Post-layout results of 64-bit CL2A and 64-bit CL3A against Ling-Carry-select adder are presented in 14nm along with the advantages and limitations.

[Abstract] In multi-digit parallel decimal multipliers, multiplication can be broadly divided into two major steps: partial product generations (PPGs) and partial product accumulations (PPAs). Although most operands in decimal multipliers are represented in popular 8421 BCD codes, alternative 4221 and 5211 BCD codes are also sometimes employed, alone or mixed with 8421 codes, to represent the partial products, with a hope that by doing so, the multipliers' area/time efficiency will be improved. We propose an 8421-5421 BCD multiplier that is equipped with a simplified precomputation stage for computing the needed multiples of the multiplicand based on 8421-5421 recoding for PPG and an improved 8421 carry-lookahead adder tree for PPA. This 8421-5421 decimal multiplier is compared against two best known multiplier designs using 90nm TSMC technology. The simulation results have confirmed that the proposed 8421-5421 multiplier achieves the lowest delay and is the most time-area efficient design.

[Abstract] An architecture for a combinational floating point multiplier and squarer is designed for the purpose of producing a low power floating point square with a small area footprint. The floating point multiplier and squarer architecture are compared to each other to show the power advantage of the squarer. The multiplier and squarer are combined into one circuit in order to take advantage of the squarer power improvements while minimally increasing the area. Shared circuitry among the units provides justification for inclusion of a dedicated squarer since a small amount of additional circuitry is required and the power savings for squaring computations is significant as compared to the use of a general-purpose multiplier to generate a square value.

Session C5L-E: Digital Signal Processing II

Chair: Moataz AbdelWahab, *Nile University*
Time: August 7, 2013, 16:00 - 17:40
Location: Suzanne M. Scharer

[Abstract] This paper suggests the use of linear programming and curve fitting to approximate Gaussian filters with a combination of recursive linear-phase exponential filters. The switching and reset method is used to create a stable implementation of an otherwise unstable pole-zero cancelation in the exponential filters. The results show that an accurate approximation of a Gaussian filter, of any order, can be recursively implemented using only 18 constant coefficient multipliers and 26 adders.

[Abstract] Recent advances in signal processing hardware has made possible the implementation of sophisticated algorithms. The Complex Block Conjugate Least Mean Square algorithm with Individual adaptation (CBCI-LMS) has recently been proposed and applied in adaptive filtering applications. This technique involves matrix inversion, which is computationally intensive. To improve the feasibility of the algorithm in practice, especially for high-order adaptive systems, this paper proposes two efficient implementations of the CBCI-LMS algorithm. The first efficient implementation applies an iterative matrix inversion lemma without any sacrifice in convergence speed and accuracy. The second method further simplifies the algorithm by using a diagonal matrix for approximation at the first iteration, at the expense of a few additional iterations to achieve convergence. Both of the simplified approaches effectively reduce the computational complexities of the CBCI-LMS algorithm.

[Abstract] We consider the problem of implementing an algorithm for the extraction of leading eigenvectors of a small Hermitian matrix on field-programmable gate array (FPGA). The evolution of FPGAs can now handle increasingly bandwidth problems or larger in size. Jacobi algorithms are usually implemented in FPGA for real matrix size not exceeding 20*20. The increase in size or complex number problem may lead to use other algorithms such as Lanczos, which are rarely implemented on FPGA. Recently, it has been pointed out that the Lanczos method can efficiently address the extreme eigenvalues computation problem on FPGA, for medium size real matrices. This paper presents an algorithm for the extraction of extremal eigenvalues and corresponding eigenvectors for small Hermitian matrix using a high-level approach for the architecture synthesis.

[Abstract] Since its acceptance as the adopted authenticated encryption algorithm, AES-GCM has been utilized in various security-constrained applications. This paper describes the benefits of adding key-synthesized property to AES-GCM using FPGAs. Presented architectures can be used for applications which require encryption and authentication with slow changing keys like Virtual Private Networks (VPNs). Our architectures were evaluated using Virtex4 and Virtex5 FPGAs. It is shown that the performance of the presented AES-GCM architecture outperforms the previously reported ones.

[Abstract] Particle filters (PFs) are computationally intensive, which prevents them from being widely used in some real-time applications with high throughput requirements. A parallel implementation is a feasible approach to enable using PFs in these applications. However, effective resampling algorithms such as the Systematic Resampling (SR) algorithm are sequential in nature. In this paper, we propose a new form of the SR algorithm suitable for parallel implementation in an Application-Specific Instruction-set Processor (ASIP). Six custom instructions were designed for this reformulated SR algorithm. Experimental results show that the ASIP implementation of the reformulated SR algorithm, with four weights calculated in parallel, and eight categories defined by uniformly distributed numbers that are compared simultaneously to achieve a 30.6× speedup over the serial SR algorithm in a general-purpose processor. This comes at a cost of only 54K additional gates, or 68% overhead to be added to a base processor with 79K gates.

Session C5L-F: Advances in Control Systems, Mechatronics, and Robotics

Chair: Charna Parkey, *University of Central Florida*
Co-Chair: Genevieve Sapijaszko, *Devry University*
Time: August 7, 2013, 16:00 - 17:40
Location: Rosa M. Ailabouni

[Abstract] In this paper we applied predictor-based system identification technique to several different systems, which are identified without and with integrated noise. The PBSID uses the Kalman observer whose Kalman gain is calculated from the Riccati equation thus, the observer matrix is guaranteed to be stable even identified system is unstable. We applied this concept to the CD player arm and the food extruder system to show its effectiveness with simulation using the Matlab©.

[Abstract] In this contribution, we investigate the Generalized synchronization (GS) problem of strictly different nonlinear systems. GS in nonlinear systems appears when the states of one system, through a functional mapping are equal to states of another. This mapping can be obtained if there exist a differential primitive element which generates a differential transcendence basis. The first component of the differential transcendence basis is called differential primitive element and, in general, is defined by means of a linear combination of the known states and the control input. Furthermore, we construct a dynamical feedback controller able to achieve complete synchronization in the coordinate transformation systems and GS in the original coordinates. These particular forms of GS are illustrated with numerical results of Colpitts and Chua circuits.

[Abstract] In this paper an algorithm is proposed to plan the path to be taken by a robot in order to reach a specific coordinate. The algorithm is proposed to be used in a robot with a synchronous propulsion architecture, because this architecture improves robot odometry and has not been common in navigation tasks, mapping and localization. Furthermore, this algorithm determines the shortest path with respect to the resolution of the displacement and rotation of the robot, minimizing the efforts to reach the desired goal.

[Abstract] In this paper we apply predictor-based system identification technique to unstable system to identify system dynamics. Due to instability, we need to avoid diverging output by designing controller which can keep the system poles inside unit circle in discrete time domain. This technique is applied to identify highly oscillatory wind turbine systems. In both cases, the I/O data collected by forming feedback controller (in this case, LQG controller in 1-DOF) have been successfully used for identification of unstable and oscillatory wind turbine systems. Its effectiveness is demonstrated with simulation using the Matlab©.