

# **10th Annual International Wafer-Level Packaging Conference**

**(IWLPC 2013)**

**San Jose, California, USA  
6 – 7 November 2013**

**ISBN: 978-1-62993-453-2**

**Printed from e-media with permission by:**

Curran Associates, Inc.  
57 Morehouse Lane  
Red Hook, NY 12571



**Some format issues inherent in the e-media version may also appear in this print version.**

Copyright© (2013) by Surface Mount Technology Association (SMTA)  
All rights reserved.

Printed by Curran Associates, Inc. (2014)

For permission requests, please contact Surface Mount Technology Association (SMTA)  
at the address below.

Surface Mount Technology Association (SMTA)  
5200 Wilson Road  
Suite 215  
Edina, MN 55424

Phone: (952) 920-4682  
Fax: (952) 926-1819

[www.smta.org](http://www.smta.org)

**Additional copies of this publication are available from:**

Curran Associates, Inc.  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: 845-758-0400  
Fax: 845-758-2634  
Email: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

# IWLPC 2013 PROGRAM | November 6-7, 2013

Wednesday, November 6<sup>th</sup>

## WLP TRACK

### Session 1 – Wafer-Level Automation & Test

**Overcoming the Productivity Challenges in Wafer-Level Packaging** 1

Shekar Krishnaswamy, Applied Materials, Inc.

Co-author: David Hanny, Applied Materials, Inc.

**Automating the Design and Layout of Wafer Level Masks** 6

Steve DiBartolomeo, Artwork Conversion Software

Co-author: Andrew Wilford, Artwork Conversion Software

**Spring Contact Probes in Wafer Level Test: Fundamentals and Advanced Concepts** 12

Jon Diller, Interconnect Devices, Inc.

Co-author: Jiachun (Frank) Zhou, Ph.D., Interconnect Devices, Inc

## 3D TRACK

### Session 2 – Thermo-Compression Bonding for 3D Packaging

**A Process Level Comparative Analysis between D2W Local and Collective 3D Bonding** 19

Robert Daily, IMEC

Co-authors: G. Capuz, T. Wang, P. Bex, H. Struyf, K. Rebibis, IMEC

**Thin Die Interconnect Process for 3DIC Utilizing Multiple Layers of 50 Micron Thick Die on 300mm Wafers with a Tack and Collective Bonding Approach for Manufacturability** 24

Daniel Pascual, CNSE

Co-authors: Colin McDonough, Anh Nguyen, Megha Rao, Robert Carroll, Doug Coolbaugh, Joseph Piccirillo, and Robert Green, CNSE

**Exploring Process Interaction of No-Flow Underfill and Thermo-Compression Bonding in D2D Stacking** 28

Giovanni Capuz, IMEC

Co-authors: Robert Daily, Teng Wang, Herbert Struyf, Andy Miller, and Kenneth June Rebibis, IMEC

## MEMS TRACK

### Session 3 – Wafer-Level Packaged MEMS

**MEMS Packaging: What Makes It So Special?** 36

Rozalia Beica, Yole Développement

**30 Years of Wafer-Level Packaging for Microsystems: From Automotive to Mobile Electronics and Beyond** 39

Leland "Chip" Spangler, Ph.D., Aspen Microsystems, LLC

**Wafer Level Packaging for Ultra-Miniature/Low-Cost MEMS Accelerometers** 48

Noureddine Hawat, MEMSIC Inc.

Co-authors: Zhiwei Duan and Yang Zhao, Ph.D., MEMSIC Inc.

## WLP TRACK

### Session 4 – Wafer-Level Materials

**Single Wafer Resist Removal for Wafer Level Packaging with Improved Process Integration** 52

Travis Acra, Dynaloy

Co-authors: Travis Acra, Richie Peters, Yuanmei Cao, Kimberly Pollard, Don pfetts chen, and Don Pettscher, and Meng Guo, Dynaloy, a Subsidiary of Eastman Chemical Co.

**Modeling the Imidization Kinetics of a Low Temperature Cure Photosensitive Polyimide in Solid State** 59

Frank Windrich, Fraunhofer IZM-ASSID

Co-authors: Mikhail Malanin, Ph.D., Klaus-Jochen Eichhorn, Ph.D., Brigitte Voit, Leibniz Institute of Polymer Research Dresden e.v.

**Reliable Interconnection with Electroplated Cu Pillars and Snag Solder Caps** 66

Yi Qin, Ph.D., Dow Electronics Materials

Co-authors: Jeff Calvert, Jui-Ching Lin, Jianwei Dong, Masaaki Imanari, Inho Lee, Pedro Lopez Montesinos, Jonathan Prange, Erik Reddington, Wataru Tachikawa, Julia Woertink, Dow Chemical Company

**Study of the Electroless Plating Process for Special Materials or Small Pads for UBM Formation** 70

Donald Gudeczauskas, Uyemura International Corporation

Co-authors: Shigeo Hashimoto, Yukinori Oda, Shinji Ishimaru, Hiromu Inagawa, Uyemura International Corporation

**3D TRACK | 1:45pm – 3:45pm | SAN CARLOS**

**Session 5 – 3D Processing and Technology**

**Polyimide PCB Embedded with Two Dies in Stacked Configuration** 76

Koji Munakata, Fujikura Ltd.

Co-authors: Nobuki Veta, Masahiro Okamoto, Kumihisa Onodera, Kazu Itoi, and Satoshi Okude, and Osamu Nakao Fujikura Ltd.; Jon Aday and Theodore (Ted) Tessier, Flipchip International

**An Investigation on the Effect of Upstream Processes on the Quality of Cu-Cu Bonding Interconnect Under Controlled Manufacturing Environment** 82

Anh Nguyen, Ph.D., State University of New York at Albany

Co-authors: Daniel Pascual, Eric Malocsay, Kevin Fealy, Paul Tariello, and Peter Reilly, State University of New York at Albany

**Interconnect Structure for Room Temperature 3D-IC Stacking Employing Binary Alloying for High Temperature Stability** 88

Eric Schulte, SET North America

Co-authors: Matthew Lueck and Alan Huffman, RTI; Keith Cooper, SET North America

**Temporary Bonding Material Total Thickness Variation (TTV)** 93

Aaron Jacobs, Brewer Science, Inc.

Co-authors: M. Preivett and G. Brand, Brewer Science

**MEMS TRACK**

**Session 6 – Wafer Bonding and Testing for MEMS**

**Metal Inter-Diffusion and Eutectic Wafer Bonding Processes for Advanced MEMS Packaging** 99

Sumant Sood, SUSS MicroTec

**Multiple Wafer MEMS WLP** 105

Mike Shillinger, Innovative Micro Technology

**Examination of Key Packaging Metrics of a Hermetically Sealed MEMS Geosensor** 110

Joshua Krabbe, MSC, Micralyne Inc.

Co-authors: Nick Wakefield, Ph.D., Serguei Roupasov, MSC, Peter Hrudey, Ph.D., Andy vanPopta, Ph.D., and Siamak Akhlaghi, Ph.D., Micralyne Inc.

**Minimizing Cost of Calibration and Test (COCT) to Drive Cost Reduction of MEMS** 118

John Rychcik, Multitest Electronic Systems, Inc.

Co-author: Barbara Loferer, Multitest Electronic Systems, Inc.

# IWLPC 2013 PROGRAM | November 6-7, 2013

Thursday, November 7<sup>th</sup>

## WLP TRACK

### Session 7 – Wafer-Level Process

**High-Speed Removal of Thick Negative Photoresist in Advanced Packaging Applications** 123

Mani Sobhian, TEL NEXX

Co-authors: Dave Webster, IBM; and Patrick Kearney, IMEC

**Micro Ball Bumping Packaging for Wafer-Level & 3-D Solder Sphere Transfer and Solder Jetting** 133

Richard McKee, Pac Tech- USA

Co-authors: Thomas Oppert, Thorsten Teutsch, Ghassem Azdasht, and Elke Zakel, Pac Tech

**Advances in 300mm WLCSP Spheron™ Cu Plated RDL Technology for Higher Density and Lower Cost Packaging** 138

André Cardoso, Nanium S.A.

Co-authors: Anthony Curtis, FlipChip International

## 3D TRACK

### Session 8 – Interposers

**Some Trends in the Field of Silicon Interposers** 143

Andre Rouzaud, CEA-Léti

Co-authors: G. Simon and JP. Polizzi, CEA-Léti

**Novel Cheap Solutions for 3D Integration on Wafers with Thin Interposers** 149

Semyon Savransky, Ph.D., The TRIZ Experts

**2.5D and 3D Packaging Platform for Next Generation RF and Digital Modules Using Through Glass via (TGV) Technology** 152

Sergio Cardona, nMode Solutions, Inc.

Co-author: Tim Mobley, Triton Micro Tech, Inc.

## 3D TRACK

### Session 9 –3D Metrology and Test

**Quality in 3D Assembly – Is “Known Good Die” Good Enough?** 156

James Quinn, Multitest

Co-author: Barbara Loferer, Multitest

**Inspection and Metrology Solutions for Copper Pillar High Volume Manufacturing** 161

Rajiv Roy, Rudolph Technologies

**Optical Technologies for TSV Inspection** 166

Arun Aiyer, Frontier Semiconductor

Co-authors: Nikolai Maltsev and Jaesok Ryu, Frontier Semiconductor

## WLP TRACK

### Session 10 - Fan-Out Wafer-Level Packaging Technologies

**Implementation of a Fully Molded Fan-Out Packaging Technology** 172

William Rogers, Ph.D., DECA Technologies

Co-authors: Chris Scanlan and Tim Olson, DECA Technologies

**Cost Comparison of Multi-Die Fan-Out Wafer Level Packaging and 2.5D Packaging with a Silicon Interposer** 178

Amy Palesko, SavanSys Solutions LLC

Co-author: Chet Palesko, SavanSys Solutions LLC and E. Jan Vardaman, TechSearch International, Inc.

**Choosing Lithography Equipment to Minimize the Cost of Wafer Level Packaging** 183  
Tim McCrone, SUSS MicroTec

**3D TRACK**

**Session 11 - TSV Processing and Implementation**

**TSV Resist and Etch Residue Removal for 3DIC** 188

Kim Pollard, Dynaloy  
Co-authors: Richard Peters, Mike Phenix, Yuanmei Cao, and Travis Acra, Dynaloy

**Recent Results Using Met-Via® TSV Interposer Technology as TMV Element in Wafer-Level through Mold via Packaging of CMOS Biosensors** 193

Jessica Fredlund, SILEX Microsystems AB  
Co-Authors: Thorbjorn (Toby) Ebefors, Ph.D., SILEX Microsystems AB; Erik Jung and Tanja Braun, Fraunhofer IZM

**Converging Front-End, Back-End and Flat Panel Display Manufacturing Technologies To Meet 2.5/3D And Fan-Out Packaging Requirements** 201

Klaus Ruhmer, Rudolph Technologies  
Co-authors: Rajiv Roy and Elvino Da Silveira, Rudolph Technologies

**3D TRACK**

**Session 12 - 3D Processing**

**Vacuum-assisted Wet Processing for Advanced 3D Devices** 206

Ismail Kashkoush, Ph.D., Akרון Systems

**Low Warpage and Improved 2.5/3Dic Process Capability with a Low Stress Polyimide Dielectric** 213

Robert Hubbard, Lambda Technologies  
Co-authors: Bong-Sub Lee, Invensas Technologies

**Microbump Lithography for 3D Stacking Applications** 220

Gareth Kenyon, Ultratech Inc.  
Co-authors: Patrick Jaenen and John Slabbekoorn, IMEC; Warren Flack, Manish Ranjan, Robert Hsieh, and Ha-Ai Nguyen, Ultratech