

2014 20th IEEE International Symposium on Asynchronous Circuits and Systems

(ASYNC 2014)

Potsdam, Germany
12-14 May 2014



IEEE Catalog Number: CFP14012-POD
ISBN: 978-1-4799-3790-5

2014 20th IEEE International Symposium on Asynchronous Circuits and Systems

ASYNC 2014

Table of Contents

Welcome Message from the Chairs.....	vii
Committees	ix
Sponsors.....	xii
Keynote Talks.....	xiii

Session 1: Error Resilience

A Compact Soft-Error Tolerant Asynchronous TCAM Based on a Transistor/Magnetic-Tunnel-Junction Hybrid Dual-Rail Word Structure	1
<i>Naoya Onizawa, Shoun Matsunaga, and Takahiro Hanyu</i>	
An Asynchronous SDM Network-on-Chip Tolerating Permanent Faults	9
<i>Guangda Zhang, Wei Song, Jim Garside, Javier Navaridas, and Zhiying Wang</i>	

Session 2: Interfacing Fundamentals

GALS Partitioning by Behavioural Decoupling Expressed in Petri Nets	17
<i>Danil Sokolov and Alex Yakovlev</i>	
Modelling Mixed 4phase Pipelines: Structures and Patterns	27
<i>Graham M. Birtwistle and Kenneth S. Stevens</i>	

Session 3: Established Applications

Effect of Dynamic Frequency Scaling on Interface Design for Rationally-Related Multi-clocked Systems	37
<i>Joycee Mekie</i>	
Argo: A Time-Elastic Time-Division-Multiplexed NOC Using Asynchronous Routers	45
<i>Evangelia Kasapaki and Jens Sparsø</i>	

Session 4: Asynchronous Design Automation

Semi-custom NCL Design with Commercial EDA Frameworks: Is it Possible?	53
<i>Matheus Moreira, Augusto Neutzling, Mayler Martins, André Reis, Renato Ribas, and Ney Calazans</i>	
Synthesis of QDI FSMs from Synchronous Specifications	61
<i>Fu-Chiung Cheng, Yuan-Feng Chen, Shu-Chuan Huang, and Ching Yang Huang</i>	
Integrated Fanout Optimization and Slack Matching of Asynchronous Circuits	69
<i>Mehrdad Najibi and Peter A. Beerel</i>	

Session 5: Low Power

Reconditioning: Automatic Power Optimization of QDI Circuits	77
<i>Arash Saifhashemi, Hsin-Ho Huang, and Peter A. Beerel</i>	
Low Power Asynchronous VLSI with NEM Relays	85
<i>Benjamin Z. Tang, Sunil A. Bhave, and Rajit Manohar</i>	

Session 6: Tools and Libraries

A New CMOS Topology for Low-Voltage Null Convention Logic Gates Design	93
<i>Matheus Trevisan Moreira, Michel Evandro Arendt, Ricardo Aquino Guazzelli, and Ney Laert Vilar Calazans</i>	

Industrial Session 1: Metastability

Metastability in Better-Than-Worst-Case Designs	101
<i>Salomon Beer, Marco Cannizzaro, Jordi Cortadella, Ran Ginosar, and Luciano Lavagno</i>	

Industrial Session 2: Design and Test

A 72-Port 10G Ethernet Switch/Router Using Quasi-Delay-Insensitive Asynchronous Design	103
<i>Mike Davies, Andrew Lines, Jon Dama, Alain Gravel, Robert Southworth, Georgios Dimou, and Peter Beerel</i>	
Test and Repair Flow for Shared BISR in Asynchronous Multi-processors	105
<i>Gang Wang, Xu Wang, Xink Chen, and Shuangbai Xue</i>	
Clockless Design Performance Monitoring for Nanometer Technologies	108
<i>Marc Renaudin, Aurélien Buhrig, Charles Guillemet, Robin Wilson, and Sylvain Engels</i>	
Performance and Area Optimization of a Bundled-Data Intel Processor through Resynthesis	110
<i>Arash Saifhashemi, Dylan Hand, Peter A. Beerel, William Koven, and Hong Wang</i>	
Author Index	112