

2014 International Conference on Simulation of Semiconductor Processes and Devices

(SISPAD 2014)

**Yokohama, Japan
9-11 September 2014**



IEEE Catalog Number: CFP14SSD-POD
ISBN: 978-1-4799-5289-2

PROGRAM

September 9

9:00–9:10 Opening and Welcome Remarks

N. Mori (*Osaka Univ., Japan*)

Session 1: Plenary

Chairpersons: K. Sonoda (*Renesas Electronics, Japan*)

M. Stettler (*Intel, USA*)

1-1 9:10–9:55 [invited talk]

“Physics of Electronic Transport in Low-Dimensionality Materials for Future FETs”

M.V. Fischetti¹, W.G. Vandenberghe¹, B. Fu¹, S. Narayanan¹, J. Kim¹, Z.-Y. Ong¹, A. Suarez-Negreira¹, C. Sachs¹, and S.J. Aboud² (¹*Univ. Texas Dallas, USA*, ²*Stanford Univ., USA*) 1

1-2 9:55–10:40 [invited talk]

“Current Status and Future Prospects of Non-Volatile Memory Modeling”

A. Benvenuti¹, A. Ghetti¹, A. Mauri¹, H. Liu², and C. Mouli²

(¹*Micron Technology, Italy*, ²*Micron Technology, USA*) 5

1-3 10:40–11:25 [invited talk]

“Challenge of Adopting TCAD in the Development of Power Semiconductor Devices for Automotive Applications”

K. Hamada (*Toyota Motor Corporation, Japan*) 9

11:25–13:00 *Lunch*

Session 2: FinFET

Chairpersons: T. Noda (*Panasonic, Japan*)

N. Goldsman (*Univ. Maryland, USA*)

2-1 13:00–13:30 [invited talk]

“Device and Process Modeling: 20 Years at Intel’s Other Fab”

M.A. Stettler (*Intel Corporation, USA*) 13

2-2 13:30–13:50

“Analysis of Heat Conduction Property in FinFETs Using Phonon Monte Carlo Simulation”

I.N. Adisusilo¹, K. Kukita¹, and Y. Kamakura^{1,2} (¹*Osaka Univ., Japan*, ²*JST CREST, Japan*) 17

2-3 13:50–14:10

“3D Multi-Subband Ensemble Monte Carlo Simulator of FinFETs and Nanowire Transistors”

C. Sampredo¹, L. Donetti¹, F. Gámiz¹, A. Godoy¹, F.J. Garcia-Ruiz¹, V.P. Georgiev², S.M. Amoroso², C. Riddet³, E.A. Towie³, and A. Asenov^{2,3} (¹*Univ. Granada, Spain*, ²*Univ. Glasgow, UK*, ³*Gold Standard Simulations Ltd., UK*) 21

2-4	14:10–14:30	“USJ Engineering Impacts on FinFETs and RDF Investigation Using Full 3D Process/Device Simulation” E.M. Bazizi ¹ , A. Zaka ¹ , T. Herrmann ¹ , F. Benistant ² , J.H.M. Tin ² , J.P. Goh ² , L. Jiang ³ , M. Joshi ³ , H. van Meer ³ , and K. Korablev ³ (¹ <i>GLOBALFOUNDRIES Inc., Germany</i> , ² <i>GLOBALFOUNDRIES Inc., Singapore</i> , ³ <i>GLOBALFOUNDRIES Inc., USA</i>) 25
2-5	14:30–14:50	“Accurate Fringe Capacitance Model Considering RSD and Metal Contact for Realistic FinFETs and Circuit Performance Simulation” K.K. Choe, T.Y. An, and S.Y. Kim (<i>Sungkyunkwan Univ., Korea</i>) 29

Session 3: Nonvolatile Memories I

Chairpersons: T. Kunikiyo (*Renesas Electronics, Japan*)
T. Wada (*Samsung, Japan*)

3-1	13:30–13:50	“Advanced Simulation of CBRAM Devices with the Level Set Method” P. Dorion ^{1,2} , O. Cueto ¹ , M. Reyboz ¹ , J.C. Barbe ¹ , A. Grigoriu ³ , and Y. Maday ² (¹ <i>CEA-Leti, France</i> , ² <i>UPMC, France</i> , ³ <i>Univ. Paris Diderot, France</i>) 33
3-2	13:50–14:10	“Multi-Scale Modeling of Oxygen Vacancies Assisted Charge Transport in Sub-Stoichiometric TiO _x for RRAM Applications” O. Pirrotta ¹ , A. Padovani ¹ , L. Larcher ¹ , L. Zhao ² , B. Magyari-Kope ² , and Y. Nishi ² (¹ <i>Univ. Modena and Reggio Emilia, Italy</i> , ² <i>Stanford Univ., USA</i>) 37

3-3	14:10–14:30	“Verilog-A Compact Model for Oxide-Based Resistive Random Access Memory (RRAM)” Z. Jiang ¹ , S. Yu ² , Y. Wu ³ , J.H. Engel ¹ , X. Guan ⁴ , and H.-S.P. Wong ¹ (¹ <i>Stanford Univ., USA</i> , ² <i>Arizona State Univ., USA</i> , ³ <i>Oracle, USA</i> , ⁴ <i>IBM, USA</i>) 41
3-4	14:30–14:50	“Development of an Electro-Thermal Resistive Switching Model Based on O-Frenkel Pairs to Study Reset and Set Mechanisms in HfO ₂ -based RRAM Cells” O. Cueto, A. Payet, and T. Cabout (<i>CEA-Leti, France</i>) 45

14:50–15:10 *Coffee Break*

Session 4: Power Devices

Chairpersons: H. Hayashi (*Lapis Semiconductor, Japan*)
C.-K. Lin (*TSMC, Taiwan*)

4-1	15:10–15:40 [invited talk]	“Exploring the Limits of the Safe Operation Area of Power Semiconductor Devices” C. Sandow ¹ , R. Baburske ¹ , F.-J. Niedernostheide ¹ , F. Pfirsich ¹ , and C. Töchterle ² (¹ <i>Infineon Technologies AG, Germany</i> , ² <i>Tech. Univ. München, Germany</i>) 49
4-2	15:40–16:00	“A Novel Duality-Based Modeling Methodology for Reverse Current-Voltage Characteristics of SiC” T. Yamamoto, T. Sawai, K. Mizutani, N. Otsuka, E. Fujii, N. Horikawa, and Y. Kanzawa (<i>Panasonic Corporation, Japan</i>) 53

4-3	16:00–16:20	
	“Efficient and Universal Method to Design Multiple Field Limiting Rings for Power Devices” M. Mochizuki, H. Tanaka, and H. Hayashi (<i>LAPIS Semiconductor Co., Ltd., Japan</i>)	57
4-4	16:20–16:40	
	“Effects of Carbon-Related Oxide Defects on the Reliability of 4H-SiC MOSFETs” D. Ettisserry ¹ , N. Goldsman ¹ , A. Akturk ¹ , and A.J. Lelis ² (¹ <i>Univ. Maryland, USA</i> , ² <i>U.S. Army Research Lab., USA</i>)	61

Session 5: Atomic Level Simulation

Chairpersons: T. Sugiyama (*Toyota Central R&D Lab., Japan*)
M. Rudan (*Univ. Bologna, Italy*)

5-1	15:40–16:00	
	“Towards Atomic Level Simulation of Electron Devices Including the Semiconductor-Oxide Interface” S. Markov ¹ , C.Y. Yam ¹ , G.H. Chen ¹ , B. Aradi ² , G. Penazzi ² , and T. Frauenheim ² (¹ <i>Univ. Hong Kong, China</i> , ² <i>Univ. Bremen, Germany</i>)	65
5-2	16:00–16:20	
	“Atomic Ordering Effect on SiGe Electronic Structure” Y.-T. Tung, E. Chen, T.-M. Shen, Y. Okuno, C.-C. Wu, J. Wu, and C.H. Diaz (<i>TSMC, Taiwan</i>)	69
5-3	16:20–16:40	
	“Density-Functional-Theory-Based Study of Monolayer MoS ₂ on Oxide” A. Valsaraj ¹ , L.F. Register ¹ , S.K. Banerjee ¹ , and J. Chang ² (¹ <i>Univ. Texas Austin, USA</i> , ² <i>SEMATECH, USA</i>)	73
	18:00–20:00 <i>Reception</i>	

September 10

Session 6: Reliability I

Chairpersons: A. Hiroki (*Kyoto Inst. Tech., Japan*)
A. Asenov (*Univ. Glasgow, UK*)

6-1	9:00–9:30	[invited talk]
	“Advanced Modeling of Charge Trapping: RTN, 1/f noise, SILC, and BTI” W. Goes, M. Waltl, Y. Wimmer, G. Rzepa, and T. Grasser (<i>TU Wien, Austria</i>)	77
6-2	9:30–9:50	
	“Physical Modeling of NBTI: From Individual Defects to Devices” G. Rzepa ¹ , W. Goes ¹ , G. Rott ² , K. Rott ² , M. Karner ³ , C. Kernstock ³ , B. Kaczer ⁴ , H. Reisinger ² , and T. Grasser ¹ (¹ <i>TU Wien, Austria</i> , ² <i>Infineon Technologies AG, Germany</i> , ³ <i>Global TCAD Solutions GmbH, Austria</i> , ⁴ <i>imec, Belgium</i>)	81
6-3	9:50–10:10	
	“Time Dependent 3-D Statistical KMC Simulation of High-k Degradation Including Trap Generation and Electron Capture/Emission Dynamic” Y. Wang, P. Huang, X. Liu, G. Du, and J. Kang (<i>Peking Univ., China</i>)	85

10:10–10:30 *Coffee Break*

6-4 10:30–10:50

“A Predictive Physical Model for Hot-Carrier Degradation in Ultra-Scaled MOSFETs”

S. Tyaginov^{1,2}, M. Bina¹, J. Franco³, Y. Wimmer¹, D. Osintsev¹, B. Kaczer³, and T. Grasser¹

(¹TU Wien, Austria, ²Ioffe Phys. Tech. Inst., Russia, ³imec, Belgium) 89

6-5 10:50–11:10

“3D Atomistic Simulations of Bulk, FDSOI and Fin FETs Sensitivity to Oxide Reliability”

L. Gerrer¹, S. Amoroso¹, R. Hussin¹, F. Adamu-Lema¹, and A. Asenov²

(¹Univ. Glasgow, UK, ²Gold Standard Simulations Ltd., UK) 93

6-6 11:10–11:30

“Study of AlGaN/GaN HEMT Degradation through TCAD Simulations”

H.Y. Wong¹, N. Braga¹, R.V. Mickevicius¹, F. Gao², and T. Palacios²

(¹Synopsys, Inc., USA, ²MIT, USA) 97

Session 7: Transport

Chairpersons: Y. Kamakura (*Osaka Univ., Japan*)

C. Jungemann (*RWTH Aachen Univ., Germany*)

7-1 9:30–9:50

“Experimental and Theoretical Investigation of the ‘Apparent’ Mobility Degradation in Bulk and UTBB-FDSOI Devices: A Focus on the Near-Spacer-Region Resistance”

D. Rideau¹, F. Monsieur¹, O. Nier^{1,2}, Y.M. Niquet³, J. Lacord⁴, V. Quenette¹, G. Mugny^{1,4}, G. Hiblot^{1,2}, G. Gouget¹, M. Quoirin¹, L. Silvestri⁵, F. Nallet⁵, C. Tavernier¹, and H. Jaouen¹ (¹STMicroelectronics, France, ²IMEP-LAHC, France, ³SP2M, France, ⁴CEA-Leti, France, ⁵Synopsys, Inc., Switzerland) 101

7-2 9:50–10:10

“Monte Carlo study of Effective Mobility in Short Channel FDSOI MOSFETs”

S. Guarnay^{1,2}, F. Triozon¹, S. Martinie¹, Y.-M. Niquet³, and A. Bourrel²

(¹CEA-Leti, France, ²Univ. Paris-Sud, France, ³CEA-UJF, France) 105

10:10–10:30 *Coffee Break*

7-3 10:30–10:50

“Semi-Classical Ensemble Monte Carlo Simulator Using Innovative Quantum Corrections for Nano-Scale n-Channel FinFETs”

D.M. Crum, A. Valsaraj, L.F. Register, and S.K. Banerjee (*Univ. Texas Austin, USA*) 109

7-4 10:50–11:10

“The Wigner Monte Carlo Method for Accurate Semiconductor Device Simulation”

P. Ellinghaus, M. Nedjalkov, and S. Selberherr (*TU Wien, Austria*) 113

7-5 11:10–11:30

“Investigation of Quantum Transport in Nanoscaled GaN High Electron Mobility Transistors”

O. Baumgartner¹, Z. Stanojević¹, L. Filipović¹, A. Grill¹, T. Grasser¹, H. Kosina¹, and M. Karner²

(¹TU Wien, Austria, ²Global TCAD Solutions GmbH, Austria) 117

11:30–13:00 *Lunch*

Session 8: TCAD Application and Novel Materials

Chairpersons: T. Iizuka (*Hiroshima Univ., Japan*)
A. Akturk (*Univ. Maryland, USA*)

8-1	13:00–13:30 [invited talk]	
	“Nonlinear Thermoelectroelastic Simulation of III-N Devices” M.G. Ancona (<i>Naval Research Lab., USA</i>)	121
8-2	13:30–13:50	
	“Analysis of GeSn-SiGeSn Hetero-Tunnel FETs” S.R. Sant ¹ , Q.-T. Zhao ² , D. Buca ² , S. Mantl ² , and A. Schenk ¹ (¹ <i>ETH Zurich, Switzerland</i> , ² <i>Peter Gruenberg Inst., Germany</i>)	125
8-3	13:50–14:10	
	“Simulation of Light-Illuminated STM Measurements” K. Fukuda ¹ , M. Nishizawa ¹ , T. Tada ¹ , L. Bolotov ² , K. Suzuki ³ , S. Sato ³ , H. Arimoto ¹ , and T. Kanayama ¹ (¹ <i>AIST, Japan</i> , ² <i>Tsukuba Univ., Japan</i> , ³ <i>Fujitsu Semiconductor Ltd., Japan</i>)	129
8-4	14:10–14:30	
	“Organic Thin-Film Transistor Compact Model with Accurate Charge Carrier Mobility” T.K. Maiti, T. Hayashi, L. Chen, M. Miura-Mattausch, and H.J. Mattausch (<i>Hiroshima Univ., Japan</i>)	133
8-5	14:30–14:50	
	“DC, AC and Noise Simulation of Organic Semiconductor Devices Based on the Master Equation” C. Jungemann and C. Zimmermann (<i>RWTH Aachen Univ., Germany</i>)	137

Session 9: Nonvolatile Memories II

Chairpersons: K. Matsuzawa (*Toshiba, Japan*)
C. Mouli (*Micron Technology, USA*)

9-1	13:30–13:50	
	“Investigation of Retention Behavior for 3D Charge Trapping NAND Flash Memory by 2D Self-Consistent Simulation” Z. Lun, S. Liu, Y. He, Y. Hou, K. Zhao, G. Du, X. Liu, and Y. Wang (<i>Peking Univ., China</i>)	141
9-2	13:50–14:10	
	“An Analysis of the Effect of Hydrogen Incorporation on Electron Traps in Silicon Nitride” K. Sonoda, E. Tsukuda, M. Tanizawa, K. Ishikawa, and Y. Yamaguchi (<i>Renesas Electronics Corporation, Japan</i>)	145
9-3	14:10–14:30	
	“A Unified Circuit Model for Ferroelectrics” K. Auluck ¹ , E.C. Kan ¹ , and S.R. Rajwade ² (¹ <i>Cornell Univ., USA</i> , ² <i>Intel Corporation, USA</i>)	149

Poster Session

Chairperson: S. Satoh (*Fujitsu Semiconductor, Japan*)

- P1** “Extraction of Quasi-Ballistic Transport Parameters in Si Double-Gate MOSFETs Based on Monte Carlo Method,” R. Ishida¹, S. Koba¹, H. Tsuchiya^{1,2}, Y. Kamakura^{2,3}, N. Mori^{2,3}, S. Uno^{2,4}, and M. Ogawa¹ (¹Kobe Univ., Japan, ²JST CREST, Japan, ³Osaka Univ., Japan, ⁴Ritsumeikan Univ., Japan) 153
- P2** “Physical Modeling of Time Dependent Dielectric Breakdown (TDDB) of BEOL Oxide using Monte Carlo Particle Simulation,” S. Choi and Y.J. Park (*Seoul National Univ., Korea*) 157
- P3** “High-Order Solution Scheme for Transport in Low-D Devices,” F. Buscemi¹, E. Piccinini², R. Brunetti¹, and M. Rudan² (¹Univ. Modena and Reggio Emilia, Italy, ²Univ. Bologna, Italy) 161
- P4** “Spatial Distribution of State Densities Dominating Strain Sensitivity of Carbon Nanotubes,” M. Ohnishi, K. Suzuki, and H. Miura (*Tohoku Univ., Japan*) 165
- P5** “Optimization of Program and Erase Characteristics of Two Bit Flash Memory P-Channel Cell Structure Using TCAD,” H. Hayashi¹, V. Axelrad², M. Mochizuki¹, T. Hayashi¹, T. Maruyama¹, K. Suzuki¹, and Y. Nagatomo¹ (¹LAPIS Semiconductor Co., Ltd., Japan, ²SEQUOIA Design Systems, USA) 169
- P6** “Avalanche Breakdown of PN-Junctions - Simulation by Spherical Harmonics Expansion of the Boltzmann Transport Equation,” D. Jabs and C. Jungemann (*RWTH Aachen Univ., Germany*) 173
- P7** “The Role of Electron Viscosity on Plasma-Wave Instability in HEMTs,” H. Wang, W. Li, J. Zhang, Y. Wang, and Z. Yu (*Tsinghua Univ., China*) 177
- P8** “On the Validity of Momentum Relaxation Time in Low-Dimensional Carrier Gases,” Z. Stanojević¹, O. Baumgartner¹, M. Karner², L. Filipović¹, C. Kernstock², and H. Kosina¹ (¹TU Wien, Austria, ²Global TCAD Solutions GmbH, Austria) 181
- P9** “Self-Forces in 3D Finite Element Monte Carlo Simulations of a 10.7 nm Gate Length SOI FinFET,” M. Aldegunde and K. Kalna (*Swansea Univ., UK*) 185
- P10** “A Study of Performance Enhancement in Uniaxial Stressed Silicon Nanowire Field Effect Transistors,” H.-E. Jung, W.J. Jeong, and M. Shin (*KAIST, Korea*) 189
- P11** “Increasing Mobility and Spin Lifetime with Shear Strain in Thin Silicon Films,” D. Osintsev, V. Sverdlov, T. Windbacher, and S. Selberherr (*TU Wien, Austria*) 193
- P12** “A Three Dimensional TCAD System Focused on Power and Nano-Scaled Device Applications,” Y. Ookura, N. Kato, S. Kobayashi, T. Kuwabara, M. Harada, K. Yamaguchi, and H. Koike (*AdvanceSoft Corporation, Japan*) 197
- P13** “Numerical Simulation of Current Noise Caused by Potential Fluctuation in Nanowire FET with an Oxide Trap,” Y. Furubayashi, M. Ogawa, and S. Souma (*Kobe Univ., Japan*) 201
- P14** “A Simulation Analysis of Backside-Illuminated Multi-Collection-Gate Image Sensor Employing Monte Carlo Method,” K. Shimonomura¹, V.T.S. Dao¹, T.G. Etoh¹, and Y. Kamakura² (¹Ritsumeikan Univ., Japan, ²Osaka Univ., Japan) 205
- P15** “Predictive Modeling of Pattern-Dependent Etch Effects in Large-Area Fully-Integrated 3D Virtual Fabrication,” D.M. Fried, K.B. Greiner, D.B. Faken, M. Kamon, A.L. Pap, R.J. Patz, M.J. Stock, J.T. Lehto, and S.R. Breit (*Coventor, Inc., USA*) 209
- P16** “Optimization of Si MOS Transistors for THz Detection Using TCAD Simulation,” R. Jain^{1,2}, H. Rücker¹, and N.R. Mohapatra² (¹IHP, Germany, ²IIT Gandhinagar, India) 213
- P17** “Template-Based Mesh Generation for Semiconductor Devices,” F. Rudolf, J. Weinbub, K. Rupp, A. Morhammer, and S. Selberherr (*TU Wien, Austria*) 217

- P18** “Electromigration in Solder Bumps: A Mean-Time-to-Failure TCAD Study,” H. Ceric, W.H. Zisser, M. Rovitto, and S. Selberherr (*TU Wien, Austria*) 221
- P19** “Modeling and Algorithms of Device Simulation for Ultra-High Speed Devices,” H. Mutoh (*Link Research Corporation, Japan*) 225
- P20** “Diameter Dependence of Scattering Limited Transport Properties of Si Nanowire MOSFETs under Uniaxial Tensile Strain,” T. Tanaka and K.M. Itoh (*Keio Univ., Japan*) 229
- P21** “Modeling Self-Heating Effects in AlGaN/GaN Electronic Devices during Static and Dynamic Operation Mode,” A.N. Tallarico, P. Magnone, E. Sangiorgi, and C. Fiegna (*Univ. Bologna, Italy*) 233
- P22** “Electro-Thermal Simulation of Silicon Carbide Power Modules,” A. Akturk, N. Goldsman, and S. Potbhare (*CoolCAD Electronics, LLC, USA*) 237
- P23** “Nano-meter Scaled Gate Area High-K Dielectrics with Trap-Assisted Tunneling and Random Telegraph Noise,” P.-J.J. Lin, Z.-A.A. Lee, C.-W.K. Yao, H.-J.V. Lin, and H. Watanabe (*National Chiao Tung Univ., Taiwan*) 241
- P24** “BTB Tunneling in InAs/Si Heterojunctions,” L. Filipović, O. Baumgartner, Z. Stanojević, and H. Kosina (*TU Wien, Austria*) 245
- P25** “Electromigration Induced Resistance Increase in Open TSVs,” W.H. Zisser, H. Ceric, J. Weinbub, and S. Selberherr (*TU Wien, Austria*) 249
- P26** “MC/DD Study of Metal Grains Induced Current Variability in a Nanoscale InGaAs FinFET,” N. Seoane¹, M. Aldegunde¹, K. Kalna¹, and A. García-Loureiro² (¹*Swansea Univ., UK*, ²*Univ. Santiago de Compostela, Spain*) 253
- P27** “Atomistic Simulations of Phonon- and Alloy-Scattering-Limited Mobility in SiGe nFinFETs,” H.-H. Park¹, Y. Lu¹, W. Choi¹, Y.-T. Kim², K.-H. Lee², and Y. Park² (¹*Samsung Semiconductor Inc., USA*, ²*Samsung Electronics, Korea*) 257
- P28** “Monte Carlo Simulation of InAlAs/InGaAs HEMTs with Various Shape of Buried Gate,” A. Endoh^{1,2}, I. Watanabe¹, A. Kasamatsu¹, and T. Mimura^{1,2} (¹*INCT, Japan*, ²*Fujitsu Laboratories Ltd., Japan*) . 261
- P29** “Large-Scale 3D TCAD Study of the Impact of Shorts in Phase Controlled Thyristors,” M. Bellini¹ and J. Vobecký² (¹*ABB, Switzerland*, ²*ABB Semiconductors Inc., Switzerland*) 265
- P30** “3D Coupled Electro-Thermal FinFET Simulations Including the Fin Shape Dependence of the Thermal Conductivity,” L. Wang¹, A.R. Brown², M. Nedjalkov³, C. Alexander², B. Cheng^{1,2}, C. Millar², and A. Asenov^{1,2} (¹*Univ. Glasgow, UK*, ²*Gold Standard Simulations Ltd., UK*, ³*TU Wien, Austria*) ... 269

September 11

Session 10: Variability

Chairpersons: K. Fukuda (*AIST, Japan*)
T. Grasser (*TU Wien, Austria*)

10-1 9:00–9:30 **[invited talk]**

“Progress in the Simulation of Time Dependent Statistical Variability in Nano CMOS Transistors”
A. Asenov^{1,2}, S.M. Amoroso¹, and L. Gerrer¹
(¹*Univ. Glasgow, UK*, ²*Gold Standard Simulations Ltd., UK*) 273

10-2	9:30–9:50	
“A FinFET LER V_T Variability Estimation Scheme with 300x Efficiency Improvement” S.N. Chinta, S. Mittal, P. Debasish, and U. Ganguly (<i>IIT Bombay, India</i>) 277		
10-3	9:50–10:10	
“The Impact of Fin/Sidewall/Gate Line Edge Roughness on Trapezoidal Bulk FinFET Devices” W.-T. Huang and Y. Li (<i>National Chiao Tung Univ., Taiwan</i>) 281		
10:10–10:30 <i>Coffee Break</i>		
10-4	10:30–10:50	
“The Discrepancy Between the Uniform and Variability Aware Atomistic TCAD Simulations of Decananometer Bulk MOSFETs and FinFETs” F. Adamu-Lema ¹ , S.M. Amoroso ¹ , X. Wang ¹ , B. Cheng ^{1,2} , L. Shifren ³ , R. Aitken ³ , S. Sinha ³ , G. Yeric ³ , and A. Asenov ^{1,2} (¹ <i>Univ. Glasgow, UK</i> , ² <i>Gold Standard Simulations Ltd., UK</i> , ³ <i>ARM Ltd., UK</i>) .. 285		
10-5	10:50–11:10	
“Simultaneous Simulation of Systematic and Stochastic Process Variations” J. Lorenz ¹ , E. Bär ¹ , A. Burenkov ¹ , P. Evanschitzky ¹ , A. Asenov ² , L. Wang ² , X. Wang ² , A.R. Brown ³ , C. Millar ³ , and D. Reid ³ (¹ <i>Fraunhofer IISB, Germany</i> , ² <i>Univ. Glasgow, UK</i> , ³ <i>Gold Standard Simulations Ltd., UK</i>) 289		
10-6	11:10–11:30	
“Variability-Aware Compact Model Strategy for 20-nm Bulk MOSFETs” X. Wang ¹ , D. Reid ² , L. Wang ¹ , A. Burenkov ³ , C. Millar ² , B. Cheng ^{1,2} , A. Lange ⁴ , J. Lorenz ³ , E. Bär ³ , and A. Asenov ^{1,2} (¹ <i>Univ. Glasgow, UK</i> , ² <i>Gold Standard Simulations Ltd., UK</i> , ³ <i>Fraunhofer IISB, Germany</i> , ⁴ <i>Fraunhofer IIS/EAS, Germany</i>) 293		
Session 11: Spintronic Devices		
Chairpersons: T. Kurusu (<i>Toshiba, Japan</i>) D. Rideau (<i>STMicroelectronics</i>)		
11-1	9:30–9:50	
“Influence of Device Geometry on the Non-Volatile Magnetic Flip Flop Characteristics” T. Windbacher, H. Mahmoudi, V. Sverdlov, and S. Selberherr (<i>TU Wien, Austria</i>) 297		
11-2	9:50–10:10	
“Extended Hückel Theory for Quantum Transport in Magnetic Tunnel Junctions” G. Shine ¹ , S. Manipatruni ² , A. Chaudhry ² , K.C. Saraswat ¹ , D.E. Nikonov ² , and I.A. Young ² (¹ <i>Stanford Univ., USA</i> , ² <i>Intel Corporation, USA</i>) 301		
10:10–10:30 <i>Coffee Break</i>		
11-3	10:30–10:50	
“0.5V Operation and Performance of Nonvolatile SRAM Cell Based on Pseudo-Spin-FinFET Architecture” Y. Shuto, S. Yamamoto, and S. Sugahara (<i>Tokyo Inst. Tech., Japan</i>) 305		
11-4	10:50–11:10	
“Interplay among Bilayer PseudoSpin Field-Effect Transistor (BiSFET) Performance, BiSFET Scaling and Condensate Strength” X. Mou, L.F. Register, and S.K. Banerjee (<i>Univ. Texas Austin, USA</i>) 309		
11:30–13:00 <i>Lunch</i>		

Session 12: Nanowire and TFT

Chairpersons: S. Yamakawa (*Sony, Japan*)
P. Oldiges (*IBM, USA*)

12-1	13:00–13:30	[invited talk]	
		“Multigate transistors: Pushing Moore’s Law to the Limit”	
		J.-P. Colinge (<i>TSMC, Taiwan</i>)	313
12-2	13:30–13:50		
		“Electron-Phonon Interaction in Si Nanowire Devices: Low Field Mobility and Self-Consistent EM NEGF Simulations”	
		G. Mil’nikov ^{1,2} and N. Mori ^{1,2} (¹ <i>Osaka Univ., Japan</i> , ² <i>JST CREST, Japan</i>)	317
12-3	13:50–14:10		
		“Single Dopant Nanowire Transistors: Influence of Phonon Scattering and Temperature”	
		H. Carrillo-Nuñez ^{1,2} , M. Bescond ¹ , E. Dib ¹ , N. Cavassilas ¹ , and M. Lannoo ¹	
		(¹ <i>IM2NP, France</i> , ² <i>ETH Zurich, Switzerland</i>)	321
12-4	14:10–14:30		
		“Channel-Size Dependent Dopant Placement in Silicon Nanowires”	
		H. Ryu ¹ , J. Kim ² , and K.-H. Hong ³	
		(¹ <i>KISTI, Korea</i> , ² <i>Samsung Advanced Inst. Tech., Korea</i> , ³ <i>Hanbat National Univ., Korea</i>)	325
12-5	14:30–14:50		
		“Comapct Modeling of Carrier Trapping for Accurate Prediction of Frequency Dependent Circuit Operation”	
		Y. Oodate, Y. Tanimoto, H. Tanoue, H. Kikuchihara, H. Miyamoto, H.J. Mattausch, and M. Miura-Mattausch (<i>Hiroshima Univ., Japan</i>)	329

Session 13: Reliability II

Chairpersons: N. Nakano (*Keio Univ., Japan*)
Y. Li (*National Chiao Tung Univ., Taiwan*)

13-1	13:30–13:50		
		“Unifying Self-heating and Aging Simulations with TMI2”	
		W.-K. Lee, K. Huang, J. Liang, J.-Y. Chen, C. Hsiao, K.-W. Su, C.-K. Lin, and M.-C. Jeng (<i>TSMC, Taiwan</i>)	333
13-2	13:50–14:10		
		“New Perspective on Lifetime Prediction Approach for BTI and HCI Stressed Device and Its Impact on Circuit Lifetime”	
		M.-C. Park ^{1,2} , G.-Y. Yang ¹ , J.-S. Yang ² , K.-H. Lee ¹ , and Y.-K. Park ¹	
		(¹ <i>Samsung Electronics, Korea</i> , ² <i>Sungkyunkwan Univ., Korea</i>)	337
13-3	14:10–14:30		
		“Three-Dimensional Simulation for the Reliability and Electrical Performance of Through-Silicon Vias”	
		L. Filipović ¹ , F. Rudolf ¹ , E. Bär ² , P. Evanschitzky ² , J. Lorenz ² , F. Roger ³ , A. Singulani ³ , R. Minixhofer ³ , and S. Selberherr ¹ (¹ <i>TU Wien, Austria</i> , ² <i>Fraunhofer IISB, Germany</i> , ³ <i>ams AG, Austria</i>)	341
13-4	14:30–14:50		
		“High-Accuracy Estimation of Soft Error Rate using PHYSERD with Circuit Simulation”	
		T. Kato, T. Uemura, and H. Matsuyama (<i>Fujitsu Semiconductor Ltd., Japan</i>)	345
	14:50–15:10	Coffee Break	

Session 14: Frontier of Simulation Methodology and Application

Chairpersons: S. Uno (*Ritsumeikan Univ., Japan*)
J. Lorenz (*Fraunhofer Institut IISB, Germany*)

14-1 15:10–15:40 [invited talk]

“Novel Biosensing Devices for Medical Applications: Soft Contact-Lens Sensors for Monitoring Tear Sugar”
K. Mitsubayashi (*Tokyo Medical and Dental Univ., Japan*) 349

14-2 15:40–16:00

“A Technique to Model the AC Response of Diffuse Layers at Electrode/Electrolyte Interfaces and to Efficiently Simulate Impedimetric Biosensor Arrays for Many Analyte Configurations”
F. Pittino and L. Selmi (*Univ. Udine, Italy*) 353

14-3 16:00–16:20

“Full-Scale Whole Device EMC/MD Simulation of Si Nanowire Transistor Including Source and Drain Regions by Utilizing Graphic Processing Units”
A. Suzuki¹, T. Kamioka², Y. Kamakura³, and T. Watanabe¹
(¹Waseda Univ., Japan, ²Toyota Tech. Inst., Japan, ³Osaka Univ., Japan) 357

14-4 16:20–16:40

“Quantum Transport in NEMO5: Algorithm Improvements and High Performance Implementation”
Y. He, T. Kubis, M. Povolotskyi, J. Fonseca, and G. Klimeck (*Purdue Univ., USA*) 361

14-5 16:40–17:00

“Cell-Centered Finite Volume Schemes for Semiconductor Device Simulation”
K. Rupp, M. Bina, Y. Wimmer, A. Jüngel, and T. Grasser (*TU Wien, Austria*) 365

17:00–17:10 Closing

N. Mori (*Osaka Univ., Japan*)