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4th December 2014

Session	A1: Wafer Level Packaging 1
Date/Time	Thursday, 4th December 2014 / 10:50 – 12:10 hrs
Venue	Orchard Main Ballroom 4301AB
Chair(s)	John Hunt

W2W Permanent Stacking for 3D System Integration

Lan Peng, Soon-Wook Kim, Michael Soules, Markus Gabriel, Margarete Zoberbier, Erik Sleeckx, Herbert Struyf, Andy Miller and Eric Beyne

- Stochastic Wire-length Model with TSV Placement on Periphery Area
 Jianhui Ling, Huiyun Li, Guoqing Xu and Liying Xiong
- Innovative Wafer Level Package Manufacturing with FlexLine TM Seung Wook Yoon, Chen Kang, Kok Hwa Lim, Kenneth Seah and Yaojian Lin

Session	A2: Emerging Technologies
Date/Time	Thursday, 4th December 2014 / 10:50 – 12:10hrs
Venue	Orchard Main Ballroom 4302
Chair(s)	Bill Chen

Extremely High Temperature and High Pressure (x-HTHP) Endurable SOI
 Device & Sensor Packaging for Deep Sea, Oil and Gas Applications
 Daniel Rhee Min Woo, Jason Au Keng Yun, Yu Jun, Eva Wai Leong Ching
 and F. X. Che

Silver Screen Printed Transmission Lines- Analyzing the Influence of Substrate Roughness on the RF Performance up to 30 GHz

Ying Ying Lim, Yee Mey Goh, Manabu Yoshida, Tung Thanh Bui, Tracey Vincent, Masahiro Aoyagi and Changqing Liu

Characterization of Copper Conductive Ink for Low Temperature Sintering Processing on Flexible Polymer Substrate

Jaewon Kim, Byunghoon Lee, Jun Yan Lek, Riko I Made, Budiman Salam and Chee Lip Gan

High Power SiC Inverter Module Packaging Solutions for Junction Temperature over 220°C

Daniel Rhee Min Woo, Hwang How Yuan, Jerry Aw Jie Li, Ho Siow Ling, Lee Jong Bum, Zhang Songbai

Session	A3: Advanced Packaging 1
Date/Time	Thursday, 4th December 2014 / 10:50 – 12:10hrs
Venue	Orchard Main Ballroom 4303
Chair(s)	Vempati Srinivas

Workability and Reliability Assessment of Various High Bandwidth PoP Structures

Mike Hung, Louie Huang, Timmy Lin, Eting Chen, Edward Huang and YC Ding

Etch-hole Design in Encapsulation for Better Robustness

Jae-Wung Lee, Jaibir Sharma, Srinivas Merugu and Navab Singh

BGA Packaging Using Insulated Wire for Die Area Reduction

Shailesh Kumar, Vikas Garg, Chetan Verma, Rishi Bhooshan, Poh Zi-Song and LC Tan

Design and Implementation of Two Different RF SiPs for Micro Base Station

Yi He, Fengman Liu, Peng Wu, Fengze Hou, Jun Li, Jie Pan, Dongkai Shangguan, Liqiang Cao

Session	A4: Quality & Reliability 1
Date/Time	Thursday, 4th December 2014 / 10:50 – 12:10hrs
Venue	Orchard Main Ballroom 4202
Chair(s)	Stevan Hunter

A Fast Passive-Heating Setup to Investigate Die-Attach Delamination in Packaged Devices

Tiphaine Pélisset, Mirko Bernardoni, Michael Nelhiebel and Thomas Antretter

Effect of Additive Elements on Crack Propagation Behavior for Sn-Bi Solders at High Temperatures

Noritake Hiyoshi, Mitsuo Yamashita and Hiroaki Hokazono

Reliability Physics and Probabilistic Design for Reliability (PDfR): Role, Attributes, Challenges

E. Suhir

Session	A5: Materials & Processes 1
Date/Time	Thursday, 4th December 2014 / 10:50 – 12:10hrs
Venue	Orchard Main Ballroom 4203
Chair(s)	Loke Yuen Wong

Interfacial Microstructure and Shear Strength of Sn-Ag-Cu Based Composite Solders on Cu and Au/Ni Metallized Cu Substrates

Tama Fouzder, Y. C. Chan and Daniel K. Chan

Challenges and Solutions on Pre-Assembly Processes for Thinned 3D Wafers with Micro-bumps on the Backside

A. Podpod, C. Demeurisse, C. Gerets, K. J. Rebibis, G. Capuz, F. Duval, A. Phommahaxay, E. Sleeckx, H. Struyf, R. A. Miller, G. Beyer and E. Beyne

Low Stress Die Attach Material Challenges for Critical Si Node with Cu Wire

Megan Chang and Anderson Li

The Study of Adhesive Performance Within Backside-Via Revealing H. Y. Li, L. Ding and G. Q. Lo

Session	B1: Interconnection Technologies 1
Date/Time	Thursday, 4th December 2014 / 14:00 – 15:20hrs
Venue	Orchard Main Ballroom 4301AB
Chair(s)	Hong Meng Ho

Advanced Electrical Array Interconnections for Ultrasound Probes Integrated in Surgical Needles

Giuseppe Schiavone, Thomas Jones, Dennis Price, Rachael McPhillips, Zhen Qiu, Christine E. M. Demore, Yun Jiang, Carl Meggs, Syed O. Mahboob, Sam Eljamel, Tim W. Button, Sandy Cochran and Marc P. Y. Desmulliez

Sintering of Ag Paste for Power Devices Die Attach on Cu Surfaces
 Vemal Raja Manikam and Erik Nino Tolentino

Bondability and Challenges of Cu Ultra-Fine-Wire Bonding

Sylvia Sutiono, Zhangxi, Tok Chee Wei, Don Syth An, Murali Sarangapani, Louie Huang, Jason Hung and Frank Lin

Breakthrough Development of Ultimate Ultra-Fine Pitch Process with Gold Wire & Copper Wire in QFN Packages

C. E.Tan , J. Y. Liong , Jeramie Dimatira , Lee Wee Kok , Jason Tan, Lie Handra Wijaya, James Song , Teshima Satoshi and K. H. Kwong

Session	B2: Electrical Modelling 1
Date/Time	Thursday, 4th December 2014 / 14:00 – 15:20hrs
Venue	Orchard Main Ballroom 4302
Chair(s)	Wui Weng Wong

A Low-Cost, High Efficiency Power Architecture Map for Basic and Performance Level Tablet Computers

Suvankar Biswas and Ripan Das

Measurement of Power Distribution Network Impedance Using an Error Analysis Approach

Eng-Kee Chua, Xing-Ming Li, Shan-Qing Hu and Kye-Yak See

Vertical Interconnections using Through Encapsulant Via (TEV) and Through Silicon Via (TSV) for High-Frequency System-in-Package Integration

M. Wojnowski, K. Pressel, G. Beer, A. Heinig, M. Dittrich and J. Wolf

Capacitive Crosstalk Compensation Structure for Improved High-Speed On-Package Signaling

Bok Eng Cheah, Jackson Kong, Ping Ping Ooi, Kok Hou Teh and Po Yin Yaw

Session	B3: Advanced Packaging 2
Date/Time	Thursday, 4th December 2014 / 14:00 – 15:20hrs
Venue	Orchard Main Ballroom 4303
Chair(s)	John Oviso

Air-Gap in Encapsulation for Fast Release and Safe Sealing Jae-Wung Lee, Srinivas Merugu, Jaibir Sharma, Geng Li and Navab Singh

- The Study of High-Lead Solder Joints Reliability of Flip Chip Devices
 Lingjuan Tian, Yuanfu Zhao, Quanbin Yao, Yusheng Cao and Binhao Lian
- Elongated Copper Pillar Bump Flip Chip Design on Molded Interconnect
 Substrate (MIS) for Advanced Flip Chip Packages

Ho Siow Ling, Sherryll Alialy, Stephenie, Zhang Xiaowu and Raymond Shoa Siong Lim

Structure Reliability and Characterization for FC Package w/ Embedded Trace Coreless Substrate

Eason Chen, Albert Lan, Jack You and Mark Liao

Session	B4: Quality & Reliability 2
Date/Time	Thursday, 4th December 2014 / 14:00 – 15:20hrs
Venue	Orchard Main Ballroom 4202
Chair(s)	Tong Yan Tee

Development of Scanning Acoustic Microscopy Method with Passive
 Integration Package for Mass Production Monitoring

C.T. Tai, C.Y. Lai and Subramanian Eswariy

- Intermetallic Compound Growth Mechanism and Failure Modes of Flip Chip Solder Bump with Different UBM Structure during Electromigration Yong-Sheng Zou, Yu-Hsiang Hsiao and Kwang-Lung Lin
- Analysis of Silicone-Based Adhesive Bond Separation
 L. E. Khoong , T. K. Gan and M. B. Young

Copper Ball Bond Shear Test for Two Pad Aluminum Thicknesses

Derek Andrews, Levi Hill, Aaron Collins, Kok Inn Hoo and Stevan Hunter

Session	B5: Materials & Processes 2
Date/Time	Thursday, 4th December 2014 / 14:00 – 15:20hrs
Venue	Orchard Main Ballroom 4203
Chair(s)	L. C. Tan

- Flip Chip Die Attach Flux Evaluation Method
 Adam Liu, Tank Lo, James Li, Eason Chen, JZ Yang and CT Chen
- Simultaneously Obtaining the Young's Relaxation Modulus and Shear Relaxation Modulus of an Epoxy Molding Compound by Using DMA Dao-Long Chen, Tz-Cheng Chiu, Tei-Chen Chen, Ping-Feng Yang, Chih-Pin Hung and Jen-Kuang Fang
- Picking Large Thinned Dies with High Topography on Both Sides

Carine Gerets, Jaber Derakhshandeh, Teng Wang, Giovanni Capuz, Arnita Podpod, Caroline Demeurisse, Kenneth June Rebibis, Andy Miller, Gerald Beyer and Eric Beyne

Session	C1: Quality & Reliability 3
Date/Time	Thursday, 4th December 2014 / 15:50 – 16:50hrs
Venue	Orchard Main Ballroom 4301AB
Chair(s)	Che Faxing

An Alternative Methodology of Determining the Package Delamination
 Failure Starting Point Using the Thermomechanical Analyzer

Aaron D. Cadag and Bernie Chrisanto M. Ang

Towards Adequate Qualification Testing of Electronic Products: Review and Extension

G. Khatibi, B. Czerny, J. Magnien, M. Lederer, E. Suhir and J. Nicolics

Session	C2: Wafer Level Testing
Date/Time	Thursday, 4th December 2014 / 15:50 – 16:50hrs
Venue	Orchard Main Ballroom 4302
Chair(s)	Bruce Kim

Thickness Dependency of Adhesion Properties of TiW Thin Films A. Roshangias, R. Pelzer, G. Khatibi and J. Steinbrenner

Concurrent System Level Test (CSLT) Methodology for Complex Systemon-Chip

Dilip Kumar Reddy Tipparthi and Karthik Krishna Kumar

Session	C3: Advanced Packaging 3
Date/Time	Thursday, 4th December 2014 / 15:50 – 16:50hrs
Venue	Orchard Main Ballroom 4303
Chair(s)	Yew Cheong Mui

Flip Chip Packaging with Pre-Molded Coreless Substrate

Tom Tang, Albert Lan, Jensen Tsai, Ivan Chang and Evan Chen

- Study on Electrical Characteristics for Active Die Embedding Substrate Hyunho Kim
- Temporary Handling Technology for Advanced Wafer Level Packaging Applications Based on Adhesive Bonding and Laser Assisted De-Bonding Kai Zoschke, Thorsten Fischer, Hermann Oppermann and Klaus-Dieter Lang

Session	C4: Interconnection Technologies 2
Date/Time	Thursday, 4th December 2014 / 15:50 – 16:50hrs
Venue	Orchard Main Ballroom 4202
Chair(s)	Eric Yong

Manufacturability Readiness of Insulated Cu Wire Bonding Process in PBGA Package

Leong HungYang , Yap BoonKar, Tan Chou Yong, Navas Khan, Mohd Rusli Ibrahim, L. C. Tan

Wirebond Enhancement on Copper Palladium Bonding in a Over Pad Metalization

Michael B. Tabiera, Bryan Christian S. Bacquian and Terencio D. Lacuesta

Process Development and Optimization for High Temperature Endurable
 Flip Chip Interconnection in SiC High Power Module

Jie Li Aw, Bu Lin, Hwang How Yuan and Daniel Rhee Min Woo

Session	C5: Materials & Processes 3
Date/Time	Thursday, 4th December 2014 / 15:50 – 16:50hrs
Venue	Orchard Main Ballroom 4203
Chair(s)	Alvin Lee

 High Temperature Die Attach Material on ENEPIG Surface for High Temperature (250DegC/500hour) and Temperature Cycle (-65 to +150DegC) Applications

Leong Ching Wai, Seit Wen Wei, Hwang How Yuan and Daniel Rhee MinWoo

- Functionalised Copper Nanoparticles as Catalysts for Electroless Plating
 R. E. Litchfield, J. Graves, M. Sugden, D. A. Hutt and A. Cobley
- Fabrication and Characterization of Gold-Tin Eutectic Bonding for Hermetic Packaging of MEMS Devices
 Eyup Can Demir, M. Mert Torunbalci, Inci Donmez, Y. Eren Kalay and Tayfun Akin

Poster Session 1

New Process Flow to Make QFN Package with Stand-Off Peng Liu, Ping Wu and Q. C. He

60GHz Wideband Yagi-Uda Antenna Integrated on 2.5D Through Silicon Interposer

Songbai Zhang, Ka Fai Chang, Cheng Jin, Guruprasad Katti, Roshan Weerasekera and Surya Bhattacharya

- Embedded Compact BaTiO 3 -Polymer Film VHF Band-Pass Filter Wenhu Yang, Shuhui Yu, Rong Sun and Wei-Hsin Liao
- A Compact and Low-profile GaN Power Amplifier Using Interposer-Based MMIC Technology

Dongsu Kim, Jong Min Yook, Sung Jin An, Sung Ryul Kim, Jong-Gwan Yook and Jun Chul Kim

Through Silicon via (TSV) Scallop Smoothening Technique

Goon Heng Wong, Guan Kian Lau, King Jien Chui and Woon Leng Loh

2.5D Through Silicon Interposer Package Fabrication by Chip-on-Wafer
 (CoW) Approach

S. W. Ho, Mian Zhi Ding, Pei Siang Lim, Daniel Ismail Cereno, Guruprasad Katti, Tai Chong Chai and Surya Bhattacharya

Fabrication of Dielectric Insulation Layers in TSV by Different Processes Zhenzhong Yong, Hengfu Li and Wenqi Zhang

Novel Spray Coating Process with Polymer Material Applied in CIS Wafer-Level-Packaging

Yuechen Zhuang, Daquan Yu, Fengwei Dai, Zhongcai Niu, Wenqi Zhang and Guoping Zhang

- Development of Fluxless Bonding Using Deposited Gold-Indium Multi-Layer Composite for Heterogeneous Silicon Micro-Cooler Stacking
 B. L. Lau, Yong Han H. Y. Zhang, L. Zhang and X. W. Zhang
- Performance of Electrically Conductive Adhesive Attached Sensors in High Temperature Cycling

Sanna Lahokallio and Laura Frisk

 Study of Intermetallic Compound Growth and Failure Mechanisms in Long Term Reliability of Silver Bonding Wire

You Cheol Jang, So Yeon Park, Hyoung Dong Kim, Yeo Chan Ko, Kyo Wang Koo, Mi Ri Choi, Hyung Giun Kim, Nam Kwon Cho, Tae Kang, Jae Hak Yee, Sung Hwan Lim

Electrical Measurement and Analysis of TSV/RDL for 3D Integration Xin Sun, Runiu Fang, Yunhui Zhu, Xiao Zhong, Yuan Bian, Shenglin Ma, Min Miao, Jing Chen, Yan Wang and Yufeng Jin

Integrated Electronic and Microfluidic Packaging for CMOS Biosensor Chip

Mian Zhi Ding, Chaitanya Kantak, Vempati Srinivasa Rao, Mi Kyoung Park and Chee Chung Wong

- Biocompatible Packaging for Implantable Miniaturized Pressure Sensor Device used for Stent Grafts: Concept and Choice of Materials Sabine Kirsten, Martin Schubert, Markus Braunschweig, Gregor Woldt, Tetiana Voitsekhivska, Klaus-Jürgen Wolter
- Package Characterization of FET-Based Biochemical Sensors Tetiana Voitsekhivska, Eike Suthau, Sabine Kirsten, Martin Schubert, Felix Zörgiebel, Gianaurelio Cuniberti and Klaus-Jürgen Wolter
- Inkjet Printed Transmission Line Elements for RF Applications and Measurement Challenges

Nishshanka Bandara Narampanawe, See Kye Yak and Zhang Jie

One-Sided Directional Slot Antenna with Impedance Matching Circuit for
 3D Packaging

Haruichi Kanaya, Naoto Iizasa and Tomoki Oda

Sequential Stress Combinations in Product Level Reliability Testing of Industrial Electronics

J. Pippola, T. Marttila and L. Frisk

How to Improve Void Performance in Wafer Bumping

Zhang Ruifen, Yap Kong Tat, Yam Lip Huei and Reynoso Dexter

 Optimization of the Wafer Level Molding Process for High Power Device Module

Lin Bu, Siow Ling Ho, Sorono Dexter Velez and Daniel Rhee Min Woo

- Single & Multi Beam Laser Grooving Process Parameter Development and Die Strength Characterization for 40nm Node Low-K/ULK Wafer Koh Wen Shi, K. Y. Yowand Calvin Lo
- Joint Strength and Microstructures of Brazed Joints of Stainless Steel with Fe-based Filler

Takahiro Tsunoda, Kangdao Shi, Ikuo Shohji, Kotaro Matsu and Yasuhiro Taguchi

5th December 2014

Session	D1: Advanced Packaging 4
Date/Time	Friday, 5th December 2014 / 08:30 – 10:10hrs
Venue	Orchard Main Ballroom 4301AB
Chair(s)	Bok Eng Cheah

- Electrical Performance Characterization for Novel Multiple
 Compartments Shielding and Verification on LTE Modem SiP
 Albert Lin, Vincent Chen, JJ Chen, Simon Leou, Thomas Wang and Harrison
 Chang
- Alternative Package-on-Package with Organic Substrate Interposer for Stacking Packaging Solution

Steven Lin, Mark Liao, Albert Lan and David Wang

- Photonic Device Package Design, Assembly and Encapsulation J. Hamelink and A. Bos
- Ultrahigh Speed Transceiver Package with Stacked Silicon Integration
 Technology

Hong Shi

Session	D2: Electrical Modelling 2
Date/Time	Friday, 5th December 2014 / 08:30 – 10:10hrs
Venue	Orchard Main Ballroom 4302
Chair(s)	Weerasekera Roshan

Integrated Passive Devices on Through Silicon Interposer with Redistribution Layers

Cheng Jin, Guruprasad Katti and Songbai Zhang

Capacitor Selection Process for High-Speed Power Distribution Network Based on Switching Current Requirement

Xing-Ming Li, Shan-Qing Hu, Kye-Yak See and Eng-Kee Chua

Segmented Plated-Thru-Hole Design in Flip-Chip Packaging for Improved Electrical Performance

Jackson Kong, Bok Eng Cheah, Chin Lee Kuan and Ping Ping Ooi

Electromagnetic Modelling and Simulation of TSVs in 2.5D Interposers for RFICs

Kaushal Kannan and David Crouse

Study of Transmission Line Performance on Through Silicon Interposer Ka Fai Chang, Rui Li, Liang Ding and Songbai Zhang

Session	D3: Mechanical Modelling 1
Date/Time	Friday, 5th December 2014 / 08:30 – 10:10hrs
Venue	Orchard Main Ballroom 4303
Chair(s)	Andrew Tay

Comprehensive Study on Reliability of Chip-Package Interaction Using Cu Pillar Joint onto Low k Chip

F. X. Che, Jong-Kai Lin, K. Y. Au and Xiaowu Zhang

Evaluating the Optimal Location for Embedded Accelerometers using Experimentally Validated Computer Algorithms

Guy Banwell, Richard Sharpe, Paul Conway and Andrew West

Wirebondability Enhancement for Very Small Die in Power Packages with Dynamic Simulation

Xueren Zhang, Kim-yong Goh, Yiyi Ma, Tito Verano, Raquel Fundan, Wingshenq Wong and Loic Renard

Unit Warpage Control with Universal Die Thickness

Gu Bin, Jun Dimaano Jr., Richen Chen, Eric Bool, Seow Fui Shi, Choon Ghee Ang and Nathapong Suthiwongsunthorn

Thermal Effects of TSV (Through Silicon via) with Void

Yunna Sun, Hui-Yeol Kim, Yan Wang, Guifu Ding, Junhong Zhao and Hong Wang

Session	D4: Wafer Level Packaging 2
Date/Time	Friday, 5th December 2014 / 08:30 –10:10hrs
Venue	Orchard Main Ballroom 4202
Chair(s)	Yoon Seung Wook

Cu-Cu Insertion Bonding Technique Using Photosensitive Polymer as WLUF

G. Potoms, W. Teng, J. Derakhshandeh, R. Daily, G. Capuz, M. Gonzalez, G. Beyer, K.J. Rebibis, R. A. Miller and E. Beyne

Process Development of Multi-Die Stacking Using 20 um Pitch Micro Bumps on Large Scale Dies

Lee Jong Bum, Jerry Aw Jie Li and Daniel Rhee Min Woo

Tunable 3D TSV-Based Inductor for Integrated Sensors

Bruce Kim, Saikat Mondal and Seok Ho Noh

Wafer to Wafer Bonding Using CuSn Microbumps for GaN-LED Substrate Transfer Process

Nga. P. Pham, Philippe Soussan, Lan Peng, Maarten Rosmeulen and Deniz Sabuncuoglu

Session	D5: Thermal Characterization & Cooling Solutions 1
Date/Time	Friday, 5th December 2014 / 08:30 – 10:10hrs
Venue	Orchard Main Ballroom 4203
Chair(s)	Rathin Mandal

Package-Level Si-Based Micro-Jet Impingement Cooling Solution With Multiple Drainage Micro-Trenches

Yong Han, Boon Long Lau, Hengyun Zhang and Xiaowu Zhang

Experimental Characterization of Si Micropillar Based Evaporator for Advanced Vapor Chambers

Mengyao Wei, Sivanand Somasundaram, Bin He, Qian Liang, Chuan Seng Tan and Evelyn N. Wang

The Effect of Variation of Doping Density on Thermal Properties of Power Si MOSFET

Risako Kibushi, Tomoyuki Hatakeyama, Shinji Nakagawa and Masaru Ishizuka

Comparative Analysis of Novel Thermal Interface Containing Nano Additives

Przemysaw Matkowski, Tomasz Faat and Andrzej Mościcki

Design Considerations on the External Heat Exchanger for Cooling of Microelectronic Devices

H. Y. Zhang, X. W. Zhang, Y. Han, B. L. Lau, Hector Valladares, Hikmat Chammasand and Bruce Bolliger

Session	E1: Quality & Reliability 4
Date/Time	Friday, 5th December 2014 / 10:40 – 12:20hrs
Venue	Orchard Main Ballroom 4301AB
Chair(s)	John Pang

 Experimental Study of Water Absorption of Electronic Components and Internal Local Temperature and Humidity into Electronic Enclosure Héléne Conseil, Morten S. Jellesen and Rajan Ambat

Thermal and Mechanical Reliability of Low-Temperature Solder Alloys for Handheld Devices

Morgana Ribas, Sujatha Chegudi, Anil Kumar, Ranjit Pandher, Rahul Raut, Sutapa Mukherjee, Siuli Sarkar and Bawa Singh

Sensor-Enabled PCBs to Aid Right First Time Manufacture Through Defect Prediction

Richard Sharpe, Guy Banwell, Paul P. Conway and Andrew A. West

Growth Behavior and Physical Response of Al-Cu Intermetallic Compounds

Rainer Pelzer, Stefan Woehlert, Heinrich Koerner, Golta Khatibi and Juergen Walter

Session	E2: Materials & Processes 4
Date/Time	Friday, 5th December 2014 / 10:40 – 12:20hrs
Venue	Orchard Main Ballroom 4302
Chair(s)	Ernest Leo

Temporary Bonding on the Move Towards High Volume: A Status Update on Cost-Of-Ownership

Thomas Uhrmann, Jürgen Burggraf, Harald Wiesbauer, Julian Bravin, Thorsten Matthias, Markus Wimplinger and Paul Lindner

Influence of the Height of Carbon Nanotubes on Hot Switching of Au/Cr-Au/MWCNT Contact Pairs

H. Liu, A. P. Lewis, S.H. Pu, L. Jiang, J. W. McBride

Plasma Technology Optimization for a Robust Flip Chip Package

Jesus B. Bautista, Ma. Jean Krisca N. Blas, Erma G. Gardose, Antonio R. Taloban, Jr and Vikas Gupta

Thermo-Compression Bonding for 2.5D Fine Pitch Copper Pillar Bump Interconnections on TSV Interposer

Sharon Pei-Siang Lim, Mian Zhi Ding, Sorono Dexter Velez, Daniel Ismael Cereno, Jong Kai Lin and Vempati Srinivasa Rao

Wafer Level Underfill Study for High Density Ultra-fine Pitch Cu-Cu Bonding for 3D IC Stacking

Ling Xie, Sunil Wickramanayaka, Boo Yung Jung, Jerry Aw Jie Li, Lim Jung-Kai and Daniel Ismael

Session	E3: Mechanical Modelling 2
Date/Time	Friday, 5th December 2014 / 10:40 – 12:20hrs
Venue	Orchard Main Ballroom 4303
Chair(s)	Xueren Zhang

- Board Level Drop Test Simulation Using Explicit and Implicit Solvers
 Yiyi Ma, Kim-Yong Goh and Xueren Zhang
- Finite Strain Thermomechanical Material Characterization of Adhesives
 Used in Automotive Electronics for Quantitative Finite Element
 Simulations

B. Öztürk, P. Gromala, C. Silber, K. M. B. Jansen and L. J. Ernst

Chip Scale Package with Low Cost Substrate Evaluation and Characterization

Vito Lin, Vincent Lin, Nicholas Kao, Don Son Jiang and C. S. Hsiao

Over-Acceleration of Corrosion Mechanisms During Reliability Testing: A Method to Relate Biased HAST Tests and Application Conditions for Cu Wire Products

J. J. M. Zaal, A. Mavinkurve, R. Rongen, J. H. J. Janssen and P. Drummen

Effect of Thermo-Mechanical Excursions on Growth of Interfacial Intermetallic Compounds in Cu/Sn-Ag-Cu Solder Joints

Rituparna Ghosh, Praveen Kumar and Abha Misra

Session	E4: Advanced Packaging 5
Date/Time	Friday, 5th December 2014 / 10:40 – 12:20hrs
Venue	Orchard Main Ballroom 4202
Chair(s)	Chen Zhaohui

Thermal Compression Bonding with Non-Conductive Adhesive of 30μm
 Pitch Cu Pillar Micro Bumps on Organic Substrate with Bare Cu
 Bondpads

Jie Li Aw, Alvin Chow, K. Y. Au and Jong-Kai Lin

Reliability of 3D Package Using Wafer Level Underfill and Low CTE Epoxy Mold Compound Materials

F. Cadacio, K. J. Rebibis, G. Capuz, R. Daily, C. Gerets, F. Duval, T. Wang, R. A. Miller, G. Beyer and E. Beyne

New Nano Size Filled TIM Material With High Thermally Conductive Properties

A. Mościcki, T. Faat, A. Kinart, A. Smolarek and E. Merten

Microbumping Technology for Hybrid IR Detectors, 10µm Pitch and Beyond

B. Majeed, P. Soussan, P. Le Boterf and P. Bouillon

Session	E5: Interconnection Technologies 3
Date/Time	Friday, 5th December 2014 / 10:40 – 12:20hrs
Venue	Orchard Main Ballroom 4203
Chair(s)	Liming Shen

- Sinter Paste for Power Packages Yong Ling Xin
- Application and High Temperature Storage Test on Zn-Al-Ge High Temperature Solder for Die Attach

Pan Wei Chih, Baquiran Joseph Aaron Mesa, Xie Hong and Goh Min Hao

- A 24 GHz Microstrip Grid Array Antenna Excited by Coaxial-Fed Slot Zihao Chen and Yue Ping Zhang
- Study of 0.6mil Silver Alloy Wire in Challenging Bonding Processes
 Jie Wu, Jeong-Ho Yang, Oranna Yauw, Ivy Qin, Tom Rockey and Bob Chylak
- Highly Efficient Packaging Processes by Reactive Multilayer Materials for Die-Attach in Power Electronic Applications
 Martin Mueller and Joerg Franke

Session	F1: Advanced Packaging 6
Date/Time	Friday, 5th December 2014 / 14:10 – 15:30hrs
Venue	Orchard Main Ballroom 4301AB
Chair(s)	En-Xiao Liu

Chip Package Interaction Induced ILD Integrity Issues in Fine Pitch Flip Chip Packages

Vikas Gupta, Shawn O'Connor and Charles Pilch

Gold-Germanium Laser Jetting for High Temperature (300°C) Flip Chip Application

Hwang How Yuan, Ding Mian Zhi and Daniel Rhee Min Woo

Advanced Thermocompression Flip Chip Bonding

Horst Clauberg, Alireza Rezvani, Evan Galipeau, Matt Wasserman, Tom Colosimo, Guy Frick, Daniel Buergi and Bob Chylak

Package characterization of UTAC's Grid Array Package (GQFN) and Performance Comparison over Standard Laminate Packages

Daniel Ting Lee The, Carolyn Epino Tubillo, Kyaw Ko Lwin, Gu Bin, Ang Choon Ghee, Jun Dimaano, Saravuth Sirinorakul and Nathapong Suthiwongsunthorn

Session	F2: Quality & Reliability 5
Date/Time	Friday, 5th December 2014 / 14:10 – 15:30hrs
Venue	Orchard Main Ballroom 4302
Chair(s)	James How

Thermal Cycling Reliability of SnAgCu Solder Joints in WLCSP Kejun Zeng and Amit Nangia

An Automatic Visual System to Identify and Estimate Ionic
 Contamination in Printed Circuit Boards Using Electrochemical Migration
 Patterns

Helen S. Villanueva, Manolo G. Mena and Prospero C. Naval

The IMC Formation and Progress in the Copper Pillar Cu/Sn1.8Ag /OSP Cu Microbump Structure upon Current Stressing

Chiao-Wen Chen, Kwang-Lung Lin, Ying-Ta Chiu, Chin-Li Kao, Chiu-Wen Lee and Ping-Feng Yang

Leadfree Solder Joint Improvement Study

Anocha Sriyarunya AND Jiraporn Tondtan

Session	F3: Interconnection Technologies 4
Date/Time	Friday, 5th December 2014 / 14:10 – 15:30hrs
Venue	Orchard Main Ballroom 4303
Chair(s)	Mohandass Sivakumar

Basic Evaluation of Au Micro-Bumps Formed by Cyanide-Free Electroless Au Plating Process

Naoya Watanabe, Shunsuke Nemoto, Katsuya Kikuchi, Masahiro Aoyagi, Tomoaki Tokuhisa, Takuo Owada and Masaru Kato

Electrical Performance of Isotropic Conductive Adhesives with Copper and Copper Coated Iron Fillers

Junpeng Liu, Richard Redei, Siyuan Qi, David A. Hutt and David Whalley

Fabrication of VGA Size Near-Infrared Image Sensor Using Room-Temperature Flip-Chip Bonding Technology

Takanori Shuto, Keiichiro Iwanabe, Mutsuo Ogura, Katsuhiko Nishida and Tanemasa Asano

Magnetically Responsive SAC305 Solder for Precison Melting Applications

Gopala Krishnan R.. Yiteng Lin, Xu Ke, Justin Zhou Yong, Eng Soon Tok, Yaadhav Raaj and Srayes G

Session	F4: Materials & Processes 5
Date/Time	Friday, 5th December 2014 / 14:10 – 15:30hrs
Venue	Orchard Main Ballroom 4202
Chair(s)	Lau Boon Long

Laminating Thin Glass Onto Glass Carrier to Eliminate Grinding and Bonding Process for Glass Interposer

Leon Tsai, Bor Kai Wang, Aric Shorey, Alvin Lee, Jay Su, Baron Huang, Wen-Wei Shen, Hsiang-Hung Chang and C. H. Chien

Influence of Mold Compound Type Towards Palladium Doped and Copper Doped 2N Au wire

Goh Chen Liew, Khoo Ju Lee and Manantan Soriano Aileen

Characterization of Dicing Tape Adhesion for Ultra-thin Die Pick-up Process

Jun Dimaano, Saravuth Sirinorakul and Nathapong Suthiwongsunthorn

Novel Smart Ferroelectric Functional Material for Application in Transducers

R. Islam, M. A. Matin, R. Mahbub, M. A. Hakim and M. F. Islam

Session	F5: Advanced Packaging 7
Date/Time	Friday, 5th December 2014 / 14:10 – 15:30hrs
Venue	Orchard Main Ballroom 4203
Chair(s)	Han Yong

Advanced Interconnect Equipment and Process Development

Tao Xu, Todd Walker, Raymond Chen, Jason Fu and Christoph Luechinger

Power QFN Down Bond Lift and Delamination Study

Hanmin Zhang, M. Hu, Sonder Wang, Schmadlak Ilko, B. G. Yin, Q. C. He and D. H. Ye

Thermo-Compression Bonding Assembly Process and Reliability Studies of Cu Pillar Bump on Cu/Low-K Chip

K. Y Au, F. X Che, Jie Li Aw, Jong-Kai Lin, Bjoern Boehme and Frank Kuechenmeister Room Temperature and Zero Pressure High Quality Oxide Direct Bonding for 3D Self-Aligned Assembly

Vikas Dubey , Stefaan Van Huylenbroeck, Nina Tutunjyan, John Slabbekoorn, Ingrid De Wolf ,Kenneth June Rebibis, Andy Miller, Jean Pierre Celis and Eric Beyne

Session	G1: Quality & Reliability 6
Date/Time	Friday, 5th December 2014 / 16:00 – 17:20hrs
Venue	Orchard Main Ballroom 4301AB
Chair(s)	Ho Xininig

Aging Effect on Creep Properties of SnBi Solders

Masao Sakane, Kota Yagi, Takamoto Itoh, Mitsuo Yamashita and Hiroaki Hokazono

Alternative Flip Chip Sample Preparation Technique Using Triple Ion Beam Milling

W. Qiu, B. Zee, F. J. Foo and W. Grünewald

Accelerated Testing of Multi-Walled CNT Composite Electrical Contacts for MEMS Switches

Adam P. Lewis, John W. McBride, Suan Hui Pu and Liudi Jiang

Session	G2: Advanced Packaging 8
Date/Time	Friday, 5th December 2014 / 16:00 – 17:20hrs
Venue	Orchard Main Ballroom 4302
Chair(s)	David Hutt

Development of Low Profile Fan Out PoP Solution with Embedded Passive

Boo Yang Jung, David Soon Wee Ho, Dexter Velez Sorono, Sharon Pei Siang Lim, Zhaohui Chen, Han Yong, Bu Lin and Chai Tai Chong

- Performance and Reliability Study of TGV Interposer in 3D Integration Tiwei Wei, Qian Wang, Jian Cai, Le Chen, Jones Huang, Lu Wang, Long Zhang and Cheng Li
- Development of Ruggedized Timer and Temperature Sensor Packaging for 300°C/30kpsi Downhole Environment

Hwang How Yuan, Haridas Kuruveettil, Eva Wai Leong Ching, Eric Phua Jian Rong, Gan Chee Lip and Daniel Rhee Min Woo

Insulated PdCu Wire Bond Challenges and Resolution for HVM Robustness

Siong Chin Teck, Eu Poh Leng, Tan Lan Chu, Mohd Rusli Ibrahim, Au Ying Kheng, Yow Kai Yun, Zhang Xi, Cheryl Lee, Su Dan, Tok Chee Wei, Sarangapani MuraliRobert Lyn

Session	G3: Thermal Characterization & Cooling Solutions 2
Date/Time	Friday, 5th December 2014 / 16:00 – 17:20hrs
Venue	Orchard Main Ballroom 4303
Chair(s)	Marta Rencz

Thermal Modeling and Characterization of SiC Power Module Under
 Both Air Cooling and Liquid Cooling Conditions

Hengyun Zhang, How Yuan Hwang, Lin Bu, Jerry Jie Li Aw and Daniel Min Woo Rhee

Processing of Metallic Thermal Interface Materials Using Liquid Phase
 Sintering Followed by Accumulative Roll-Bonding

Rajesh Kumar Tiwari, Deepak Sharma, Rohan Sharma and Praveen Kumar

Methodology for More Accurate Assessment of Heat Loss in Microchannel Flow Boiling

Mrinal Jagirdar and Poh Seng Lee

Session	G4: Materials & Processes 6
Date/Time	Friday, 5th December 2014 / 16:00 – 17:20hrs
Venue	Orchard Main Ballroom 4202
Chair(s)	Melvin Tan Siow Pin

Interfacially Engineered Micro and Nano-Scale Cu-In Composites as High
 Performance Thermal Interface Materials for Advanced Electronics

I. Dutta, J. Liu, K. Mireles, P. Kumar and L. Meinshausen

Inter-Connecting Process Investigation to Resolve Delamination
 Bob Lee and Stanley Chou

Enhanced Stitch Bonding Concept for QFN Package's Cu Wirebonding Process

Allen M. Descartin, Zhang XiaoLong, Sun Deguo, Li Jun and Yan BeiYue

Session	G5: Quality & Reliability 7
Date/Time	Friday, 5th December 2014 / 16:00 – 17:20hrs
Venue	Orchard Main Ballroom 4203
Chair(s)	Zhao Huapeng

 Analysis of Concurrent Failure Mechanisms in IGBT Structures During Active Power Cycling Tests

Zoltan Sarkany, Andras Vass-Varnai and Marta Rencz

Test Methods and Influencing Factors for the Adhesion Strength Measurement of Metallized Structures on Thermoplastic Substrates Thomas Kuhn and Joerg Franke

Poster Session 2

- A Robust Chip Capacitor for Video Band Width in RF Power Amplifiers Aznita Abdul Aziz, Frank Danaher and Anigah Hashim
- Comparison of Aluminum Post Etch Cleaning on MEMS Structures Using Formulated Organic Solvent Cleaners

Lee Hou Jang Steven, Vladimir Bliznetsov, Deng Wei, Tham Dexian and Sunil Wickramanayaka

Optimization Studies of Lift-Off Methods and its Application in Electrochemical Biosensors

Leong Yew Wing, Zhang ShiYun, Christopher Pang, Mohammad Hazren, Sunil Arya Kumar and Wong Chee Chung

- Considerations for Package Routing for DRAM and NAND Flash Memory Wang Ai-Chie and Chong Chin Hui
- Effect of Temperature on Tensile Properties of High-melting Point Bi System Solder

Haidong Zhang, Ikuo Shohji, Masayoshi Shimoda and Hirohiko Watanabe

- Mechanical Properties of Low-Silver Sn-1.0Ag-0.7Cu-1.6Bi-0.2In Solder Yuki Takahashi and Ikuo Shohji
- Tensile Properties of Low-melting Point Sn-Bi-Sb Solder
 Yuto Kubota, Ikuo Shohji, Tetsuyuki Tuchida and Kiyotomo Nakamura
- Effect Of Copper Roughness On Dielectric Adhesion
 Serine Soh Siew Boon, David Ho SW, Ding Liang and Sek Soon Ann

Experimental Results Versus Numerical Simulations of In/Cu Intermetallic Compounds Growth

Tomasz Faat, Bartosz Patek, Przemysaw Matkowski, Jan Felba, Carl Zendén, Li-lei Ye and Johan Liu

Influence of Sintering Process Parameters on Mechanical Strength of Joints Based on Silver Nano Particles

Tomasz Faat, Krzysztof Stojek, Przemysaw Matkowski, Bartosz Patek, Jan Felba and Andrzej Mościcki

- Power Noise Isolation in a Silicon Interposer with Through Silicon Vias Myunghoi Kim, Dong-Hwan Shin, Man-Seok Um and In-Bok Yom
- Embedded Filter Based on the BaTiO 3 -epoxy Composite Film Wenhu Yang, Shuhui Yu, Wei-Hsin Liao and Rong Sun
- Thermo-mechanical Reliability Study on Package on Package (PoP) with Embedded Wafer Level Package (eWLP)

Zhaohui Chen, Boo Yang Jung, Sharon Pei Siang Lim, Sorono Velez Dexter, David Soon Wee Ho and Xiaowu Zhang

MoldFlow Simulation Study on Void Risk Prediction for FCCSP with Molded Underfill Technology

Freedman Yen, Leo Hung, Nicholas Kao and Don Son Jiang

Mechanical Modeling and Characterization of Silicon Micro Cooler
 F. X. Che, Yong Han, Boon Long Lau, Hengyun Zhang, Lu Zhang and Xiaowu
 Zhang

Application of Transmission EBSD on High Topography Surface Aluminum Thin Film

S. Y. Zhang, Y. J. Zhang, W. M. Kwek, L. S.Goi, A. D. Trigg and L. J. Tang

Heat Conduction Study Across Metal/graphene Interface by Molecular Dynamics

Fulong Zhu, Kai Tang, Ying Li, Ke Duan, Sheng Liu and Yanming Chen

Thermal Analyses of Package-on-Package (PoP) Structure for Tablet Application

Miaowen Chen, Leo Huang, George Pan, Nicholas Kao and Don Son Jiang

Study of Electromigration Behavior of Cu Pillar with Micro Bump on Fine Pitch Chip-To-Substrate Interconnect

Hsiao Hsiang Yao , Alastair David Trigg and Chai Tai Chong

Improving Performance and Reliability of 3D Wafer Level Packaging with Unique Polymer Coating Process

Antun Peic., Felix Massa, Johanna Bartel, Thorsten Matthias, Markus Wimplinger, Thomas Uhrmann and Paul Lindner

Effect of Process Pressure on PVD AIN Thin Film

J.L. Xie and Sunil Wickramanayaka

50-Gb/s Silicon Mach-Zehnder Interferometer-based Optical Modulator with only 1.3 V pp Driving Voltages

Xiaoguang Tu, Tsung-Yang Liow, Junfeng Song, Xianshu Luo, Lian-Xi Jia, Qing Fang, Mingbin Yu and Guo-Qiang Lo