

2015 International Conference on Microelectronic Test Structures (ICMTS 2015)

**Tempe, Arizona, USA
23-26 March 2015**



**IEEE Catalog Number: CFP15MTS-POD
ISBN: 978-1-4799-8305-6**

TABLE OF CONTENTS

Session 1: Reliability and Array Structures

Co-Chairs:

Brad Smith, Freescale, USA

Christopher Hess, PDF, USA

09:10 [1-1] 14nm BEOL TDDDB Reliability Testing and Defect Analysis , T. Kane	2
09:30 [1-2] A Novel Structure of MOSFET Array to Measure Ioff-Ion with High Accuracy and Density , T. Suzuki, A. Anchlia, V. Cherman, H. Oishi, S. Mori, J. Ryckaert, K. Ogawa, G. Van der Plas, E. Beyne, Y. Fukuzaki, D. Verkest, and H. Ohnuma	9
09:50 [1-3] Circuit Architecture and Measurement Technique to Reduce the Leakage Current Stemming from Peripheral Circuits with an Array Structure in Examining the Resistive Element , S. Sato, T. Ito, and Y. Omura	14
10:10 [1-4] A Proposal for Early Warning Indicators to Detect Impending Metallization Failure of DMOS Transistors in Cyclic Operation , M. Ritter and M. Pfost	18

Session 2: Modeling

Co-Chairs:

Hans P. Tuinhout, NXP, Netherlands

Yu Cao, ASU, USA

11:10 [2-1] SPICE Modeling of 55nm Embedded Superflash® Memory Cells , S. Martinie, O. Rozeau, M. Tadayoni, C. Raynaud, E. Nowak, S. Hariharan, and N. Do	24
11:30 [2-2] Compact Modeling and Parameter Extraction Strategy of Normally-on MOSFET T. Umeda, Y. Hirano, D. Suzuki, A. Tone, T. Inoue, H. Kikuchiara, M. Muira-Mattausch, H. J. Mattausch	29
11:50 [2-3] A Simple T-Model for On-Chip Spiral Inductors , J.-W. Jeong, S.-K. Kwon, J.-N. Yu, S.-Y. Jang, S.-H. Oh, C.-Y. Kim, G.-W. Lee, and H.-D. Lee	33
12:10 [2-4] A Four-Terminal JFET Compact Model for High-Voltage Power Applications , W. Wu, S. Banerjee, and K. Joardar	37

Session 3: Process Evaluation

Co-Chairs:

Larg Weiland, PDF, USA

Satoshi Habu, Keysight, Japan

13:40 [3-1] Accelerating 14nm Device Learning and Yield Ramp Using Parallel Test Structures as Part of a New Inline Parametric Test Strategy , G. Moore, V. Liao, S. McDade, and B. Verzi	44
14:00 [3-2] Employing an On-Die Test Chip for Maximizing Parametric Yields of 28 nm Parts , J. Mueller, S. Jallepalli, R. Mooraka, and S. Hector	50
14:20 [3-3] Robust Process Capability Index Tracking for Process Qualification , C. Gu and C. C. McAndrew	54
14:40 [3-4] New Compact Model for Performance and Process Variability Assessment in 1 4nm FDSOI CMOS Technology , Y. Denis, F. Monsieur, G. Ghibaudo, J. Mazurier, E. Josse, D. Rideau, C. Charbillet, C. Tavernier, and H. Jaouen	59
15:00 [3-5] Silicon Thickness Monitoring Strategy for FD-SOI 28 nm Technology , A. Cros, F. Monsieur, Y. Carminati, P. Normandon, D. Petit, F. Arnaud, and J. Rosa	65

Session 4: Discussion Session plus Exhibitor Presentations

Chair:

Anthony J. Walton, U. Edinburgh, UK

15:50 [4.1] A Test Cell for Characterizing Wheat Using Dielectric Spectroscopy , M. Buehler	72
16:00 [4.2] Development of a Compacted Doubly Nesting Array in Narrow Scribe Line Aimed at Detecting Soft Failures of Interconnect Via , H. Shinkawata, N. Tsuboi, A. Tsuda, S. Sato, and Y. Yamaguchi	78
16:10 [4.3] The Impact of Deep Trench and Well Proximity on MOSFET Performance , H. Sheng, T. Bettinger, and J. Bates	82
16:20 [4.4] Withdrawn	
16:30 [4.5] A Test Structure for Reliability Analysis of CMOS Devices and DC and High Frequency AC Stress , T. Matsuda, K. Ichihashi, H. Iwata, and T. Ohzone	86
16:40 [4.6] Measurement and Modeling of IC Self-Heating Including Cooling System Properties , T. Nishimura, H. Tanoue, Y. Odate, H. J. Mattausch, and M. Miura-Mattausch	90
16:50 [4.7] Large Surface Strain Sensing Structures based on Elastic Instabilities , Y. Li, G. McHale, J. G. Terry, S. Smith, A. J. Walton, and B. Xu	94
17:00 [4.8] Cross-Correlation of Electrical Measurements via Physics-Based Device Simulations: Linking Electrical and Structural Characteristics , A. Padovani, L. Larcher, L. Vandelli, M. Bertocchi, R. Cavicchioli, D. Veskler, and G. Bersuker	100
17:10 [4.9] NPN CML Ring Oscillators for Model Verification and Process Monitoring , C. Compton	103

Session 5: Parameter Extraction

Co-Chairs:

Mark Poulter, TI, USA

Antoine Cros, STMicroelectronics, France

- 09:00 [5-1] **Compact Modeling Solution of Layout Dependent Effect for FinFET Technology**, D. C. Chen, R. Lee, G. S. Lin, T. H. Lee, M. F. Wang, and D. Y. Wu **110**
- 09:20 [5-2] **A Simple Method for Characterization of MOSFET Serial Resistance Asymmetry**, D. Tomaszewski, G. Glusko, J. Malesinska, K. Domanski, M. Zaborowski, K. Kucharski, D. Szmigiel, and A. Sierakowski **116**
- 09:40 [5-3] **Threshold Voltage Extraction Method in 2D Devices having a mobility with Power-Law Dependence of Carrier Density**, V. Mosser, D. Seron, and Y. Haddab **122**
- 10:00 [5-4] **Measurement of V_{th} due to STI Stress and Inverse Narrow Channel Effect at Ultra-Low Voltage in a Variability-Suppressed Process**, Y. Ogasahara, M. Hioki, T. Nakagawa, T. Sekigawa, T. Tsutsumi, and H. Koike **126**

Session 6: Capacitance

Co-Chairs:

Bill Verzi, Keysight, USA

Yuzo Fukuzaki, Sony Corporation

- 10:50 [6-1] **Monitoring Test Structure for Plasma Process Induced Charging Damage Using Charge-Based Capacitance Measurement (PID-CBCM)**, S. Mori, K. Ogawa, H. Oishi, T. Suzuki, M. Tomita, M. Bairo, Y. Fukuzaki, and H. Ohnuma **132**
- 11:10 [6-2] **A Novel Gate Charge Measurement Method**, A. Mikatani, H. Kakitani, R. Takeda, and A. Wadsworth **138**
- 11:30 [6-3] **Area and Performance Study of FinFET with Detailed Parasitic Capacitance Analysis in 16 nm Process Node**, T. Okagaki, K. Shibutani, H. Matsushita, H. Ojio, M. Morimoto, Y. Tsukamoto, K. Nii, and K. Onozawa **141**
- 11:50 [6-4] **In-line Monitoring Test Structure for Charge-Based Capacitance Measurement (CBCM) with a Start-Stop Self-Pulsing Circuit**, K. Sawada, G. Van der Plas, S. Mori, V. Cherman, A. Mercha, V. Diederik, Y. Fukuzaki, and H. Ammo **145**

Session 7: Resistance

Co-Chairs:

Kiyoshi Takeuchi, Renesas, Japan

Alain Toffoli, CEA/LETI, France

- 13:40 [7-1] **Design and Evaluation of a SiCr ThinFilm Resistor Matching Test Structure**, H. Tuinhout, N. Wils, P. Huiskamp, E. de Koning **152**
- 14:00 [7-2] **Characterization of Recessed Ohmic Contacts to AlGaIn/GaN**, M. Hajlasz, J. J. T. M. Donkers, S. J. Sque, S. B. S. Heil, D. J. Gravesteijn, F. J. R. Rietveld, and J. Schmitz **158**

14:20 [7-3] Novel Sheet Resistance Measurement of AlGaIn/GaN HEMT Wafer Adapted from Four-Point Probe Technique , J. Lehmann, C. Leroux, G. Reimbold, M.Charles, A.Torres, E.Morvan, Y.Baines, G. Ghibaudo, and E.Bano	163
14:40 [7-4] Sheet Resistance Measurement for Process Monitoring of 400° C PureB Deposition on Si , L. Qi and L. K. Nanver	169
15:00 [7-5] Combined Transmission Line Measurement Structures to Study Thin Film Resistive Sensor Fabrication , A. Tabasnikov, A.J. Walton and S. Smith	175

Session 8: Emerging Technologies

Co-Chairs:

Richard Allen, NIST, USA

Tsuyoshi Sekitani, U. Tokyo, Japan

15:50 [8-1] Test Structures for the Wafer Mapping and Correlation of Electrical, Mechanical, High Frequency Magnetic, and Composition of Electroplated Ferromagnetic Alloys , E. Sirotkin, S. Smith, R. Walker, J. G. Terry, and A. J. Walton	182
16:10 [8-2] A Fully-Automated Methodology and System for Printed Electronics Foil Characterization ; F. Vila, J. Pallares, A. Conde, and L. Teres	188
16:30 [8-3] A Capacitive Based Piezoelectric AlN Film Quality Test Structure , N. Jackson, Z. Olszewski , L. Keeney, A. Blake, and A. Mathewson	193

Session 9: Circuits

Co-Chairs:

Greg Yeric, ARM, USA

Mark Ketchen, IBM, USA

09:00 [9-1] Silicon Measurements of Characteristics for Pass-gate/Pull-down/Pull-up MOSs and Search MOS in a 28 nm TCAM Bitcell , K. Nii, K. Yamaguchi, M. Yabuuchi, N. Watanabe, T. Hasegawa, S. Yoshida, T. Okagaki, M. Yokota, and K. Onozawa	200
09:20 [9-2] Test circuit for Accurate Measurement of Setup/Hold and Access Time of Memories , N. Agarwal	204
09:40 [9-3] Reduction of Overhead in Adaptive Body Bias Technology due to Triple-well Structure based on Measurement and Simulation , Y. Ogasahara, T. Sekigawa, M. Hioki, T.i Nakagawa, T. Tsutsumi, and H. Koike	207
10:00 [9-4] Sensitivity-Independent Extraction of Vth Variation Utilizing Log-normal Delay Distribution , A. K. M. M. Islam and H. Onodera	212

Session 10: RF

Co-Chairs:

Kevin McCarthy, UC Cork, Ireland

Stewart Smith, U. Edinburgh, UK

10:50 [10-1] Characterization of Wideband Decoupling Power Line with Extremely Low Characteristic Impedance for Millimeter-Wave CMOS Circuits , R. Goda, S. Amakawa, K. Katayama, K. Takano, T. Yoshida, and M. Fujishima	220
--	-----

11:10 [10-2] Observations on Substrate Characterisation through Coplanar Transmission Line Impedance Measurements , L. Floyd and J. Pike	224
11:30 [10-3] Systematic Calibration Procedure of Process Parameters for Electromagnetic Field Analysis of Millimeter-Wave CMOS Devices , K. Takano, K. Katayama, S. Mizukusa, S. Amakawa, T.Yoshida, and M. Fujishima	230
11:50 [10-4] Electromagnetic Field Test Structure Chip for Back End of the Line Metrology , L. You, Y. Obeng, and J. Kopanski	235