

11th Annual International Wafer- Level Packaging Conference

(IWLPC 2014)

**San Jose, California, USA
11-13 November 2014**

ISBN: 978-1-5108-0356-5

Printed from e-media with permission by:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571



Some format issues inherent in the e-media version may also appear in this print version.

Copyright© (2014) by Surface Mount Technology Association (SMTA)
All rights reserved.

Printed by Curran Associates, Inc. (2015)

For permission requests, please contact Surface Mount Technology Association (SMTA)
at the address below.

Surface Mount Technology Association (SMTA)
5200 Wilson Road
Suite 215
Edina, MN 55424

Phone: (952) 920-4682
Fax: (952) 926-1819

www.smta.org

Additional copies of this publication are available from:

Curran Associates, Inc.
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: 845-758-0400
Fax: 845-758-2634
Email: curran@proceedings.com
Web: www.proceedings.com

Sessions at a Glance: Tuesday, November 11th

7:50 AM	Opening Comments Keith Cooper, SET North America, Conference General Chair Oak Ballroom (2nd Floor)		
8:00 AM	Keynote Address: Living Connected Through Trillions Sensors 1 Janusz Bryzek, Ph.D., Chair of the TSensors Summit Oak Ballroom (2nd Floor)		
9:00 AM	Coffee Break Exhibit Hall		
	WLP TRACK MONTEREY ROOM	3D TRACK SAN CARLOS ROOM	MEMS TRACK SANTA CLARA
	Session 1 – Wafer-Level Final Test & Simulation Chair: Janet Love, Blair-Gordon Associates Co-Chair: Rey Alvarado, Qualcomm	Session 2 – Temporary Wafer Bonding Integration and Underfill Chair: Peter Ramm, Ph.D., Fraunhofer EMFT Co-Chair: Ted Tessier, FlipChip International	Session 3 – 3D MEMS Interconnects and Bonding Chair: Roger Grace, Roger Grace Associates Co-Chair: Russell Shumway, Amkor Technology
9:45 AM	Mobile Applications to Enhance Manufacturing Productivity in Advanced Packaging 33 Shekar Krishnaswamy, Applied Materials, Inc. and Didier Chavet, SanDisk	Temporary Bonding on the Move Towards High Volume: A Status Update On Cost Of Ownership Thomas Uhrmann, EV Group 54	NCP Versus NCF for Thermocompression MEMS Bonding Using Gold Stud Bumps 79 Maaike M. Visser Taklo, SINTEF
10:15 AM	OEE and Production Yield Improvements on WLCSP Devices: Case Study Using Novel Probe Design 38 Ranauld Perez, Johnstech International	Addressing Critical Assembly Challenges in 2.5D and 3D IC Assembly 59 Guilian Gao, Invensas Corporation	Ceramic Wafer Bonding for Vertically Integrated MEMS 86 Dirk Wuensch, Chemnitz, University of Technology
10:45 AM	Material Selection and Its Impact on Coplanarity of Spring Pin Probe Heads..... 44 Jiachun Zhou, Smiths Connectors – ID	Non-Conductive Film (NCF) Underfill for Flip Chip Assembly and High Reliability 66 Anupam Choubey, The Dow Chemical Company	A New Manufacturing Approach for Fabricating Next Generation 3-D Interconnects for MEMS and ICs Using Directed Nanoparticle Assembly 91 Cihan Yilmaz, Northeastern University
11:15 AM	BVA™ Technology Enabling the Next Generation of Ultra-Fine Pitch Wide-IO Package-on-Package 48 Rajesh Katkar, Invensas Corporation	Room Temperature Temporary Bonding/ Debonding Processes for 2.5/ 3D Integration .. 73 Tim McCrone, SUSS MicroTec	3D MEMS Wafer Level Packaging Exemplified by RF Characterized TSVs & TGVs and Integration of Bonding Processes 97 Peter Ágren, Ph.D., Silex Microsystems AB
11:45 AM	Lunch Break – Sponsored By Johnstech International Bayshore Foyer		
1:15 PM	3D PANEL DISCUSSION - HOSTED BY 3D INCITES, INC. OAK BALLROOM (2ND FLOOR)		
	System Level Advantages of 3D Integration Moderator: Francoise von Trapp, 3D InCites, Inc. Panelists: Rama Alapati, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Haba, Google Simon McElrea, Energon Corporation		
2:45 PM	Refreshment Break – Sponsored by Axus Technology Exhibit Hall		
	WLP TRACK MONTEREY ROOM	3D TRACK SAN CARLOS ROOM	MEMS TRACK SANTA CLARA
	Session 4 - Wafer-Level Materials Chair: Luu Nguyen, Ph.D., Texas Instruments Co-Chair: Boyd Rogers, Ph.D., Deca Technologies	Session 5 – Bonding and Metrology Chair: Sumant Sood, KLA-Tencor Co-Chair: Keith Cooper, SET Corporation	Session 6 - MEMS Wafer Level Packaging Chair: Maaike M. Visser Taklo, Ph.D., SINTEF Co-Chair: Russell Shumway, Amkor Technology
3:30 PM	Enhancing WLPGA Board Level Reliability Through SACQ™, A New Lead-Free Solder Material Tak Sang Yeung, Broadcom Corporation..... 109	Characterization of Stress and Topology In WLP Processes Using CGS Interferometry 131 David Owen, Ph.D., Ultratech, Inc.	MEMS WLP Processes and Examples 156 Micheal Shillinger, Innovative Micro Technology (IMT)
4:00 PM	Wafer-Level Chip-Scale Packaging for Power Device Operating at High Temperature..... 116 Chenping Jia, CTR AG	Electrostatic Supported Thin-Wafer Processing in 3DIC By Means of the T-ESC Technology ...137 Suresh Biligiri, ProTec Carrier Systems	The Optimization of MEMS Through The Development of Generic Manufacturing Platforms Andre Rouzaud, CEA LETI 161
4:30 PM	Reconstituted Big-Chip LEDs on Multi-layer Interconnects for High-Brightness Lighting 121 Liang Wang, Invensas Corporation	Development Done on Device Bonder to Address 3D Requirements in a Production Environment Pascal Metzger, Ph.D., SET Corporation 143	Extending Capabilities of Etch and Deposition Technologies for 3D Packaging of MEMS in Volume Production 165 Chris Jones, SPTS Technologies
5:00 PM	Recent Advances in Die Attach Film 126 Frederick Lo, AI Technology	Thermal Resistant Thin Wafer Support Technology for 3DIC 149 John Moore, Daetec, LLC	Fabrication of 3D Microrobotic Parallel Actuator Architecture 172 Peter Raffensperger, University of Canterbury
	5:30pm - 7:00pm, Exhibit Hall Exhibitor Reception – Hosted by KLA - Tencor		

Sessions at a Glance: Wednesday, November 12th

8:00 AM	MEMS Plenary: Wearable, Wireless Health Solutions and Related Packaging Challenges 183 Mehran Mehregany, Ph.D., Case Western Reserve University OAK BALLROOM (2ND FLOOR)		
9:00 AM	9:00 – 9:45am, Exhibit Hall Coffee Break		
	WLP TRACK MONTEREY ROOM	3D TRACK SAN CARLOS ROOM	3D TRACK SANTA CLARA ROOM
	Session 7 – Wafer-Level Process & Metrology Chair: Jainwen Li, SMIC Co-Chair: Janet Love, Blair-Gordon Associates	Session 8 – Processing: TSV and Interposers Chair: Laurette Nacamulli, The Dow Chemical Company Co-Chair: André Rouzaud, CEA LETI	Session 9 – Metrology Chair: Maaikje M. Visser Taklo, Ph.D., SINTEF Co-Chair: Keith Cooper, SET Corporation
9:45 AM	Metrology and Inspection for RDL in HVM 198 Russ Dudley, Rudolph Technologies, Inc.	Bosch Process Characterization for Donut TSV's Andy Miller, IMEC 214	High Throughput Wafer Edge Inspection and Monitoring for Advanced Wafer Level Packaging Sumant Sood, KLA-Tencor 237
10:15 AM	Enhancing WLCSP Reliability Through Build-Up Structure Improvements and New Solder Alloys Boyd Rogers, Deca Technologies, Inc. 201	300mm Wafer-Scale Through-Silicon Via (TSV) Process With Optimized Backside Reveal and Planarization Methods 220 Seth Kruger, SUNY Polytechnic Institute	High Resolution 3D X-Ray Microscopy for the Development of Wafer Level Packaging and 3D IC Integration 242 Allen Gu, Ph.D., Carl Zeiss X-ray Microscopy, Inc.
10:45 AM	Automated Wafer-Level Testing of Critical MEMS Parameters using Optical Vibration Measurement Eric Lawrence, Polytec Inc. 208	Analytical and Experimental Studies Of 2.5D Silicon Interposer Warpage: Impact of Assembly Sequences, Materials Selection and Process Parameters 225 Ron Zhang, Invensas Corporation	Optical Metrology for High Volume Manufacturing of 3DIC with TSV N/A Christopher Rosenthal, Lasertec USA Inc.
11:15 AM	Process Control at Post-Saw for Low-K Wafers Reza Asgari, Rudolph Technologies, Inc. 212	Demonstration of SiC Interposer with High Density and Fine Pitch Microbumps 232 Melanie Yajima, HRL Laboratories, LLC	Wafer Overlay Measurement Using Bright-Field Optical Microscopy 248 Chia-Hung Cho, Industrial Technology Research Institute (ITRI)
11:45 AM	Lunch Break – Sponsored By Sonix Bayshore Foyer		
1:15 PM	WLP Plenary - Enabling Wearable Electronics: Innovation through Miniaturization 253 Theodore (Ted) G. Tessier, FlipChip International, LLC OAK BALLROOM (2ND FLOOR)OAK BALLROOM		
	2:15pm– 3:00pm, Exhibit Hall Refreshment Break – Sponsored by Johnstech International		
	Exhibition Closes 3:30pm		
	WLP TRACK MONTEREY ROOM	3D TRACK SAN CARLOS ROOM	3D-I TRACK SANTA CLARA ROOM
	Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology Co-Chair: Rey Alvarado, Qualcomm	Session 11 – Electroplating and Metrology Chair: Steven Xu, Qualcomm Co-Chair: André Rouzaud, CEA LETI	Session 12 – Integration Chair: Laurette Nacamulli, The Dow Chemical Company Co-Chair: Keith Cooper, SET Corporation
3:00 PM	FlexLine™ - A Universal Wafer-Level Packaging Platform for Fan-In and Fan-Out Designs 274 Rajendra Pendse, Ph.D., STATS ChipPAC, Inc.	Uniform, Flat, and Interfacial Void Free Deposits for Copper Pillar Applications 297 Matthew Thorseth, The Dow Chemical Company	Interposer Based Wide IO-Processor Integration Andy Heinig, Fraunhofer Institute for Integrated Circuits 319
3:30 PM	Panel Based Fan-Out Packaging to Reduce Cost Klaus Ruhmer, Rudolph Technologies, Inc. 280	The Advanced Monitoring of Organic Additives in Copper Electroplating Baths 302 Peter Bratin, Ph.D., ECI Technology	Cost Comparison of Embedded Die and Wafer Level Packaging 325 Chet Palesko, SavanSys Solutions LLC
4:00 PM	Size Does Matter - Breaking the Barriers of Wafer Level Packaging 286 Adi Merschon, Universal Instruments Corporation	Non-destructive Acoustic Metrology for Void Detection in TSV's 308 Robin Mair, Rudolph Technologies, Inc.	Integrated Tools and Systems to Improve 3D Manufacturability 329 Sony Varghese, Micron Technology Inc.
4:30 PM	Adhesive Enhancement Technology for Directly Metal Plating on Molding Compound 291 Kenichiroh Mukai, Atotech USA Inc.	Endoscopes Gain from 3D Assembly and Meticulous Process Control 316 Phil Marcoux, Promex Industries	Unique Polymer Coating Process for Improving Performance and Reliability of 3D Wafer Level Packaging 336 Antun Peic, Ph.D., EV Group
	5:00pm IWLPC Concludes		