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Phone: (952) 920-4682 Fax: (952) 926-1819

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Session 1 - Water-Level Find Test & Simulation Chair. Januel Love, Billic down Associates Ca-Chair: Ray Alvarado, Quatorm Session 2 - Temporary Mark Bonding Integration and Underfill Chair: Poter Stark, FiloChip International Session 3 - Memory Mark Bonding Chair: Roy Stark, Poter Stark, PiloChip International Session 3 - Memory Mark Bonding Chair: Roy Stark, Pilor Philo Chair: Ted Tessier, FiloChip International Session 3 - Memory Mark Bonding Chair: Roy Stark, Pilor Philom Chair: Ted Tessier, FiloChip International NCP Versus NCF for Thermocomy Bonding Using Gold Stud Bumps Marke M. Visser Taklo, SINTEF 11:15 AM Design 38 Bramad Perz, Jonstein International Temporary Bonding on the Move Towards High Nethers Starks Update On Cost Of Ownership Banadu Perz, Jonstein International NCP Versus NCF for Thermocomy Marke M. Visser Taklo, SINTEF 10:45 AM Material Selection and Its Impact on Coplanarity of Jachum Zhou, Smiths Connectors – ID Non-Conductive Film (NCF) Underfill for Filo Chip Assembly59 Guilan Gao, Invensas Corporation A New Marking Almostice Asse Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Boros Chan Yinaz, Markesator Boros Chan Yinaz, Markesator Diversite Analysis Katar, Invensas Corporation New Katariang Applications Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Soria Chan Yinaz, Markesator Jonesa Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Soria Chan Yinaz, Markesator Soria Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Soria Chan Yinaz, Markesator Newers Chan Yinaz	Opening Comments	Sessions			
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Design 38 Guilan Gao, Invensas Corporation Dirk Wuensch, Chemnitz, University 10:45 AM Material Selection and Its Impact on Coplanarity of Jachun Zhou, Smiths Connectors – ID Non-Conductive Film (NCF) Underfill for Filp Chip Assembly and High Reliability 66 Anupam Choubey, The Dow Chemical Company A New Manufacturing Approach for Beneration 30 Dirke Valenza 11:15 AM BVA*** Technology Enabling the Next Generation of Rejesh Katkar, Invensas Corporation Room Temperature Temporary Bonding/ Debonding Processes for 2.5 / 30 Integration 30 MEMS Wafer Level Packaging Tim McCrone, SUSS MicroTec 11:45 AM Bysher Foyer 30 PANEL DISCUSSION + HOSTED BY 30 INCITES, INC. OAK BALLROOM (2ND FLOOR) 30 DEMS Wafer Level Packaging Tim McCrone, SUSS MicroTec 11:45 AM 30 PANEL DISCUSSION + HOSTED BY 30 INCITES, INC. OAK BALLROOM (2ND FLOOR) 30 DEMS Wafer Level Packaging Tim McCrone, SUSS MicroTec 11:45 FM System Level Advantages of 30 Integration Moderator: Francoise von Trapp. 30 InCites, Inc. Panelists: Rama Alapat, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Habe, Google Simon McElrea, Energous Corporation 2:45 PM WLP TRACK MONTEREY ROOM Session 4 - Wafer-Level Materials Chair: Luu Nguyen, Ph.D., Tesas Instruments Co-Chair: Burding McMerology Chair: Sumant Sood, KLA-Tencor Co-Chair: Boyd Rogers, Ph.D., Deas Technologies 30 TRACK SAN CARLOS ROOM MEMS TRACK SAN T Co-Chair: Russell Shurway, Anko Co-Chair: Russel Shurway, Anko Co-Chair: Russel Shurway, Anko Co-Chair: Ru	3D IC Assembly 59 MEMS 86				
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John Moore, Daetec, LLC Peter Rattensperger, University of C					
5:30pm - 7:00pm, Exhibit Hall		.,			

	Sessions at a Glance: Wednesday, November 12th MEMS Plenary: Wearable, Wireless Health Solutions and Related Packaging Challenges 183 Mehran Mehregany, Ph.D., Case Western Reserve University OAK BALLROOM (2ND FLOOR) 9:00 – 9:45am, Exhibit Hall Coffee Break				
9:00 AM					
	WLP TRACK MONTEREY ROOM	3D TRACK SAN CARLOS ROOM	3D TRACK SANTA CLARA ROOM		
	Session 7 – Wafer-Level Process & Metrology Chair: Jainwen Li, SMIC Co-Chair: Janet Love, Blair-Gordon Associates	Session 8 – Processing: TSV and Interposers Chair: Laurette Nacamulli, The Dow Chemical Company Co-Chair: André Rouzaud, CEA LETI	Session 9 – Metrology Chair: Maaike M. Visser Taklo, Ph.D., SINTEF Co-Chair: Keith Cooper, SET Corporation		
9:45 AM	Metrology and Inspection for RDL in HVM 198 Russ Dudley, Rudolph Technologies, Inc.	Bosch Process Characterization for Donut TSV's Andy Miller, IMEC 214	High Throughput Wafer Edge Inspection and Monitoring for Advanced Wafer Level Packaging Sumant Sood, KLA-Tencor 237		
10:15 AM	Enhancing WLCSP Reliability Through Build-Up Structure Improvements and New Solder Alloys Boyd Rogers, Deca Technologies, Inc 201	300mm Wafer-Scale Through-Silicon Via (TSV) Process With Optimized Backside Reveal and Planarization Methods 220	High Resolution 3D X-Ray Microscopy for the Development of Wafer Level Packaging and 3D IC Integration 242		
		Seth Kruger, SUNY Polytechnic Institute	Allen Gu, Ph.D., Carl Zeiss X-ray Microscopy, Inc.		
10:45 AM	Automated Wafer-Level Testing of Critical MEMS Parameters using Optical Vibration Measurement Eric Lawrence, Polytec Inc 208	Analytical and Experimental Studies Of 2.5D Silicon Interposer Warpage: Impact of Assembly Sequences, Materials Selection and Process Parameters 225	Optical Metrology for High Volume Manufacturing of 3DIC with TSV N/A Christopher Rosenthal, Lasertec USA Inc.		
44.45 AM	Process Control at Post-Saw for Low-K Wafers	Ron Zhang, Invensas Corporation Demonstration of SiC Interposer with High			
11:15 AW	Reza Asgari, Rudolph Technologies, Inc 212	Density and Fine Pitch Microbumps 232 Melanie Yajima, HRL Laboratories, LLC	Wafer Overlay Measurement Using Bright-Field Optical Microscopy 248 Chia-Hung Cho, Industrial Technology Research Institute (ITRI)		
		Lunch Break – Sponsored By Sonix	()		
11:45 AM		Bayshore Foyer			
1:15 PM	WLP Plenary - Enbabling Wearable Electronics: Innovation through Miniaturization 253 Theodore (Ted) G. Tessier, FlipChip International, LLC OAK BALLROOM (2ND FLOOR)OAK BALLROOM 2:15pm- 3:00pm, Exhibit Hall Refreshment Break - Sponsored by Johnstech International				
1:15 PM			tional		
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<u>1:15 PM</u>		reshment Break – Sponsored by Johnstech Interna	tional 3D-I TRACK SANTA CLARA ROOM		
<u>1:15 PM</u>	Ref	reshment Break – Sponsored by Johnstech Interna Exhibition Closes 3:30pm	3D-I TRACK SANTA CLARA ROOM Session 12 – Integration		
	Ref WLP TRACK MONTEREY ROOM Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology	reshment Break – Sponsored by Johnstech Interna Exhibition Closes 3:30pm 3D TRACK SAN CARLOS ROOM Session 11 – Electroplating and Metrology Chair: Steven Xu, Qualcomm	3D-I TRACK SANTA CLARA ROOM Session 12 – Integration Chair: Laurette Nacamulli, The Dow Chemical Compan Co-Chair: Keith Cooper, SET Corporation Interposer Based Wide IO-Processor Integration		
3:00 PM	Ref WLP TRACK MONTEREY ROOM Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology Co-Chair: Rey Alvarado, Qualcomm FlexLine™ - A Universal Wafer-Level Packaging Platform for Fan-In and Fan-Out Designs 274	reshment Break – Sponsored by Johnstech Interna Exhibition Closes 3:30pm 3D TRACK SAN CARLOS ROOM Session 11 – Electroplating and Metrology Chair: Steven Xu, Qualcomm Co-Chair: André Rouzaud, CEA LETI Uniform, Flat, and Interfacial Void Free Deposits for Copper Pillar Applications 297	3D-I TRACK SANTA CLARA ROOM Session 12 – Integration Chair: Laurette Nacamulli, The Dow Chemical Compan Co-Chair: Keith Cooper, SET Corporation Interposer Based Wide IO-Processor Integration Andy Heinig, Fraunhofer Institute for Integrated Circuits 319		
3:00 PM 3:30 PM	Ref WLP TRACK MONTEREY ROOM Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology Co-Chair: Rey Alvarado, Qualcomm FlexLine™ - A Universal Wafer-Level Packaging Platform for Fan-In and Fan-Out Designs 274 Rajendra Pendse, Ph.D., STATS ChipPAC, Inc. Panel Based Fan-Out Packaging to Reduce Cost	The Advanced Monitoring of Organic Additives in Copper Electroplating and State Comparison	3D-I TRACK SANTA CLARA ROOM Session 12 – Integration Chair: Laurette Nacamulli, The Dow Chemical Compan Co-Chair: Keith Cooper, SET Corporation Interposer Based Wide IO-Processor Integration Andy Heinig, Fraunhofer Institute for Integrated Circuits 319 Cost Comparison of Embedded Die and Wafer Leve Packaging 325		
3:00 PM 3:30 PM 4:00 PM	Ref WLP TRACK MONTEREY ROOM Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology Co-Chair: Rey Alvarado, Qualcomm FlexLine™ - A Universal Wafer-Level Packaging Platform for Fan-In and Fan-Out Designs 274 Rajendra Pendse, Ph.D., STATS ChipPAC, Inc. Panel Based Fan-Out Packaging to Reduce Cost Klaus Ruhmer, Rudolph Technologies, Inc 280 Size Does Matter - Breaking the Barriers of Wafer Level Packaging 286	The Advanced Monitoring of Organic Additives in Copper Fillar Applications 302 The Advanced Monitoring and Metrology The Advanced Monitoring of Organic Additives The Advanced Monitoring of Organic Additives The Advanced Monitoring and Metrology The Advanced Monitoring and Organic Additives The Advanced Monitoring Baths 302 The Advanced Monitoring Of Organic Additives The Advanced Monitoring States 302 The Advanced Monitoring Metrology The Advanced Met	3D-I TRACK SANTA CLARA ROOM Session 12 – Integration Chair: Laurette Nacamulli, The Dow Chemical Compan Co-Chair: Keith Cooper, SET Corporation Interposer Based Wide IO-Processor Integration Andy Heinig, Fraunhofer Institute for Integrated Circuits 319 Cost Comparison of Embedded Die and Wafer Level Packaging 325 Chet Palesko, SavanSys Solutions LLC Integrated Tools and Systems to Improve 3DI Manufacturability 329		