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(IWLPC 2014)

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Session 1 - Water-Level Find Test & Simulation Chair. Januel Love, Billic down Associates Ca-Chair: Ray Alvarado, Quatorm         Session 2 - Temporary Mark Bonding Integration and Underfill Chair: Poter Stark, FiloChip International         Session 3 - Memory Mark Bonding Chair: Roy Stark, Poter Stark, PiloChip International         Session 3 - Memory Mark Bonding Chair: Roy Stark, Pilor Philo Chair: Ted Tessier, FiloChip International         Session 3 - Memory Mark Bonding Chair: Roy Stark, Pilor Philom Chair: Ted Tessier, FiloChip International         NCP Versus NCF for Thermocomy Bonding Using Gold Stud Bumps Marke M. Visser Taklo, SINTEF           11:15 AM Design 38 Bramad Perz, Jonstein International         Temporary Bonding on the Move Towards High Nethers Starks Update On Cost Of Ownership Banadu Perz, Jonstein International         NCP Versus NCF for Thermocomy Marke M. Visser Taklo, SINTEF           10:45 AM Material Selection and Its Impact on Coplanarity of Jachum Zhou, Smiths Connectors – ID         Non-Conductive Film (NCF) Underfill for Filo Chip Assembly59 Guilan Gao, Invensas Corporation         A New Marking Almostice Asse Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Boros Chan Yinaz, Markesator Boros Chan Yinaz, Markesator Diversite Analysis Katar, Invensas Corporation         New Katariang Applications Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Soria Chan Yinaz, Markesator Jonesa Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Soria Chan Yinaz, Markesator Soria Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Newers Chan Yinaz, Markesator Soria Chan Yinaz, Markesator Newers Chan Yinaz	Opening Comments	Sessions			
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Oak Ballcom (2nd Fibor)           9:00 AM         Coffee Break Exhibit Hail           WLP TRACK   MONTEREY ROOM         30 TRACK   SAN CARLOS ROOM           Session 1 - Wafer Low Efricant Sessions Co-Chair: Ray Alvanado, Qualcomm         30 TRACK   SAN CARLOS ROOM           Chair, Ray Alvanado, Qualcomm         Session 2 - DEMRÓN Regor Grave, Rego					
9:00 AM         Coffee Break Exhibit Hall           WLP TRACK   MONTEREY ROOM Session 1 - Market vale finance 1 and the simulation Colar. Jour Low, Black Gordan, Associates Co-Chair: Rey Alrendo, Qualcomm         30 TRACK   SAN CARLOS ROOM Session 1 - Temporary Market Bending Distance Texper Rancet, Royar Grace A Co-Chair: Rey Alrendo, Qualcomm         MMMS TRACK   SAN Session 1 - Temporary Bonding on the Move Towards High Dolmer Chare: Rancet, Royar Grace A Co-Chair: Rever Sension, Filo Chip International Deller Chare: Rever Sension, Filo Chip International Deller Chare: Rancet Sension, Filo Chip International Deller Chare: Rancet Sension, Filo Chip International Ranaud Perz, Johnstein International Ranaud Perz, Johnstein International Hist SAM         NCP Varsus RCF for Thermocomy Deller Chare: Rancet Sension, Filo Co-Chair: Russet Status, SINTEF           11:15 AM         QEE and Production Yield Improvements on WLCSP Devices: Case Study Using Novel Probe Beigin					
Exhibit Hall           WLP TRACK   MONTEREY ROOM         MEMS TRACK   SANT CARLOS ROOM           Session 1 - Mark Leve Bildrechar Asexadase           Chair: Ray Alvarado, Qualcom         Session 2 - Temporary Mark Bonding           Chair: Ray Alvarado, Qualcom           Session 3 - Directoma Manufacturing         MCP Porture Mark Market M					
Session 1 - Water-Level Find Test & Simulation Chini - Love, Biair-Condon Associates Ca-Chair: Ray Alvarado, Quatomm         Session 2 - Temporary Mark Bonding Integration and Underfill Chair: Peter Ramm, PL, D., Frauchofer EMFT Ca-Chair: Ted Tessier. FijC/Chip International         Session 3 - Mark Simulation Ca-Chair: Ray Alvarado, Quatomm         Session 3 - Mark Simulation Ca-Chair: Fast Simulation Ca-Chair: Ted Tessier. FijC/Chip International         NCP Versus NCF for Thermocomy Mark Microsoft Simulation District Naves, SamDak           9:45 AM         Mobile Applications to Enhance Manufacturing Productivity in Advanced Packaging	Exhibit Hall				
Chair. Jane Love, Billin-Corton Associates Co-Chair: Ray Alvarado, Qualcom     Integration and Underfill Chair. Feer Ray Morado, Qualcom     Chair. Text Framm, Ph.D., Frambofer EMFT Co-Chair. Tod Tessier, FlipChip International     Chair. Text Preprint Co-Chair. Tod Tessier, FlipChip International     Chair. Roy Report Gaoe, Co-Chair. Roy Status Update On Cest Of Ownership Notable Chavet, SamDiak Molie Chavet, SamDiak Molie Chavet, SamDiak Ranaud Perez, Johnstein International     MCP Versus NCF for Thermocom, Baniak M. Visser Tako, SINTEF       10:15 AM OEE and Production Yield Improvements on WLCSP Devices: Case Study Using Novel Probe Besign					
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WLCSP Devices: Case Study Using Novel Probe Design	ime: A Status Update On Cost Of Ownership Maaike M. Visser Taklo. SINTEF	Productivity in Advanced Packaging 33 Shekar Krishnaswamy, Applied Materials, Inc. and			
WLCSP Devices:         Case Study Using Novel Probe Beign	ressing Critical Assembly Challenges in 2.5D Ceramic Wafer Bonding for Vertically Integrate				
Design 38         Guilan Gao, Invensas Corporation         Dirk Wuensch, Chemnitz, University           10:45 AM         Material Selection and Its Impact on Coplanarity of Jachun Zhou, Smiths Connectors – ID         Non-Conductive Film (NCF) Underfill for Filp Chip Assembly and High Reliability 66 Anupam Choubey, The Dow Chemical Company         A New Manufacturing Approach for Beneration 30 Dirke Valenza           11:15 AM         BVA*** Technology Enabling the Next Generation of Rejesh Katkar, Invensas Corporation         Room Temperature Temporary Bonding/ Debonding Processes for 2.5 / 30 Integration         30 MEMS Wafer Level Packaging Tim McCrone, SUSS MicroTec           11:45 AM         Bysher Foyer         30 PANEL DISCUSSION + HOSTED BY 30 INCITES, INC. OAK BALLROOM (2ND FLOOR)         30 DEMS Wafer Level Packaging Tim McCrone, SUSS MicroTec           11:45 AM         30 PANEL DISCUSSION + HOSTED BY 30 INCITES, INC. OAK BALLROOM (2ND FLOOR)         30 DEMS Wafer Level Packaging Tim McCrone, SUSS MicroTec           11:45 FM         System Level Advantages of 30 Integration Moderator: Francoise von Trapp. 30 InCites, Inc. Panelists: Rama Alapat, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Habe, Google Simon McElrea, Energous Corporation           2:45 PM         WLP TRACK   MONTEREY ROOM Session 4 - Wafer-Level Materials Chair: Luu Nguyen, Ph.D., Tesas Instruments Co-Chair: Burding McMerology Chair: Sumant Sood, KLA-Tencor Co-Chair: Boyd Rogers, Ph.D., Deas Technologies         30 TRACK   SAN CARLOS ROOM MEMS TRACK   SAN T Co-Chair: Russell Shurway, Anko Co-Chair: Russel Shurway, Anko Co-Chair: Russel Shurway, Anko Co-Chair: Ru	3D IC Assembly 59 MEMS 86				
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Spring Pin Probe Heads 44 Jachun Zhou, Smiths Connectors – ID       Flip Chip Assembly and High Reliability 66 Anyam Choubey, The Dow Chemical Company       Generation 3-D Interconnects for I Using Directed Nanoparticle Asse Chan Yilmaz, Northeastem Universi         11:15 AM Ultra-Fine Pitch Wide-IO Package-on-Package	-Conductive Film (NCF) Underfill for A New Manufacturing Approach for Fabricatin	,			
Jachun Zhou, Smiths Connectors – ID       Anupam Choubey, The Dow Chemical Company       Using Directed Nanoparticle Asse Chan Yilmaz, Northeastern Universi Difference Stars Marker, Invensas Corporation         11:15 AM Rajesh Katkar, Invensas Corporation       Room Temperature Temporary Bonding/ Debonding Processes for 2.5/3D Integration73 Tim McCrone, SUSS MicroTec       3D MEMS Wafer Level Packaging Tim McCrone, SUSS MicroTec         11:15 PM       Lunch Break – Sponsored By Johnstech International Bayshore Foyer       Bonding Processes97 Peter Agren, Ph.D., Silex Microsyste         11:15 PM       System Level Advantages of 3D Integration Moderator: Francoise von Trapp, 3D InClies, Inc. Panelists: Rama Alapti, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Haba, Google Simon McElrea, Energous Corporation         2:45 PM       Refreshment Break – Sponsored by Axus Technology Exhibit Hall         WLP TRACK   MONTEREY ROOM Chair: Lun Nguyen, Ph.D., Texas Instruments Ca-Chair: Boyd Rogers, Ph.D., Deca Technologies       3D TRACK   SAN CARLOS ROOM Session 4 - Wafer-Level Materials Chair: Maaike M. Visser Takko, Ph.I. Co-Chair: Royd Rogers, Ph.D., Deca Technologies       Session 5 - Bonding and Mittrology Chair: Maaike M. Visser Takko, Ph.I. Co-Chair: Royd Rogers, Ph.D., Deca Technologies         3:30 PM       Enhancing WLBGA Board Level Reliability Through SACQ **, A New Lead-Free Solder Material Tak Sang Yeung, Broadcom Corporation109       Characterization of Stress and Topology In WLP Processes Using CGS Interferometry131 David Oven, Ph.D., Uttratech, Inc.       The Optimization of MeMS Throug Peelopment of Generic Manufer Andre Rouzaud, CEA LE					
11:15 AM       BVA™ Technology Enabling the Next Generation of Room Temperature Temporary Bonding/ Utra-Fine Pitch Wide-IO Package-on-Package 46       Room Temperature Temporary Bonding/ Debonding Processes for 2.5/3 D Integration 73       3D MEMS Wafer Level Packaging Characterized TSVs & TGVs and I Bonding Processes 97 Peter Agren, Ph.D., Silex Microsyste         11.45 AM       Lunch Break – Sponsored By Johnstech International Bayshore Foyer       3D PANEL DISCUSSION - HOSTED BY 3D INCITES, INC. OAK BALLROOM (2ND FLOOR)       System Level Advantages of 3D Integration Moderator: Francoise von Trapp, 3D InCites, Inc. Panelists: Rama Alapati, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Haba, Google Simon McEirea, Energous Corporation         2:45 PM       Refreshment Break – Sponsored by Axus Technology Exhibit Hall       Session 6 - MEMS Wafer Level PA Session 6 - MeMS Wafer Level PA Chair: Luu Nguyen, Ph.D., Texas Instruments Ca-Chair: Boyd Rogers, Ph.D., Deca Technologies       Session 6 - MeMS Wafer Level PA Chair: Maaike M. Visser Taklo, Ph.I Ca-Chair: Reith Cooper, SET Corporation         3:30 PM       Enhancing WLBGA Board Level Reliability Through SACQ™, A New Lead-Free Solder Material Tak Sang Yeung, Broadcom Corporation 109       Characterization of Stress and Topology In WLP Processes Using CGS Interferometry 131 David Owen, Ph.D., Ultratech, Inc.       MEMS WLP Processes and Examp Micheal Shillinger, Innovative Micro David Owen, Ph.D., SET Corporation 133         4:30 PM       Reconstituted Big-Chip LEDs on Multi-layer Interconnects for High-Brightness Lighting 121 Liang Wang, Invensas Corporation       Development Done on Device Bonder to Address 3D Re					
BVA** Technology Enabling the Next Generation of Rajesh Katkar, Invensas Corporation       Kounn Feinporature Feinporature Foundation of SUB MicroTec       Characterized TSVs & TGVs and I Bonding Processes for 2.5/ 3D Integration 73 Tim McCrone, SUSS MicroTec       Characterized TSVs & TGVs and I Bonding Processes 97 Peter Agren, Ph.D., Silex Microsyste         11:45 AM       Lunch Break – Sponsored By Johnstech International Bayshore Foyer       Status Microsyste         11:15 PM       3D PANEL DISCUSSION - HOSTED BY 3D INCITES, INC. OAK BALLROOM (2ND FLOOR)       Status Microsyste         System Level Advantages of 3D Integration Moderator: Francoise von Trapp, 3D InCites, Inc. Panelists: Rama Alapati, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Haba, Google Simon McEirea, Energous Corporation       Status TechNology Exhibit Hall         2:45 PM       Refreshment Break – Sponsored by Axus Technology Exhibit Hall       Session 6 - MEMS Wafer Level Pa Chair: Maaike M. Visser Taklo, Ph.I. Co-Chair: Boyd Rogers, Ph.D., Deca Technologies       Session 6 - MEMS Wafer Level Pa Chair: Maaike M. Visser Taklo, Ph.I. Co-Chair: Boyd Rogers, Ph.D., Deca Technologies       Session 6 - MEMS Wafer Level Pa Chair: Maaike M. Visser Taklo, Ph.I. Co-Chair: Russel Shurmey, Amko Co-Chair: Russel Shurmey, Amko	Cihan Yilmaz, Northeastern University				
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Other the Pitch Wheel Or Package of	Characterized TSVs & TGVs and Integration of onding Processes for 2 5/ 3D Integration 73				
11:45 AM       Lunch Break - Sponsored By Johnstech International Bayshore Foyer         11:45 AM       3D PANEL DISCUSSION - HOSTED BY 3D INCITES, INC. OAK BALLROOM (2ND FLOOR)         11:15 PM       System Level Advantages of 3D Integration Moderator: Francoise von Trapp, 3D InCites, Inc. Panelists: Rama Alapati, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Haba, Google Simon McElrea, Energous Corporation         2:45 PM       Refreshment Break - Sponsored by Axus Technology Exhibit Hall         VLP TRACK   MONTEREY ROOM       3D TRACK   SAN CARLOS ROOM         Session 4 · Wafer-Level Materials Chair: Luu Nguyen, Ph.D., Texas Instruments Co-Chair: Royd Rogers, Ph.D., Deca Technologies       Session 5 - Bonding and Metrology Chair: Sumant Sood, KLA-Tencor Co-Chair: Russell Shumway, Amko         3:30 PM       Enhancing WLBGA Board Level Reliability Through SACQ <sup>TM</sup> , A New Lead-Free Solder Material Tak Sang Yeung, Broadcom Corporation 109       Characterization of Stress and Topology In WLP Processes Using CGS Interferometry 131 David Owen, Ph.D., Ultratech, Inc.       MEMS WLP Processes and Examp Micheal Shillinger, Innovative Micro David Owen, Ph.D., Ultratech, Inc.         4:30 PM       Reconstituted Big-Chip LEDs on Multi-layer Interconnects for High-Brightness Lighting 122 Liang Wang, Invensas Corporation       Development Done on Device Bonder to Address 3D Requirements in a Production Environment Pascal Metzger, Ph.D., SET Corporation 149       The Optimization of 3D Microrobotic Pa Architecture 172	McCropp SLISS MicroToc Bonding Processes 97				
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1:15 PM       OAK BALLROOM (2ND FLOOR)         System Level Advantages of 3D Integration Moderator: Francoise von Trapp, 3D InCites, Inc. Panelists: Ram Alpati, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Haba, Google Simon McElrea, Energous Corporation         2:45 PM       Refreshment Break – Sponsored by Axus Technology Exhibit Hall         WLP TRACK   MONTEREY ROOM Session 4 - Wafer-Level Materials Chair: Luu Nguyen, Ph.D., Texas Instruments Chair: Luu Nguyen, Ph.D., Deca Technologies       3D TRACK   SAN CARLOS ROOM MEMS TRACK   SANT Co-Chair: Boyd Rogers, Ph.D., Deca Technologies         3:30 PM       Enhancing WLBGA Board Level Reliability Through SACQ <sup>™</sup> , A New Lead-Free Solder Material Tak Sang Yeung, Broadcom Corporation					
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Exhibit Hall         WLP TRACK   MONTEREY ROOM       3D TRACK   SAN CARLOS ROOM       MEMS TRACK   SANT         Session 4 · Wafer-Level Materials       Session 5 - Bonding and Metrology       Session 6 - MEMS Wafer Level Pa         Chair: Luu Nguyen, Ph.D., Texas Instruments       Session 5 - Bonding and Metrology       Session 6 - MEMS Wafer Level Pa         Co-Chair: Boyd Rogers, Ph.D., Deca Technologies       Co-Chair: Keith Cooper, SET Corporation       Session 6 - MEMS Wafer Level Pa         3:30 PM       Enhancing WLBGA Board Level Reliability Through SACQ™, A New Lead-Free Solder Material Tak Sang Yeung, Broadcom Corporation 109       Characterization of Stress and Topology In WLP Processes Using CGS Interferometry 131 David Owen, Ph.D., Ultratech, Inc.       MEMS WLP Processes and Examp Micheal Shillinger, Innovative Micro         4:00 PM       Wafer-Level Chip-Scale Packaging for Power Device Operating at High Temperature 116 Chenping Jia, CTR AG       Electrostatic Supported Thin-Wafer Processing in 3DIC By Means of the T-ESC Technology137 Suresh Billigiri, ProTec Carrier Systems       The Optimization of MEMS Throug Development of Generic Manufaci Andre Rouzaud, CEA LETI 161         4:30 PM       Reconstituted Big-Chip LEDs on Multi-layer Interconnects for High-Brightness Lighting 121 Liang Wang, Invensas Corporation       Development Done on Device Bonder to Address 3D Requirements in a Production Environment Pascal Metzger, Ph.D., SET Corporation 143       Extending Capabilities of Etch and Technologies <tr< td=""><td>an, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Haba, Google</td><td colspan="4">Moderator: Francoise von Trapp, 3D InCites, Inc. Panelists: Rama Alapati, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel H</td></tr<>	an, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Haba, Google	Moderator: Francoise von Trapp, 3D InCites, Inc. Panelists: Rama Alapati, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel H			
Session 4 - Wafer-Level Materials       Session 5 - Bonding and Metrology       Session 6 - MEMS Wafer Level Pa         Chair: Luu Nguyen, Ph.D., Texas Instruments       Co-Chair: Sumant Sood, KLA-Tencor       Chair: Maaike M. Visser Taklo, Ph.I.         Co-Chair: Boyd Rogers, Ph.D., Deca Technologies       Chair: Sumant Sood, KLA-Tencor       Co-Chair: Russell Shumway, Amko         3:30 PM       Enhancing WLBGA Board Level Reliability       Chair: Sumant Sood, KLA-Tencor       Co-Chair: Russell Shumway, Amko         Through SACQ <sup>TM</sup> , A New Lead-Free Solder Material       Characterization of Stress and Topology In WLP       MEMS WLP Processes and Examp         7ak Sang Yeung, Broadcom Corporation 109       Characterization of Stress and Topology In WLP       Memory Michael Shillinger, Innovative Micro         4:00 PM       Wafer-Level Chip-Scale Packaging for Power       Electrostatic Supported Thin-Wafer Processing       The Optimization of MEMS Throug         0evelopment Jia, CTR AG       Electrostatic Supported Thin-Wafer Processing       The Optimization of MEMS Throug         4:30 PM       Reconstituted Big-Chip LEDs on Multi-layer       Development Done on Device Bonder to Address       Extending Capabilities of Etch and Technologies for 3D Packaging of Production 161         4:30 PM       Reconstituted Big-Chip LEDs on Multi-layer       Development Done on Device Bonder to Address       Extending Capabilities of Etch and Technologies for 3D Packaging of Production 143         5:00 PM					
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Co-Chair: Boyd Rogers, Ph.D., Deca Technologies       Co-Chair: Keith Cooper, SET Corporation       Co-Chair: Russell Shumway, Amko         3:30 PM       Enhancing WLBGA Board Level Reliability Through SACQ™, A New Lead-Free Solder Material Tak Sang Yeung, Broadcom Corporation 109       Characterization of Stress and Topology In WLP Processes Using CGS Interferometry 131 David Owen, Ph.D., Ultratech, Inc.       MEMS WLP Processes and Examp Micheal Shillinger, Innovative Micro         4:00 PM       Wafer-Level Chip-Scale Packaging for Power Device Operating at High Temperature 116 Chenping Jia, CTR AG       Electrostatic Supported Thin-Wafer Processing in 3DIC By Means of the T-ESC Technology137 Suresh Biligiri, ProTec Carrier Systems       The Optimization of MEMS Throug Development of Generic Manufact Andre Rouzaud, CEA LETI 161         4:30 PM       Reconstituted Big-Chip LEDs on Multi-layer Interconnects for High-Brightness Lighting 121 Liang Wang, Invensas Corporation       Development Done on Device Bonder to Address 3D Requirements in a Production Environment Pascal Metzger, Ph.D., SET Corporation 143       Extending Capabilities of Etch and Technologies for 3D Packaging of Production 165 Chris Jones, SPTS Technologies         5:00 PM       Recent Advances in Die Attach Film 126 Frederick Lo, Al Technology       Thermal Resistant Thin Wafer Support Technology for 3DIC 149       Fabrication of 3D Microrobotic Pa Architecture 172	· · · · · · · · · · · · · · · · · · ·				
Through SACQ™, A New Lead-Free Solder Material Tak Sang Yeung, Broadcom Corporation 109       Processes Using CGS Interferometry 131 David Owen, Ph.D., Ultratech, Inc.       Michael Shillinger, Innovative Micro         4:00 PM       Wafer-Level Chip-Scale Packaging for Power Device Operating at High Temperature 116 Chenping Jia, CTR AG       Electrostatic Supported Thin-Wafer Processing in 3DIC By Means of the T-ESC Technology137 Suresh Biligiri, ProTec Carrier Systems       The Optimization of MEMS Throug Development of Generic Manufact Andre Rouzaud, CEA LETI 161         4:30 PM       Reconstituted Big-Chip LEDs on Multi-layer Interconnects for High-Brightness Lighting 121 Liang Wang, Invensas Corporation       Development Done on Device Bonder to Address 3D Requirements in a Production Environment Pascal Metzger, Ph.D., SET Corporation 143       Extending Capabilities of Etch and Technologies for 3D Packaging of Production 165 Chris Jones, SPTS Technologies         5:00 PM       Recent Advances in Die Attach Film 126 Frederick Lo, Al Technology       Thermal Resistant Thin Wafer Support Technology for 3DIC 149       Fabrication of 3D Microrobotic Pa Architecture 172					
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4:30 PM       Reconstituted Big-Chip LEDs on Multi-layer Interconnects for High-Brightness Lighting 121 Liang Wang, Invensas Corporation       Development Done on Device Bonder to Address 3D Requirements in a Production Environment Pascal Metzger, Ph.D., SET Corporation 143       Extending Capabilities of Etch and Technologies for 3D Packaging of Production 165 Chris Jones, SPTS Technologies         5:00 PM       Recent Advances in Die Attach Film 126 Frederick Lo, Al Technology       Thermal Resistant Thin Wafer Support Technology for 3DIC 149       Fabrication of 3D Microrobotic Pa Architecture 172	DIC By Means of the T-ESC Technology 137				
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5:00 PM         Recent Advances in Die Attach Film 126         Thermal Resistant Thin Wafer Support         Fabrication of 3D Microrobotic Pa           Frederick Lo, Al Technology         Technology for 3DIC 149         Architecture 172					
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John Moore, Daetec, LLC Peter Rattensperger, University of C					
5:30pm - 7:00pm, Exhibit Hall		.,			

	Sessions at a Glance: Wednesday, November 12th         MEMS Plenary: Wearable, Wireless Health Solutions and Related Packaging Challenges 183         Mehran Mehregany, Ph.D., Case Western Reserve University         OAK BALLROOM (2ND FLOOR)         9:00 – 9:45am, Exhibit Hall         Coffee Break				
9:00 AM					
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	Session 7 – Wafer-Level Process & Metrology Chair: Jainwen Li, SMIC Co-Chair: Janet Love, Blair-Gordon Associates	Session 8 – Processing: TSV and Interposers Chair: Laurette Nacamulli, The Dow Chemical Company Co-Chair: André Rouzaud, CEA LETI	Session 9 – Metrology Chair: Maaike M. Visser Taklo, Ph.D., SINTEF Co-Chair: Keith Cooper, SET Corporation		
9:45 AM	Metrology and Inspection for RDL in HVM 198 Russ Dudley, Rudolph Technologies, Inc.	Bosch Process Characterization for Donut TSV's Andy Miller, IMEC 214	High Throughput Wafer Edge Inspection and Monitoring for Advanced Wafer Level Packaging Sumant Sood, KLA-Tencor 237		
10:15 AM	Enhancing WLCSP Reliability Through Build-Up Structure Improvements and New Solder Alloys Boyd Rogers, Deca Technologies, Inc 201	300mm Wafer-Scale Through-Silicon Via (TSV) Process With Optimized Backside Reveal and Planarization Methods 220	High Resolution 3D X-Ray Microscopy for the Development of Wafer Level Packaging and 3D IC Integration 242		
		Seth Kruger, SUNY Polytechnic Institute	Allen Gu, Ph.D., Carl Zeiss X-ray Microscopy, Inc.		
10:45 AM	Automated Wafer-Level Testing of Critical MEMS Parameters using Optical Vibration Measurement Eric Lawrence, Polytec Inc 208	Analytical and Experimental Studies Of 2.5D Silicon Interposer Warpage: Impact of Assembly Sequences, Materials Selection and Process Parameters 225	Optical Metrology for High Volume Manufacturing of 3DIC with TSV N/A Christopher Rosenthal, Lasertec USA Inc.		
44.45 AM	Process Control at Post-Saw for Low-K Wafers	Ron Zhang, Invensas Corporation Demonstration of SiC Interposer with High			
11:15 AW	Reza Asgari, Rudolph Technologies, Inc 212	Density and Fine Pitch Microbumps 232 Melanie Yajima, HRL Laboratories, LLC	Wafer Overlay Measurement Using Bright-Field Optical Microscopy 248 Chia-Hung Cho, Industrial Technology Research Institute (ITRI)		
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11:45 AM		Bayshore Foyer			
1:15 PM	WLP Plenary - Enbabling Wearable Electronics: Innovation through Miniaturization 253 Theodore (Ted) G. Tessier, FlipChip International, LLC OAK BALLROOM (2ND FLOOR)OAK BALLROOM 2:15pm- 3:00pm, Exhibit Hall Refreshment Break - Sponsored by Johnstech International				
1:15 PM			tional		
1:15 PM			tional		
<u>1:15 PM</u>		reshment Break – Sponsored by Johnstech Interna	tional 3D-I TRACK   SANTA CLARA ROOM		
<u>1:15 PM</u>	Ref	reshment Break – Sponsored by Johnstech Interna Exhibition Closes 3:30pm	3D-I TRACK   SANTA CLARA ROOM Session 12 – Integration		
	Ref WLP TRACK   MONTEREY ROOM Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology	reshment Break – Sponsored by Johnstech Interna Exhibition Closes 3:30pm 3D TRACK   SAN CARLOS ROOM Session 11 – Electroplating and Metrology Chair: Steven Xu, Qualcomm	3D-I TRACK   SANTA CLARA ROOM Session 12 – Integration Chair: Laurette Nacamulli, The Dow Chemical Compan Co-Chair: Keith Cooper, SET Corporation Interposer Based Wide IO-Processor Integration		
3:00 PM	Ref WLP TRACK   MONTEREY ROOM Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology Co-Chair: Rey Alvarado, Qualcomm FlexLine™ - A Universal Wafer-Level Packaging Platform for Fan-In and Fan-Out Designs 274	reshment Break – Sponsored by Johnstech Interna Exhibition Closes 3:30pm 3D TRACK   SAN CARLOS ROOM Session 11 – Electroplating and Metrology Chair: Steven Xu, Qualcomm Co-Chair: André Rouzaud, CEA LETI Uniform, Flat, and Interfacial Void Free Deposits for Copper Pillar Applications 297	3D-I TRACK   SANTA CLARA ROOM Session 12 – Integration Chair: Laurette Nacamulli, The Dow Chemical Compan Co-Chair: Keith Cooper, SET Corporation Interposer Based Wide IO-Processor Integration Andy Heinig, Fraunhofer Institute for Integrated Circuits 319		
3:00 PM 3:30 PM	Ref WLP TRACK   MONTEREY ROOM Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology Co-Chair: Rey Alvarado, Qualcomm FlexLine™ - A Universal Wafer-Level Packaging Platform for Fan-In and Fan-Out Designs 274 Rajendra Pendse, Ph.D., STATS ChipPAC, Inc. Panel Based Fan-Out Packaging to Reduce Cost	The Advanced Monitoring of Organic Additives in Copper Electroplating and State Comparison	3D-I TRACK   SANTA CLARA ROOM Session 12 – Integration Chair: Laurette Nacamulli, The Dow Chemical Compan Co-Chair: Keith Cooper, SET Corporation Interposer Based Wide IO-Processor Integration Andy Heinig, Fraunhofer Institute for Integrated Circuits 319 Cost Comparison of Embedded Die and Wafer Leve Packaging 325		
3:00 PM 3:30 PM 4:00 PM	Ref WLP TRACK   MONTEREY ROOM Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology Co-Chair: Rey Alvarado, Qualcomm FlexLine™ - A Universal Wafer-Level Packaging Platform for Fan-In and Fan-Out Designs 274 Rajendra Pendse, Ph.D., STATS ChipPAC, Inc. Panel Based Fan-Out Packaging to Reduce Cost Klaus Ruhmer, Rudolph Technologies, Inc 280 Size Does Matter - Breaking the Barriers of Wafer Level Packaging 286	The Advanced Monitoring of Organic Additives in Copper Fillar Applications 302 The Advanced Monitoring and Metrology The Advanced Monitoring of Organic Additives The Advanced Monitoring of Organic Additives The Advanced Monitoring and Metrology The Advanced Monitoring and Organic Additives The Advanced Monitoring Baths 302 The Advanced Monitoring Of Organic Additives The Advanced Monitoring States 302 The Advanced Monitoring Metrology The Advanced Met	3D-I TRACK   SANTA CLARA ROOM Session 12 – Integration Chair: Laurette Nacamulli, The Dow Chemical Compan Co-Chair: Keith Cooper, SET Corporation Interposer Based Wide IO-Processor Integration Andy Heinig, Fraunhofer Institute for Integrated Circuits 319 Cost Comparison of Embedded Die and Wafer Level Packaging 325 Chet Palesko, SavanSys Solutions LLC Integrated Tools and Systems to Improve 3DI Manufacturability 329		