

2015 IEEE International Memory Workshop

(IMW 2015)

**Monterey, California, USA
17-20 May 2015**



**IEEE Catalog Number: CFP15NOV-POD
ISBN: 978-1-4673-6934-3**

IMW 2015 Table of Contents

IMW 2015 Committees	ix
----------------------------------	----

Summary of Events	x
--------------------------------	---

Schedule	xi
-----------------------	----

Invited Talks

Technology Scaling Challenge and Future Prospects of DRAM and NAND Flash Memory	1
<i>Sung-Kye Park, SK Hynix Inc.</i>	

Understanding NAND's Intrinsic Characteristics Critical Role in Solid State Drive (SSD) Design	5
<i>Will Akin, Micron Technology, Inc.</i>	

From Memory in our Brain to Emerging Resistive Memories in Neuromorphic Systems	9
<i>Barbara DeSalvo, E.Vianello, D.Garbin, O.Bichler, L.Perniola, CEA LETI</i>	

Embedded Microcontroller Memories – Application Memory Usage	13
<i>Thomas Jew, Freescale Semiconductor, Inc.</i>	

Technology Trends and Near-future Applications of Embedded STT-MRAM	17
<i>Shinobu Fujita, Hiroki Noguchi, Kazutaka Ikegami, Susumu Takeda, Kumiko Nomura, and Keiko Abe, Toshiba Corporation</i>	

Poster Session

Modeling of Atomic Migration Phenomena in Phase Change Memory Devices	22
<i>Luca Crespi, Andrea Lacaita, Mattia Boniardi, Enrico Varesi, Andrea Ghetti, Andrea Redaelli, and Giuseppe D'Arrigo</i>	

Performance Prediction of Large-Scale 1S1R Resistive Memory Array Using Machine Learning	26
<i>Zizhen Jiang, Peng Huang, Liang Zhao, Shahar Kvatinsky, Shimeng Yu, Xiaoyan Liu, Jinfeng Kang, Yoshio Nishi, and H. -S. Philip Wong</i>	

A Novel Approach to Identify the Carrier Transport Path and Its Correlation to the Current Variation in RRAM	30
<i>Nianduan Lu, Ling Li, Pengxiao Sun, Ming Wang, Qi Liu, Hangbing Lv, Shibing Long, and Ming Liu</i>	

Optimization of the ATW Non-volatile Memory for Connected Smart Objects	34
<i>Jonathan Bartoli, Vincenzo Della Marca, Jeremy Postel-Pellerin, Julien Delalleau, Arnaud Regnier, Stephan Niel, Francesco La Rosa, Pierre Canet, and Frederic Lalande</i>	
A Study of Blocking and Tunnel Oxide Engineering on Double-Trapping (DT) BE-SONOS Performance	38
<i>Roger Lo, Pei-Ying Du, Tzu-Hsuan Hsu, Chen-Jun Wu, Jung-Yi Guo, Chun-Min Cheng, Hang-Ting Lue, Yen-Hao Shih, Tuo-Hung Hou, Kuang-Yeu Hsieh, and Chih-Yuan Lu</i>	
In-Line-Test of Variability and Bit-Error-Rate of HfO_x-Based Resistive Memory	42
<i>B. Ji, H. Li, Q. Ye, S. Gausepohl, S. Deora, D. Veksler, S. Vivekanand, H. Chong, H. Stamper, T. Burroughs, C. Johnson, M. Smalley, S. Bennett, V. Kaushik, J. Piccirillo, M. Rodgers, M. Passaro and M. Liehr</i>	
A 55 nm Logic-Process-Compatible, Split-Gate Flash Memory Array Fully Demonstrated at Automotive Temperature with High Access Speed and Reliability	46
<i>Nhan Do, Latt Tee, Santosh Hariharan, Steven Lemke, Mandana Tadayoni, Will Yang, MT Wu, Jinho Kim, Yueh-Hsin Chen, Chien-Sheng Su, Vipin Tiwari, Stephen Zhou, Rodger Qian, and Ian Yue</i>	
Characterization and Modeling of Advanced Placement Algorithms for NAND Flash Arrays	49
<i>Carmine Miccoli, Karthik Sarpatwari, Domenico Di Cicco, Mattia Cichocki, Violante Moschiano, Paul Ruby, and Krishna Parat</i>	
Improved Lateral Coupling Cell for a Standard Logic Process eNVM Application	53
<i>Kwang-Il Choi, Nam-Yun Kim, Sung-Kun Park, and In-Wook Cho</i>	
Efficiently Realizing Weak Cell Aware DRAM Error Tolerance for Sub-20nm Technology Nodes	57
<i>Hao Wang, Kai Zhao, and Tong Zhang</i>	
Memory Technologies for Neural Networks	61
<i>Dmitri Strukov, Farnood Merrikh-Bayat, Mirko Prezioso, Xinjie Guo, Brian Hoskins, and Konstantin Likharev</i>	
A Survey of Trends in Non-Volatile Memory Technologies: 2000–2014	65
<i>Kosuke Suzuki, and Steven Swanson</i>	

Technical Papers

Thin-Silicon Injector (TSI): an All-Silicon Engineered Barrier, Highly Nonlinear Selector for High Density Resistive RAM Applications	69
<i>Bogdan Govoreanu, L. Zhang, Davide Crotti, Yang-Shun Fan, Vasile Paraschiv, Hubert Hody, Thomas Witters, Johan Meersschaut, Sergiu Clima, Christoph Adelman, and Malgorzata Jurczak</i>	
Critical ReRAM Stack Parameters Controlling Complimentary versus Bipolar Resistive Switching	73
<i>Alexander Schonhals, Dirk Wouters, Astrid Marchewka, Thomas Breuer, Katharina Skaja, Vikas Rana, Stephan Menzel, and Rainer Waser</i>	

Comprehensive Methodology for ReRAM and Selector Design Guideline of Cross-point Array	77
<i>Sangheon Lee, Sooeun Lee, Kibong Moon, Jaehyuk Park, Byungsub Kim, and Hyunsang Hwang</i>	
Optimization of TiN/TaOx/HfO2/TiN RRAM Arrays for Improved Switching and Data Retention	81
<i>Xueyao Huang, Huaqiang Wu, Deepak C. Sekar, Steve N. Nguyen, Kun Wang, and He Qian</i>	
Visualization of Conductive Filament during Write and Erase Cycles on Nanometer-scale ReRAM Achieved by in-situ TEM	85
<i>Masaki Kudo, Masashi Arita, Yasuo Takahashi, Ichiro Fujiwara, Masayuki Shimuta and Kazuhiro Ohba</i>	
A Reliable Cross-Point MLC ReRAM with Sneak Current Compensation	89
<i>Jong-Min Baek, Sang-Yun Kim, Jae-Koo Park, Jae-Young Park, and Kee-Won Kwon</i>	
Relationship among Current Fluctuations During Forming, Cell-to-Cell Variability and Reliability in RRAM Arrays	93
<i>Alessandro Grossi, Cristian Zambelli, Piero Olivo, Enrique Miranda, Valeriy Stikanov, Thomas Schroeder, Christian Walczyk, and Christian Wenger</i>	
From Resistive Switching Mechanisms in AM4Q8 Mott Insulators to Mott Memories	97
<i>Julien Tranchant, Etienne Janod, Benoit Corraze, Marie-Paule Besland, and Laurent Cario</i>	
Optimization of Ru based Hybrid Floating Gate For Planar NAND Flash	101
<i>Laurent Breuil, Judit Lisoni, Pieter Blomme, Geert Van den bosch and Jan Van Houdt</i>	
A Highly Reliable and Cost Effective 16nm Planar NAND Cell Technology	105
<i>William Kueber, Giuseppina Puzzilli, Niccolo Righetti, Ricardo Basco, Lin Li, Silvia Beltrami, Massimo Bertuccio, Elisa Camozzi, David Daycock, Matthew King, Chris Larsen, Jeff Karpan, Akira Goda, and Ceredig Roberts</i>	
Integration and electrical evaluation of epitaxially grown Si and SiGe channels for vertical NAND Memory applications	109
<i>Elena Capogreco, Robin Degraeve, Judit Gloria Lisoni, K. V. Luong, Antonio Arreghini, Maria Toledano-Luque, Andriy Hikavvy, Toshinori Numata, Kristin De Meyer, Geert Van den bosch, and Jan Van Houdt</i>	
TCAD Simulation of Data Retention Characteristics of Charge Trap Device for 3-D NAND Flash Memory	113
<i>Dongyeon Oh, Bonghoon Lee, Eunmee Kwon, Sangyong Kim, Gyuseog Cho, Sungkye Park, Seokkiu Lee, and Sungjoo Hong</i>	
Performance Characterization of LDPC Codes for Large-Volume NAND Flash Data	117
<i>Patrick Khayat, Mustafa Kaynak, Sivagnanam Parthasarathy, and Saeed Sharifi Tehrani</i>	

Study on the Sub-threshold Margin Characteristics of the Extremely Scaled 3-D DRAM Cell Transistors	121
<i>Kyung Kyu Min, Il-Woong Kwon, Seehe Cho, Mikyung Kwon, Tae-Su Jang, Tae-Kyung Oh, Yong-Taik Kim, Seon-Yong Cha, Sung-Kye Park, and Sung-Joo Hong</i>	
A 16-Level-Cell Nonvolatile Memory with Crystalline In-Ga-Zn Oxide FET	125
<i>Takanori Matsuzaki, Tatsuya Onuki, Shuhei Nagatsuka, Hiroki Inoue, Takahiko Ishizu, Yoshinori Ieda, Naoto Yamade, Hidekazu Miyairi, Masayuki Sakakura, Yutaka Shionoiri, Kiyoshi Kato, Takashi Okuda, Jun Koyama, Yoshitaka Yamamoto, and Shunpei Yamazaki</i>	
A Bulk Planar SiGe Quantum-Well based ZRAM with Low VT Variability	129
<i>Sangya Dutta, Sushant Mittal, Saurabh Lodha, Udayan Ganguly, and Jorg Schulze</i>	
Novel Multi-bit Non-Volatile SRAM Cells For Runtime Reconfigurable Computing	133
<i>Yanjun Ma</i>	
A Triple-Protection Structured COB FRAM with 1.2-V Operation and 1017-Cycle Endurance	137
<i>Hitoshi Saito, Tatsuya Sugimachi, Ko Nakamura, Soichiro Ozawa, Naoya Sashida, Satoru Mihara, Yukinobu Hikosaka, Wensheng Wang, Tomoyuki Hori, Kazuaki Takai, Mitsuharu Nakazawa, Noboru Kosugi, Masaki Okuda, Makoto Hamada, Shoichiro Kawashima, Shoichiro Kawashima, Takashi Eshita, and M. Matsumiya</i>	
1T1MTJ STT-MRAM Cell Array Design with an Adaptive Reference Voltage Generator for Improving Device Variation Tolerance	141
<i>Hiroki Koike, Sadahiko Miura, Hiroaki Honjo, Tosinari Watanabe, Hideo Sato, Soshi Sat, Takashi Nasuno, Yasuo Noguchi, Mitsuo Yasuhira, Takaho Tanigawa, Masakazu Muraguchi, Masaaki Niwa, Kenchi Ito, Shoji Ikeda, Hideo Ohno, and Tetsuo Endoh</i>	
Dynamic Reference Sensing Scheme for Deeply Scaled STT-MRAM	145
<i>Wang Kang, Tingting Pang, Youguang Zhang, Dafine Ravelosona, and Weisheng Zhao</i>	
Machine Learning Prediction for 13x Endurance Enhancement in ReRAM SSD System	149
<i>Tomoko Ogura Iwasaki, Sheyang Ning, Hiroki Yamazawa, Chao Sun, Shuhei Tanakamaru, and Ken Takeuchi</i>	
3x Faster Speed Solid-State Drive with a Write Order Based Garbage Collection Scheme	153
<i>Chihiro Matsui, Asuka Arakawa, Chao Sun, Tomoko Ogura Iwasaki, and Ken Takeuchi,</i>	
Application Driven SCM&NAND Flash Hybrid SSD Design for Data-Centric Computing System	157
<i>Shun Okamoto, Chao Sun, Shogo Hachiya, Tomoaki Yamada, Yusuke Saito, Tomoko Ogura Iwasaki, and Ken Takeuchi</i>	
LDPC Soft Decoding with Reduced Power and Latency in 1X-2X NAND Flash-Based Solid State Drives	161
<i>Lorenzo Zuolo, Cristian Zambelli, Piero Olivo, Rino Micheloni, and Alessia Marelli</i>	

Functionality Demonstration of a High-Density 1.1V Self-Aligned Split-Gate NVM Cell Embedded Into LP 40 nm CMOS for Automotive and Smart Card Applications	165
<i>D. Shum, L.Q. Luo, Y.T. Chow, F. Zhang, J.B. Tan, X.S. Cai, Z.Q. Teo, N. Do, J.H. Kim, P. Ghazavi, V. Tiwari, D.X. Wang, K.Y. Lim, B.B. Zhou, J.Q. Liu, A. Yeo, T.L. Chang, Y.J. Kong, C.W. Yap, S. Lup, and R. Long</i>	
Single-Poly Embedded NVM Solution for Analog Trimming and Code Storage Applications	169
<i>Sung-Kun Park, Kwang-Il Choi, Nam-Yoon Kim, Jung-Hoon Kim, Young-Jun Kwon, Kwang-Sik Ko, In-Wook Cho, and Kyung-Dong Yoo</i>	
Junction Optimization for Embedded 40nm FN/FN Flash Memory	173
<i>Alessandro Baiano, Michiel van Duuren, Erik van der Vegt, Bob Schippers, Robert Beurze, Daniel Tajari Mofrad, Hans van Zwol, Yu Chen, Jed Chiang, Han Lokker, Kitty van Dijk, Jouke Verbree, Yi Ning Chen, Jochen Garbe, Rob Verhaar, and Do Dormans</i>	
An Analytical Model of e•MMC Key Performance Indicators	177
<i>Paolo Amato, Danilo Caraccio, Emanuele Confalonieri, and Marco Sforzin</i>	
A Procedure to Reduce Cell Variation in Phase Change Memory for Improving Multi-Level-Cell Performances	181
<i>W.S. Khwa, J.Y. Wu, T.H. Su, M.H. Lee, H.P. Li, Y.Y. Chen, M. BrightSky, T.Y. Wang, T.H. Hsu, P.Y. Du, W.C. Chien, S. Kim, H.Y. Cheng, E.K. Lai, Y. Zhu, M.F. Chang, H.L. Lung, and C. Lam</i>	
Universal Thermoelectric Characteristic in Phase Change Memories	185
<i>Nicola Ciochini, Mario Laudato, Antonio Leone, Paolo Fantini, Andrea Leonardo Lacaita, and Daniele Ielmini</i>	
Bilayer Metal-Oxide CBRAM Technology for Improved Window Margin and Reliability	189
<i>Marinela Barci, Gabriel Molas, Alain Toffoli, Mathieu Bernard, Anne Roule, Carlo Cagli, Jacques Cluzel, Elisa Vianello, Barbara De Salvo, and Luca Perniola</i>	
Fast and Stable sub-10µA Pulse Operation in W/SiO₂/Ta/Cu 90nm 1T1R CBRAM Devices	193
<i>Attilio Belmonte, Andrea Fantini, Robin Degraeve, Umberto Celano, Wilfried Vandervorst, Augusto Redolfi, Michel Houssa Malgorzata Jurczak, and Ludovic Goux</i>	
Author Index	197