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Time: Monday, May 25 (14:10-15:40)
Room: Small Auditorium
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Room: S1: Luis F. Branco
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Room: S2: E. Andrade
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Chair(s): Elisenda Bou, *Universitat Politecnica de Catalunya*
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[1]Eindhoven University of Technology, Netherlands; [2]Eindhoven University of Technology and Philips Research Eindhoven, Netherlands

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Room: S11: C. Telmo
Chair(s): Shih-Chii Liu, *ETHZ*
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Chair(s): Xiao-Ping Zhang, *Ryerson University*
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[1]Brandenburg Klinik, Germany; [2]Universität Bielefeld, Germany; [3]University of Southampton, United Kingdom

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Room: 2nd Floor Foyer
Chair(s): Tinoosh Mohsenin, *University of Maryland, Baltimore County*
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[1]Rowan University, United States; [2]University of Hail, Saudi Arabia

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[1]Aix Marseille University / Université de Toulon, France; [2]Aix Marseille University / Université de Toulon / IM2NP, France; [3]Fraunhofer Institute ENAS, Germany; [4]Universität Paderborn, Germany

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[1]National Nano Device Laboratories / National Applied Research Laboratories, Taiwan; [2]National Tsing Hua University, Taiwan

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[1]Hong Kong Polytechnic University, Hong Kong; [2]Lanzhou University, China; [3]University of Electronic Science and Technology of China, China

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[1]Fudan University, China; [2]University of Hong Kong, China

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Time: Monday, May 25 (16:00-17:30)
Room: Small Auditorium
Chair(s): Chia-Chi Chu, *National Tsing Hua University, Taiwan*
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[1]NTT Device Technology Laboratories, Japan; [2]Tokyo University of Agriculture and Technology, Japan

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Room: S5: F. Pessoa
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[1]Ain Shams University, Egypt; [2]American University in Cairo & Zewail City of Science and Technology, Egypt; [3]Cairo University, Egypt

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Room: S7: S. M. Breyner
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[1]MediaTek Inc., United States; [2]Oregon State University, United States

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[1]Pennsylvania State University, United States; [2]Tsinghua University, China

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Room: S8: G. Quartim
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Qi Tian, *University of Texas at San Antonio*

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Room: S9: M.H.V. Silva
Chair(s): Shahriar Mirabbasi, *University of British Columbia*
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Suho Son, Shiwon Jeon, Seol Namgung, Jieun Yoo, Minkyu Song
Dongguk University, Korea, South

A6L-J.2 **Configurable Low Noise Readout Front-End for Gaseous Detectors in 130nm CMOS Technology 1058**
Hugo Hernandez, Wilhelmus Van Noije, Marcelo Munhoz
Universidade de São Paulo, Brazil

A6L-J.3 **A Readout Circuit with Novel Zero-G Offset Calibration for Tri-Axes Capacitive MEMS Accelerometer 1062**
Jungryoul Choi[2], Jungwoo Lee[1], Sangyun Han[1], Sungwook Kim[1], Soonwon Hong[1], Joongho Choi[2]
[1]Sensonia Inc., Korea, South; [2]University of Seoul, Korea, South

A6L-J.4 **Direct Temperature to Digital Converters with Low Supply Sensitivity for Power/Thermal Management 1066**
Yen-Ting Wang[2], Chen Zhao[1], Degang Chen[2], Randall Geiger[2]
[1]Avago technologies, United States; [2]Iowa State University, United States

A6L-J.5 **A Programmable Temperature Trigger Circuit 1070**
Qianqian Wang, Randall Geiger, Degang Chen
Iowa State University, United States

A6L-K: Circuits & Systems for Energy Harvesting

Time: Monday, May 25 (16:00-17:30)
Room: S10: A.S. Cardoso
Chair(s): Eduard Alarcon, *Universitat Politècnica de Catalunya*
Tadashi Suetsugu, *Fukuoka University*

A6L-K.1 **Analysis of the Operation of a Regenerative Electrostatic Energy Harvester 1074**
Antonio Carlos M. de Queiroz
Universidade Federal do Rio de Janeiro, Brazil

A6L-K.2 **On-Chip Integration of Thermoelectric Energy Harvesting in 3D ICs 1078**
Dawei Li, Seda Ogrenci-Memik, Lawrence Henschen
Northwestern University, United States

A6L-K.3 **Pespectives of TFET Devices in Ultra-Low Power Charge Pumps for Thermo-Electric Energy Sources 1082**
David Cavalheiro[2], Francesc Moll[2], Stanimir Valtchev[1]
[1]Universidade Nova de Lisboa, Portugal; [2]Universitat Politècnica de Catalunya, Spain

A6L-K.4 **Power Management System for Ultra-Low Power Energy Harvesting Applications 1086**
Jarno Salomaa, Mika Pulkkinen, Tuomas Haapala, Marko Nurmi, Kari Halonen
Aalto University, Finland

A6L-K.5 **Integrated Synchronous Electric Charge Extraction System for Piezoelectric Energy Harvesters 1090**
Adrian Enriquez Aguayo, Oliver Paul, Tzeno Galchev
Albert-Ludwigs-Universität Freiburg / IMTEK, Germany

A6L-L: Imagers

Time: Monday, May 25 (16:00-17:30)
Room: S11: C. Telmo
Chair(s): Walter Daniel Leon-Salas, *Purdue University*
Tobi Delbruck, *Institute of Neuroinformatics, UZH / ETH-Zurich*

A6L-L.1 **A 3T or 4T Pixel Compatible Dr Extension Technique Suitable for 3D-IC Imagers : a 800x512 and 5µm Pixel Pitch 2D Demonstrator 1094**
Arnaud Peizerat[1], Fadoua Guezzi[1], Michele Benetti[1], Antoine Dupret[1], Remi Jalby[1], Leonardo Bruno de Sa[1], William Guicquero[1], Yves Blanchard[2]
[1]CEA LETI, France; [2]ESIEE, France

A6L-L.2 **An 8-Stage Time Delay Integration CMOS Image Sensor with on-Chip Polarization Pixels 1098**
Hang Yu, Vigil Varghese, Xinyuan Qian, Menghan Guo, Shoushun Chen, Kay Soon Low
Nanyang Technological University, Singapore

A6L-L.3 **On the Calibration of a SPAD-Based 3D Imager with in-Pixel TDC Using a Time-Gated Technique 1102**
Ion Vornicu, Ricardo Carmona-Galán, Ángel Rodríguez-Vázquez
Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, Spain

A6L-L.4 **A 1300 x 800, 700 mW, 30 fps Spectral Polarization Imager 1106**
Missael Garcia, Shengkui Gao, Christopher Edmiston, Timothy York, Viktor Gruev
Washington University in St. Louis, United States

A6L-L.5 **A Scalable 20x20 Fully Asynchronous SPAD-Based Imaging Sensor with AER Readout 1110**
Andrew Berkovich, Timir Datta-Chaudhuri, Pamela Abshire
University of Maryland, College Park, United States

A6L-M: HEVC Algorithms and Implementations

Time: Monday, May 25 (16:00-17:30)
Room: S12: D. Costa
Chair(s): Nam Ling, *Santa Clara University*
Lap-Pui Chau, *Nanyang Technological University*

A6L-M.1 **Encoding Time Control System for HEVC Based on Rate-Distortion-Complexity Analysis 1114**
Guilherme Correa[2], Pedro Assuncao[1], Luis A. Da Silva Cruz[2], Luciano Agostini[3]
[1]Politécnico de Leiria / Instituto de Telecomunicações, Portugal; [2]Universidade de Coimbra / Instituto de Telecomunicações, Portugal; [3]Universidade Federal de Pelotas, Brazil

A6L-M.2 **Rate Control for Screen Content Coding in HEVC 1118**
Yaoyao Guo[1], Bin Li[2], Songlin Sun[1], Jizheng Xu[2]
[1]Beijing University of Posts and Telecommunications, China; [2]Microsoft Research Asia, China

A6L-M.3 **Multiple Layer Parallel Motion Estimation on GPU for High Efficiency Video Coding (HEVC) 1122**
Falei Luo[1], Siwei Ma[2], Juncheng Ma[2], Honggang Qi[3], Li Su[3], Wen Gao[2]
[1]Institute of Computing Technology, Chinese Academy of Sciences, China; [2]Peking University, China; [3]University of Chinese Academy of Sciences, China

A6L-M.4 **Advanced Motion Information Prediction and Inheritance in 3D-HEVC 1126**
Jian-Liang Lin, Yi-Wen Chen, Jicheng An, Kai Zhang, Yu-Wen Huang, Shawmin Lei
MediaTek Inc., Taiwan

A6L-M.5 **Single Depth Intra Coding Mode in 3D-HEVC 1130**
Yi-Wen Chen, Jian-Liang Lin, Yu-Wen Huang, Shawmin Lei
MediaTek Inc., Taiwan

B1L-A: SPECIAL SESSION: Memristor-based Cellular Nanoscale Networks: Theory, Design, and Applications

Time: Tuesday, May 26 (09:30-11:00)
Room: Main Auditorium
Chair(s): Kyeong-Sik Min, *Kookmin University*
Fernando Corinto, *Politecnico di Torino*

B1L-A.1 **Memristor-Based Cellular Nanoscale Networks: Theory, Circuits, and Applications...1134**
Son Ngoc Truong[1], Sanghak Shin[1], Jeasang Song[1], Hyun-Sun Mo[1], Fernando Corinto[2], Kyeong-Sik Min[1]
[1]Kookmin University, Korea, South; [2]Politecnico di Torino, Italy

B1L-A.2 **Stability Analysis Supports Memristor Circuit Design.....1138**
Alon Ascoli[2], Ronald Tetzlaff[2], Stefan Slesazeck[1], Hannes Mähne[1], Thomas Mikolajick[1]
[1]Nano-electronic Materials Laboratory gGmbH, Germany; [2]Technische Universität Dresden, Germany

B1L-A.3 **Linear Programming of Voltage-Controlled Memristors with an Anti-Serial Memristor Circuit 1142**
Hyuncheol Choi, Ram Kaji Budhathoki, Sedong Park, Changju Yang, Hyongsuk Kim
Chonbuk National University, Korea, South

B1L-A.4 **Noise Properties of Ideal Memristors 1146**
Panayiotis Georgiou, It?r Köymen, Emmanuel Drakakis
Imperial College London, United Kingdom

B1L-A.5 **Memristor-Based Synapses and Neurons for Neuromorphic Computing 1150**
Le Zheng[2], Sangho Shin[2], Sung-Mo Steve Kang[1]
[1]Korea Advanced Institute of Science and Technology, Korea, South; [2]University of California, Santa Cruz, United States

B1L-B: SPECIAL SESSION: Electronics Design, Assembly and Reliability for High Temperature Applications

Time: Tuesday, May 26 (09:30-11:00)
Room: Small Auditorium
Chair(s): Colin Johnston, *Oxford University Begbroke Science Park*
Steve Riches, *GE Aviation, Newmarket, UK*

B1L-B.1 **Design of a Frequency Signal Conditioning Unit Applied to Rotating Systems in High Temperature Aero Engine Control 1154**
Lucian Stoica[2], Valentyn Solomko[2], Thorsten Baumheinrich[2], Renato Del Regno[2], Reece Beigh[2], Ian White[1], Geoff Rickard[1], Paul Williams[1]
[1]General Electric - Aviation, United Kingdom; [2]General Electric - Global Research, United States

B1L-B.2 **Electronics Design, Assembly and Reliability for High Temperature Applications 1158**
Steve Riches[1], Colin Johnston[2]
[1]GE Aviation Systems - Newmarket, United Kingdom; [2]Oxford University, United Kingdom

B1L-B.3 **High Temperature SOI CMOS Technology and Circuit Realization for Applications Up to 300°C 1162**
Holger Kappert, Norbert Kordas, Stefan Dreiner, Uwe Paschen, Rainer Kokozinski
Fraunhofer Institute for Microelectronic Circuits and Systems, Germany

B1L-B.4 **High Temperature Electronics Packaging an Overview of Substrates for High Temperature 1166**
David Shaddock, Liang Yin
General Electric, United States

B1L-B.5 **Electronic Packaging of SiC MOSFET-Based Devices for Reliable High Temperature Operation 1170**
Liang Yin, Cheng-Po Chen, Christopher Kapusta, Reza Ghandi
General Electric, United States

B1L-C: ASIC & Specialized VLSI Circuits

Time: Tuesday, May 26 (09:30-11:00)
Room: S1: Luis F. Branco
Chair(s): Malgorzata Chrzanowska-Jeske, *Portland State University*
Massimo Alioto, *National University of Singapore*

B1L-C.1 **RadixBoost: a Hardware Acceleration Structure for Scalable Radix Sort on Graphic Processors 1174**
Xingyu Liu, Shikai Li, Kuan Fang, Yufei Ni, Zonghui Li, Yangdong Deng
Tsinghua University, China

B1L-C.2 **A Programmable Multi-GNSS Baseband Receiver 1178**
Vinh Tran, Nagaraj Shivaramaiah, Oliver Diessel, Andrew Dempster
University of New South Wales, Australia

B1L-C.3 **A Flexible and Energy-Efficient Reconfigurable Architecture for Symmetric Cipher Processing 1182**
Bo Wang, Leibo Liu
Tsinghua University, China

B1L-C.4 **Critical-Path Optimization for Efficient Hardware Realization of Lifting and Flipping DWTs 1186**
Basant Mohanty[1], Pramod Kumar Meher[2], Thambipillai Srikanthan[2]
[1]Jaypee University of Engineering and Technology, India; [2]Nanyang Technological University, Singapore

B1L-C.5 **Improving Fmax of FPGA Circuits Employing DPR to Recover from Configuration Memory Upsets 1190**
Ediz Cetin, Oliver Diessel, Lingkan Gong
University of New South Wales, Australia

B1L-D: Digital Video Processing

Time: Tuesday, May 26 (09:30-11:00)
Room: S2: E. Andrade
Chair(s): Moncef Gabbouj, *Tampere University of Technology*
Tapio Saramäki, *Tampere University of Technology, Finland*

B1L-D.1 **Structural Local DCT Sparse Appearance Model for Visual Tracking 1194**
Bidare K. Shreyamsha Kumar, M.N.S. Swamy, M. Omair Ahmad
Concordia University, Canada

B1L-D.2 **Trajectory Kinematics Descriptor for Trajectory Clustering in Surveillance Videos 1198**
Wei-Cheng Wang[1], Pau-Choo Chung[2], Hsin-Wei Cheng[2], Chun-Rong Huang[2]
[1]National Cheng Kung University, Taiwan; [2]National Chung Hsing University, Taiwan

B1L-D.3 **Clustering of Matched Features and Gradient Matching for Mixed-Resolution Video Super-Resolution 1202**
Renan Ferreira, Edson Hung, Ricardo de Queiroz
Universidade de Brasília, Brazil

B1L-D.4 **A Fast Variable Block Size Motion Estimation Algorithm with Refined Search Range for a Two-Layer Data Reuse Scheme.....1206**
Luheng Jia, Chi-Ying Tsui, Oscar C. Au, Amin Zheng
Hong Kong University of Science and Technology, Hong Kong

B1L-D.5 **Foreground-Based Depth Map Generation for 2D-to-3D Conversion 1210**
Ho Sub Lee[2], Sung In Cho[2], Gyu Jin Bae[2], Hi-Seok Kim[1], Young Hwan Kim[2]
[1]Cheongju University, Korea, South; [2]Pohang University of Science and Technology, Korea, South

B1L-E: Low Power and Wearable Communication Devices

Time: Tuesday, May 26 (09:30-11:00)
Room: S5: F. Pessoa
Chair(s): Joe Cavallaro, *Rice University*
Tokunbo Ogunfunmi, *Santa Clara University, USA*

B1L-E.1 **A 4.5 µW 2.4 GHz Wake-Up Receiver Based on Complementary Current-Reuse RF Detector 1214**
Shih-En Chen, Chin-Lung Yang, Kuang-Wei Cheng
National Cheng Kung University, Taiwan

B1L-E.2 **A 0.5-V 1.56-mW 5.5-GHz RF Transceiver IC Module with J-Shaped Folded Monopole Antenna 1218**
Yosuke Ishikawa, Sang-Yeop Lee, Shin Yonezawa, Sho Ikeda, Yiming Fang, Taisuke Hamada, Hiroyuki Ito, Noboru Ishihara, Kazuya Masu
Tokyo Institute of Technology, Japan

B1L-E.3 **An Energy-Efficient IEEE 802.15.4 Tunable Digital Baseband Targeting Self-Adaptive WPANs 1222**
Vincent Lenoir, Didier Lattard, Ahmed Jerraya
CEA LETI, France

B1L-E.4 **An Ultra-Low Power Low-IF GFSK Demodulator for Bluetooth-LE Applications 1226**
Marco Silva Pereira[3], João Caldinhas Vaz[3], Carlos Azeredo Leme[2], Jose Teixeira de Sousa[1], João Costa Freire[2]
[1]INESC-ID / Universidade de Lisboa, Portugal; [2]Instituto de Telecomunicações, Portugal; [3]Universidade de Lisboa / Instituto de Telecomunicações, Portugal

B1L-E.5 **A 0.54-mW Duty Controlled RSSI with Current Reusing Technique for Human Body Communication 1230**
Jaeeun Jang, Yongsu Lee, Hyunwoo Cho, Hoi-Jun Yoo
Korea Advanced Institute of Science and Technology, Korea, South

B1L-F: Circuits for Biomedical Applications

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Room: S6: A. Negreiros
Chair(s): Pedram Mohseni, *Case Western Reserve University*
Jennifer Blain Christen, *Arizona State University*

B1L-F.1 **An 8-Channel Power-Efficient Time-Constant-Enhanced Analog Front-End Amplifier for Neural Signal Acquisition 1234**
Jung-Chen Chung, Wei-Ming Chen, Chung-Yu Wu
National Chiao Tung University, Taiwan

B1L-F.2 **A 45V 10-b Electrode Monitoring Analog-to-Digital Converter 1238**
Edward Lee
Alfred Mann Foundation, United States

B1L-F.3 **A Sub GHz Mostly Digital BPSK IR UWB Transceiver 1242**
Lei Wang, Chun Huat Heng, Yong Lian
National University of Singapore, Singapore

B1L-F.4 **Dual-Channel Pulse-Width-Modulation ASIC for Isolated Bio-Signal Recording Front-End 1246**
Sheng-En Lin, Shi-Hao Ou, Robert Rieger
National Sun Yat-Sen University, Taiwan

B1L-F.5 **An Integrated CMOS Current Driver Using Nonlinear Feedback for Bioimpedance Applications 1250**
Nazanin Neshatvar, Peter Langlois, Dai Jiang, Andreas Demosthenous
University College London, United Kingdom

B1L-G: Data Converters II

Time: Tuesday, May 26 (09:30-11:00)
Room: S7: S. M. Breyner
Chair(s): Nuno Paulino, *UNINOVA*
Luis Hernandez, *Charles III University of Madrid*

B1L-G.1 **17-MS/s 9-Bit Cyclic ADC with Gain-Assisted MDAC and Attenuation-Based Calibration 1254**
Yuki Okada, Takashi Oshima
Hitachi, Ltd., Japan

B1L-G.2 **Spectral Analysis of Multibit VCO-ADCs and PFMADCs with Sinusoidal Inputs 1258**
Eric Gutierrez, Luis Hernandez
Universidad Carlos III de Madrid, Spain

B1L-G.3 **A New Highly-Linear Highly-Sensitive Differential Voltage-to-Time Converter Circuit in CMOS 65nm Technology 1262**
Abdullah El-Bayoumi, Hassan Mostafa, Ahmed M. Soliman
Cairo University, Egypt

B1L-G.4 **Stacking Integration Methodologies in 3D IC for 3D Ultrasound Image Processing Application: a Stochastic Flash ADC Design Case Study 1266**
Hourieh Attarzadeh[2], Sung Kyu Lim[1], Trond Ytterdal[2]
[1]Georgia Institute of Technology, United States; [2]Norwegian University of Science and Technology, Norway

B1L-G.5 **A Flash-TDC Hybrid ADC Architecture 1270**
Yue Xu, Ayman Shabra
Masdar Institute of Science and Technology, U.A.E.

B1L-H: Advanced Image/Video Coding

Time: Tuesday, May 26 (09:30-11:00)
Room: S8: G. Quartim
Chair(s): Nam Ling, *Santa Clara University*
Jing-Ming Guo, *National Taiwan University of Science and Technology*

B1L-H.1 **An Inter-Image Redundancy Measure for Image Set Compression 1274**
Xinfeng Zhang[1], Yabin Zhang[1], Weisi Lin[1], Siwei Ma[2], Wen Gao[2]
[1]Nanyang Technological University, Singapore; [2]Peking University, China

B1L-H.2 **Rate-Distortion and Energy Performance of HEVC and H.264/AVC Encoders: a Comparative Analysis 1278**
Eduarda Monteiro[2], Mateus Grellert[2], Sergio Bampi[2], Bruno Zatt[1]
[1]Universidade Federal de Pelotas, Brazil; [2]Universidade Federal do Rio Grande do Sul, Brazil

B1L-H.3 **Near-Aperiodic Dot-Diffused Block Truncation Coding.....1282**
Yun-Fu Liu[1], Jing-Ming Guo[1], Zong-Jhe Wu[1], Hua Lee[2]
[1]National Taiwan University of Science and Technology, Taiwan; [2]University of California, Santa Barbara, United States

B1L-H.4 **Efficient Coding Unit Size Selection for HEVC Downsizing Transcoding 1286**
Viet Anh Nguyen[1], Minh N. Do[2]
[1]Advanced Digital Sciences Center, Singapore; [2]University of Illinois at Urbana Champaign, United States

B1L-H.5 **Color Image Coding Based on the Colorization Algorithm Using Multiple Resolution Images.....1290**
Kazunori Uruma[2], Katsumi Konishi[1], Tomohiro Takahashi[2], Toshihiro Furukawa[2]
[1]Kogakuin University, Japan; [2]Tokyo University of Science, Japan

B1L-J: Wireless Circuits I

Time: Tuesday, May 26 (09:30-11:00)
Room: S9: M.H.V. Silva
Chair(s): Shu Wei, *Nanyang Technological University*
Joseph Chang, *Nanyang Technological University*

B1L-J.1 **A Low-Voltage Voltage-Controlled Ring-Oscillator Employing Dynamic-Threshold-MOS and Body-Biasing Techniques 1294**
Somayeh Abdollahvand, Luis Oliveira, Luis Gomes, João Goes
Universidade Nova de Lisboa, Portugal

B1L-J.2 **CMOS Distributed Amplifiers for UWB Radar 1298**
Kenneth Mæland, Kristian Gjertsen Kjelgård, Tor Sverre Lande
University of Oslo, Norway

B1L-J.3 **A Noise Cancelling Envelope Detector for Low Power Wireless Sensor Applications 1302**
Samer Idres, Mohamed El-Nozahi, Hani Ragai
Ain Shams University, Egypt

B1L-J.4 **A Fully Integrated 26 dBm Linearized RF Power Amplifier in 65 nm CMOS Technology 1306**
Waqas Ahmad[2], Leijun Xu[1], Markus Törmänen[2], Henrik Sjöland[2]
[1]Jiangsu University, China; [2]Lund University, Sweden

B1L-J.5 **A Fast AGC Method for Multimode Zero-IF/Sliding-IF WPAN/Ban Receivers 1310**
Jingjing Dong, Hanjun Jiang, Zhaoyang Weng, Jingyi Zheng, Chun Zhang, Zhihua Wang
Tsinghua University, China

B1L-K: Nonlinear Circuits and Systems I

Time: Tuesday, May 26 (09:30-11:00)
Room: S10: A.S. Cardoso
Chair(s): Sergio Callegari, *University of Bologna*
Marco Storace, *University of Genoa*

B1L-K.1 **A Quantized Pulse Coupled Oscillator for Slow Clocking of Peer-to-Peer Networks ...1314**
Enkhbayasgalan Gantsog[1], Alyssa Apsel[1], Frank Lane[2]
[1]Cornell University, United States; [2]Qualcomm Inc, United States

B1L-K.2 **Parameter Estimation from Nonlinear Frequency Response of MEMS Resonators 1318**
Alexis Brenes[3], Jérôme Juillard[1], Laurent Bourgois[1], Filipe Vinci Dos Santos[2]
[1]École supérieure d'électricité, France; [2]Thales Advanced Analog Design Chair, France; [3]Thales Avionics, France

B1L-K.3 **Modelling of the Dynamical Behaviour of Floating Electrode MEMS.....1322**
Panagiotis Giounanlis[2], Elena Blokhina[2], Orla Feely[2], Loukas Michalas[1], Matroni Koutsoureli[1], George Papaioannou[1]
[1]National and Kapodistrian University of Athens, Greece; [2]University College Dublin, Ireland

B1L-K.4 **A Low-Complexity Circuit Model of Hysteresis 1326**
Matteo Biggio, Flavio Stellino, Mauro Parodi, Marco Storace
Università degli Studi di Genova, Italy

B1L-K.5 **Multi-Layer Perceptron with Pulse Glial Chain Having Oscillatory Excitation Threshold 1330**
Chihiro Ikuta, Yoko Uwate, Yoshifumi Nishio
Tokushima University, Japan

B1L-L: Cellular Nanoscale Networks

Time: Tuesday, May 26 (09:30-11:00)
Room: S11: C. Telmo
Chair(s): Mustak Yalcin, *Istanbul Technical University*

B1L-L.1 **Local Asymmetric Propagation Stopper Circuit for Asynchronous Binary Wave Computing.....1334**
Ari Paasio
University of Turku, Finland

B1L-L.2 **In-Memory Adder Functionality in 1S1R Arrays 1338**
Anne Siemon[3], Stephan Menzel[1], Anupam Chattopadhyay[2], Rainer Waser[3], Eike Linn[3]
[1]Forschungszentrum Jülich GmbH, Germany; [2]Nanyang Technological University, Singapore; [3]Rheinisch-Westfälische Technische Hochschule Aachen, Germany

B1L-L.3 **Implementation of Nondeterministic Finite Automata in an Autoassociative CAM Circuit 1342**
Jussi Poikonen, Eero Lehtonen, Mika Laiho, Timo Knuutila
University of Turku, Finland

B1L-L.4 **An Event-Driven Massively Parallel Fine-Grained Processor Array 1346**
Declan Walsh, Piotr Dudek
University of Manchester, United Kingdom

B1L-L.5 **A 512x512-Cell Associative Cam/Willshaw Memory with Vector Arithmetic 1350**
Mika Laiho[2], Jonne Poikonen[2], Eero Lehtonen[2], Mikko Pänkäälä[2], Jussi Poikonen[2], Pentti Kanerva[1]
[1]University of California, Berkeley, United States; [2]University of Turku, Finland

B1L-M: Integrated Power Circuits and Charge Pumps

Time: Tuesday, May 26 (09:30-11:00)
Room: S12: D. Costa
Chair(s): Toru Tanzawa, *Micron Technology, Inc.*
Ke-Horng Chen, *National Chiao Tung University*

B1L-M.1 **An Analytical Model of Multi-Sine AC-DC Voltage Multiplier 1354**
Toru Tanzawa
Micron Japan, Ltd., Japan

B1L-M.2 **A Comprehensive Optimization Methodology for Designing Charge Pump Voltage Multipliers 1358**
Toru Tanzawa
Micron Japan, Ltd., Japan

B1L-M.3 **Variable-Output Charge-Pump for Piezoelectric and Electrostatic Tunable RF Filters 1362**
Mohammad Abu Khater, Dimitrios Peroulis
Purdue University, United States

B1L-M.4 **Implantable Biomedical Device Supplying by a 28nm CMOS Self-Calibration DC-DC Buck Converter with 97% Output Voltage Accuracy 1366**
Te-Fu Yang, Ru-Yu Huang, Yi-Ping Su, S. Balakumar, Ke-Horng Chen, Tsung-Yen Tsai, Jian-Ru Lin, Ying-Hsi Lin, Chao-Cheng Lee, Pei-Ling Tseng
National Chiao Tung University, Taiwan

B1L-M.5 **An All-Digital Power Management Unit with 90% Power Efficiency and Ns-Order Voltage Transition Time for DVS Operation in Low Power Sensing SoC Applications 1370**
Chung-Shiang Wu[2], Kai-Chun Lin[2], Yi-Ping Kuo[2], Po-Hung Chen[2], Yuan-Hua Chu[1], Wei Hwang[2]
[1]Industrial Technology Research Institute, Taiwan; [2]National Chiao Tung University, Taiwan

B2P-N: Multicore and 3D IC Design Issues

Time: Tuesday, May 26 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Vasilis Pavlidis, *University of Manchester*
Chuan Zhang, *Southeast University*

B2P-N.1 **On the Influence of Static Power Consumption in Multicore Embedded Systems 1374**
Arthur Francisco Lorenzon[2], Márcia Cristina Cera[1], Antonio Carlos S. Beck[2]
[1]Universidade Federal do Pampa, Brazil; [2]Universidade Federal do Rio Grande do Sul, Brazil

B2P-N.2 **A Configurable CMOS Memory Platform for 3D-Integrated Memristors 1378**
Melika Payvand, Advait Madhavan, Miguel Lastras-Montaño, Amirali Ghofrani, Justin Rofeh, Tim Cheng, Dmitri B. Strukov, Luke Theogarajan
University of California, Santa Barbara, United States

B2P-N.3 **A Multi-Core Architecture of Digital Back-End for Large Mutual Capacitance Touch Sensing Systems 1382**
Akihisa Yamada, Yan Qian, Masayuki Yamaguchi, Hirohi Honjoh, Takahiro Morishita, Shunsuke Nagasawa, Shinji Shinjo, Masayuki Miyamoto
Sharp Corporation, Japan

B2P-N.4 **A Memory-Efficient NoC System for OpenCL Many-Core Platform 1386**
Chien-Hsuan Yen, Chung-Ho Chen, Kuan-Chung Chen
National Cheng Kung University, Taiwan

B2P-P: Interconnects, Clock, Noise Immunity and ESD Protection Session

Time: Tuesday, May 26 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Alexander Fish, *Ben-Gurion University of the Negev*
Shuenn-Yuh Lee, *National Cheng Kung University*

B2P-P.1 **Design and Techniques for on-Die Power Integrity Noise Measurement System with Digital Output 1390**
Hyunho Baek, William Eisenstadt
University of Florida, United States

B2P-P.2 **180.5Mbps-8Gbps DLL-Based Clock and Data Recovery Circuit with Low Jitter Performance 1394**
Yuequan Liu, Yuan Wang, Song Jia, Xing Zhang
Peking University, China

B2P-P.3 **Switched Capacitor Quasi-Adiabatic Clocks 1398**
Hany Fahmy, Ping-Yao Lin, Riadul Islam, Matthew Guthaus
University of California, Santa Cruz, United States

B2P-P.4 **Multi-Frequency Resonant Clocks 1402**
Benjamin Lacara, Ping-Yao Lin, Matthew Guthaus
University of California, Santa Cruz, United States

B2P-P.5 **LC Resonant Clock Resource Minimization Using Compensation Capacitance 1406**
Ping-Yao Lin, Hany Fahmy, Riadul Islam, Matthew Guthaus
University of California, Santa Cruz, United States

B2P-Q: Memory Circuits and Architectures III

Time: Tuesday, May 26 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Viktor Öwall, *Lund University*
Hsie-Chia Chang, *National Chiao Tung University*

B2P-Q.1 **Statistical Analysis and Design of 6T SRAM Cell for Physical Unclonable Function with Dual Application Modes 1410**
Le Zhang, Chip Hong Chang, Zhi Hui Kong, Chao Qun Liu
Nanyang Technological University, Singapore

B2P-Q.2 **Analysis and Optimization for Dynamic Read Stability in 28nm SRAM Bitcells 1414**
Ahmed T. Elthakeb[1], Thomas Haine[2], Denis Flandre[2], Yehea Ismail[1], Hamdy Abd Elhamid[1], David Bol[2]
[1]American University in Cairo & Zewail City of Science and Technology, Egypt; [2]Universite' catholique de Louvain, Belgium

B2P-Q.3 **2T2M Memristor-Based Memory Cell for Higher Stability RRAM Modules 1418**
Noha Shaarawy[3], Maged Ghoneima[1], Ahmed Radwan[2]
[1]Ain Shams University, Egypt; [2]Cairo University, Egypt; [3]Nile University, Egypt

B2P-Q.4 **Reducing Misses to External Memory Accesses in Task-Level Pipelining 1422**
Ali Azarian, Joao Cardoso
Faculdade de Engenharia da Universidade do Porto, Portugal

B2P-Q.5 **Refresh-Free Dynamic Standard-Cell Based Memories: Application to a QC-LDPC Decoder 1426**
Pascal Meinerzhagen[2], Andrea Bonetti[1], Georgios Karakonstantis[1], Christoph Roth[3], Frank Gürkaynak[3], Andreas Burg[1]
[1]École Polytechnique Fédérale de Lausanne, Switzerland; [2]Intel Corporation, United States; [3]Universität Zürich and ETH Zürich, Switzerland

B2P-R: VLSI Datapath, Arithmetic, and Array Circuits

Time: Tuesday, May 26 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Hanho Lee, *Inha University*
Seok-Bum Ko, *University of Saskatchewan*

B2P-R.1 **Efficient Subquadratic Parallel Multiplier Based on Modified SPB of GF(2^m) 1430**
Jeng-Shyang Pan[3], Pramod Kumar Meher[2], Chiou-Yng Lee[1], Hong-Hai Bai[3]
[1]Lunghwa University of Science and Technology, Taiwan; [2]Nanyang Technological University, Singapore; [3]Shenzhen Graduate School of Harbin Institute of Technology, China

B2P-R.2 **Finite Element Emulation-Based Solver for Electromagnetic Computations.....1434**
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[1]Ain Shams University, Egypt; [2]Mentor Graphics Corporation, Egypt

B2P-R.3 **New Polynomial Basis Versatile Multiplier Over GF(2^m) for Low-Power on-Chip Crypto-Systems 1438**
Mustafa Khairallah, Maged Ghoneima
Ain Shams University, Egypt

B2P-R.4 **Enhanced Level Shifter for Multi-Voltage Operation.....1442**
Weicheng Liu[2], Emre Salman[2], Can Sitik[1], Baris Taskin[1]
[1]Drexel University, United States; [2]Stony Brook University, United States

B2P-S: VLSI Systems, Architectures and Applications

Time: Tuesday, May 26 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Chip Hong Chang, *Nanyang Technological University*
Hsie-Chia Chang, *National Chiao Tung University*

B2P-S.1 **A Mixed Cells Physical Design Approach 1446**
Daniel Guimarães Jr, Julia Puget, Ricardo Reis
Universidade Federal do Rio Grande do Sul, Brazil

B2P-S.2 **A 3.46 Gb/s (9141,8224) LDPC-based ECC Scheme and on-Line Channel Estimation for Solid-State Drive Applications 1450**
Kin-Chu Ho, Chih-Lung Chen, Yen-Chin Liao, Hsie-Chia Chang, Chen-Yi Lee
National Chiao Tung University, Taiwan

B2P-S.3 **Optimal DWA Design in Scaled CMOS Technologies for Mismatch Cancellation in Multibit Sigma-Delta ADCs 1454**
Alberto Celin, Andrea Gerosa
Università degli Studi di Padova, Italy

B2P-S.4 **Exploration of Self-Healing Circuits for Timing Resilient Design Using Emerging Memristor Devices 1458**
Jie Gu[1], Jieda Li[2]
[1]Northwestern University, United States; [2]Oracle Corporation, United States

B2P-S.5 **Tamper-Resistant Authentication System with Side-Channel Attack Resistant AES and PUF Using MDR-ROM 1462**
Mitsuru Shiozaki, Takaya Kubota, Tsunato Nakai, Akihiro Takeuchi, Takashi Nishimura, Takeshi Fujino
Ritsumeikan University, Japan

B2P-S.6 **Analysis and Characterization of Data Energy Tradeoffs for VLSI Architectural Agility in C-RAN Platforms 1466**
Pascal Nsame, Guy Bois, Yvon Savaria
École polytechnique de Montréal, Canada

B2P-T: Circuits and Systems for Communications II

Time: Tuesday, May 26 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Tokunbo Ogunfunmi, *Santa Clara University, USA*
Chuan Zhang, *Southeast University*

B2P-T.2 **Memory Impact on the Lifetime of a Wireless Sensor Node Using a Semi-Markov Model 1470**
Yasmin Halawani, Baker Mohammad, Mahmoud Al-Qutayri, Hani Saleh
Khalifa University, U.A.E.

B2P-U: Circuits and Systems for Communications III

Time: Tuesday, May 26 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Jaehyouk Choi, *UNIST*
Jongsun Park, *Korea University*

B2P-U.1 **A Temperature Independent Driver for Mach-Zehnder Modulators 1474**
Shenghao Liu, Ke Li, Peter Wilson
University of Southampton, United Kingdom

B2P-U.2 **Switched State-Space Model for a Switched-Capacitor Power Amplifier 1478**
Stefan Trampitsch[3], Gerhard Knoblinger[1], Mario Huemer[2]
[1]Intel Mobile Communications Austria GmbH, Austria; [2]Johannes Kepler Universität Linz, Austria; [3]Johannes Kepler Universität Linz / Intel Mobile Communications Austria GmbH, Austria

B2P-U.3 **Routing Design for Transmission Capacity Maximization in Complex Networks 1482**
Cuili Yang, Zhongyan Fan, Wallace Tang
City University of Hong Kong, Hong Kong

B2P-U.4 **A New Baseband Post-Distortion Technique for Power Amplifiers in OFDM-Based Cognitive Radio Systems 1486**
Mouna Ben Mabrouk, Guillaume Ferré, Eric Grivel, Nathalie Deltimple
University of Bordeaux, France

B2P-U.5 **A Modeling Approach for Mixed-Mode FMCW Synthesizer Allowing Frequency Error Analysis 1490**
Yizhe Hu, Wei Li
Fudan University, China

B2P-U.6 **Efficient Realization of Probabilistic Gradient Descent Bit Flipping Decoders.....1494**
Khoa Le[1], David Declercq[1], Fakhreddine Ghaffari[1], Christian Spagnol[2], Emmanuel Popovici[2], Predrag Ivanis[4], Bane Vasic[3]
[1]Université de Cergy-Pontoise, France; [2]University College Cork, Ireland; [3]University of Arizona, United States; [4]University of Belgrade, Serbia

B2P-V: MIMO Communications Systems II

Time: Tuesday, May 26 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Magdy Bayoumi, *University of Louisiana at Lafayette*
Chuan Zhang, *Southeast University*

B2P-V.1 **VLSI Design of Large-Scale Soft-Output MIMO Detection Using Conjugate Gradients 1498**
Bei Yin[2], Michael Wu[2], Joseph R. Cavallaro[2], Christoph Studer[1]
[1]Cornell University, United States; [2]Rice University, United States

B2P-V.2 **High Throughput Constant Envelope Pre-Coder for Massive MIMO Systems 1502**
Hemanth Prabhu, Fredrik Rusek, Joachim Rodrigues, Ove Edfors
Lund University, Sweden

B2P-V.3 **A Simplified Frequency Synthesizer Architecture Thanks to Interference Cancellation 1506**
Borislav Milevsky, Myriam Ariaudo, Jean-Luc Gautier, Inbar Fijalkow
Université de Cergy-Pontoise, France

B2P-V.4 **UWB Waveform Generator for Digital CMOS Radar 1510**
øystein Bjørndal[1], Svein-Erik Hamran[1], Tor Sverre Lande[2]
[1]Forsvarets forskningsinstitutt FFI, Norway; [2]University of Oslo, Norway

B2P-W: Neural Networks and Systems

Time: Tuesday, May 26 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Majid Ahmadi, *University of Windsor*

B2P-W.2 **Wave Computer Core Using Fixed-Point Arithmetic 1514**
Baris Karakaya[1], Ramazan Yeniçeri[2], Mustak E. Yalçin[2]
[1]Firat University, Turkey; [2]Istanbul Technical University, Turkey

B2P-W.5 **Modeling the Faulty Behaviour of Digital Designs Using a Feed Forward Neural Network Approach 1518**
Zeynab Mirzadeh[1], Jean-Francois Boland[1], Yvon Savaria[2]
[1]École de Technologie Supérieure, Canada; [2]École polytechnique de Montréal, Canada

B2P-W.6 **Memristor-Based Cellular Nonlinear Networks with Belief Propagation Inspired Algorithm 1522**
Jacopo Secco, Fernando Corinto
Politecnico di Torino, Italy

B2P-W.7 **Kernel-Based Mixture of Experts Models for Linear Regression 1526**
Joseph Santarcangelo, Xiao-Ping Zhang
Ryerson University, Canada

B3L-A: SPECIAL SESSION: Exploring Emerging Memories for Energy Efficient Systems

Time: Tuesday, May 26 (11:20-12:50)
Room: Main Auditorium
Chair(s): Aida Todri-Sanial, *Le Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier*
Vasilis Pavlidis, *University of Manchester*

B3L-A.1 **A Body-Biasing of Readout Circuit for STT-RAM with Improved Thermal Reliability...1530**
Lun Yang[1], Yuanqing Cheng[1], Yuhao Wang[3], Hao Yu[4], Weisheng Zhao[5], Aida Todri-Sanial[2]
[1]Beihang University, China; [2]Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, France; [3]Nanyang Technological Univeristy, Singapore; [4]Nanyang Technological University, Singapore; [5]Université Paris-Sud / Beihang Uni

B3L-A.2 **A Case of Precision-Tunable STT-RAM Memory Design for Approximate Neural Network 1534**
Ying Wang[2], Lili Song[2], Yinhe Han[2], Yuanqing Cheng[1], Huawei Li[2], Xiaowei Li[2]
[1]Beihang University, China; [2]Institute of Computing Technology, Chinese Academy of Sciences, China

B3L-A.3 **Energy-Efficient Neuromorphic Computation Based on Compound Spin Synapse with Stochastic Learning 1538**
Deming Zhang[1], Lang Zeng[1], Yuanzhuo Qu[1], Youguang Zhang[1], Mengxing Wang[1], Weisheng Zhao[3], Tianqi Tang[2], Yu Wang[2]
[1]Beihang University, China; [2]Tsinghua University, China; [3]Université Paris-Sud / Beihang University, China

B3L-A.4 **Logic-in-Memory Architecture Made Real.....1542**
Diego Pala, Giovanni Causapruno, Marco Vacca, Fabrizio Riente, Giovanna Turvani, Mariagrazia Graziano, Maurizio Zamboni
Politecnico di Torino, Italy

B3L-B: SPECIAL SESSION: Complexity in the Design of Systems-on-a-Chip

Time: Tuesday, May 26 (11:20-12:50)
Room: Small Auditorium
Chair(s): Dimitri Galayko, *UPMC - Sorbonne Universities*
Elena Blokhina, *University College Dublin*

B3L-B.1 **Understanding Complexity in Multiphysics Systems-on-a-Chip: Modern Approaches for Design 1546**
Elena Blokhina[3], Diarmuid O'Connell[3], Dennis Andrade-Miceli[3], Sergi Gorreta-Mariné[1], Joan Pons-Nin[1], Manuel Dominguez-Pumar[1], Orla Feely[3], Dimitri Galayko[2]
[1]Universitat Politècnica de Catalunya, Spain; [2]Université Pierre et Marie Curie / LIP6, France; [3]University College Dublin, Ireland

B3L-B.2 **Fine-Grain DVFS and AVFS Techniques for Complex SoC Design: an Overview of Architectural Solutions Through Technology Nodes..... 1550**
Edith Beigne, Fabien Clermidy, Didier Lattard, Ivan Miro-Panades, Yvain Thonnart, Pascal Vivet
CEA LETI, France

B3L-B.3 **Substrate Noise Modeling with Dedicated CAD Framework for Smart Power ICs 1554**
Hao Zou[2], Yasser Moursy[2], Ramy Iskander[2], Camillo Stefanucci[1], Pietro Buccella[1], Maher Kayal[1], Jean-Michel Sallese[1]
[1]École Polytechnique Fédérale de Lausanne, Switzerland; [2]Université Pierre et Marie Curie / LIP6, France

B3L-B.4 **Practical Considerations in VLSI IC Design Flow with Respect to Tool Limitations 1558**
Robert Sobot
Université de Cergy-Pontoise, France

B3L-C: Fault Tolerance and Error Correction in VLSI Circuits

Time: Tuesday, May 26 (11:20-12:50)
Room: S1: Luis F. Branco
Chair(s): Ricardo Reis, *Universidade Federal do Rio Grande do Sul*
Viktor Öwall, *Lund University*

B3L-C.1 **An Integrated Method for Implementing Online Fault Detection in NoC-Based MPSoCs 1562**
Vinicius Fochi, Eduardo Wächter, Augusto Erichsen, Alexandre Amory, Fernando Moraes
Pontifícia Universidade Católica do Rio Grande do Sul, Brazil

B3L-C.2 **A Hierarchical IP Protection Approach for Hard IP Cores 1566**
Qiang Liu, Haie Li
Tianjin University, China

B3L-C.3 **A Context Saving Fault Tolerant Approach for a Shared Memory Many-Core Architecture 1570**
Eduardo Wächter[2], Nicolas Ventroux[1], Fernando Moraes[2]
[1]CEA, LIST, Embedded Computing Laboratory, France; [2]Pontifícia Universidade Católica do Rio Grande do Sul, Brazil

B3L-C.4 **Test Set Customization for Improved Fault Diagnosis Without Sacrificing Coverage 1574**
Srinivasa Shashank Nuthakki, Santanu Chattopadhyay, Mrityunjoy Chakraborty
Indian Institute of Technology Kharagpur, India

B3L-C.5 **On the Reuse of Existing Error Tolerance Circuitry for Low Power Scan Testing..... 1578**
Anthi Anastasiou[2], Yiorgos Tsiatouhas[2], Angela Arapoyanni[1]
[1]University of Athens, Greece; [2]University of Ioannina, Greece

B3L-D: Digital Image Processing

Time: Tuesday, May 26 (11:20-12:50)
Room: S2: E. Andrade
Chair(s): Wan-Chi Siu, *Hongkong Polytechnique University*
Mrityunjoy Chakraborty, *Indian Institute of Technology, Kharagpur*

B3L-D.1 **Image Deblocking via Group Sparsity Optimization 1582**
Zhenbo Lu, Houqiang Li, Weiping Li
University of Science and Technology of China, China

B3L-D.2 **Spatial Affine Transformations of Images by Using Fractional Shift Fourier Transform.....1586**
Soo-Chang Pei, Yu-Zhe Hsiao
National Taiwan University, Taiwan

B3L-D.3 **Heavy Haze Removal in a Learning Framework 1590**
Jie Chen, Lap-Pui Chau
Nanyang Technological University, Singapore

B3L-D.4 **No-Reference Image Quality Assessment Using Shearlet Transform and Stacked Autoencoders.....1594**
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[1]Chu Hai College of Higher Education, China; [2]City University of Hong Kong, Hong Kong

B3L-E: Wireline Communications II

Time: Tuesday, May 26 (11:20-12:50)
Room: S5: F. Pessoa
Chair(s): Wei Xing Zheng, *University of Western Sydney*
Chang-Ho Lee, *Qualcomm*

B3L-E.1 **Delay Window Blind Oversampling Clock and Data Recovery Algorithm with Wide Tracking Range 1598**
Travis Bartley[1], Shuji Tanaka[1], Yutaka Nonomura[2], Takahiro Nakayama[3], Masanori Muroyama[1]
[1]Tohoku University, Japan; [2]Toyota Central R&D Labs., Inc., Japan; [3]Toyota Motor Corp., Japan

B3L-E.2 **On-Chip Jitter Tolerance Measurement Technique for CDR Circuits 1602**
Kyung-Sub Son, Kyongsu Lee, Jin-Ku Kang
Inha University, Korea, South

B3L-E.3 **Design of a Sample-and-Hold Analog Front End for a 56Gb/s PAM-4 Receiver Using 65nm CMOS 1606**
Khosrov Sadeghipour, Paul Townsend, Peter Ossieur
Tyndall National Institute, Ireland

B3L-E.4 **A 24-mW 28-Gb/s Wireline Receiver with Low-Frequency Equalizing CTLE and 2-Tap Speculative DFE 1610**
Minseo Kim, Joonsung Bae, Unsoo Ha, Hoi-Jun Yoo
Korea Advanced Institute of Science and Technology, Korea, South

B3L-E.5 **A Low-Power Pulse Position Modulation Transceiver 1614**
Woorham Bae, Chang-Soo Yoon, Deog-Kyoon Jeong
Seoul National University, Korea, South

B3L-F: CMOS Imagers and Bio applications

Time: Tuesday, May 26 (11:20-12:50)
Room: S6: A. Negreiros
Chair(s): Angel Rodríguez-Vázquez, *University of Seville*
Bo Zhao, *Tsinghua University*

B3L-F.1 **A 23µW Digitally Controlled pMUT Interface Circuit for Doppler Ultrasound Imaging.....1618**
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B3L-F.2 **A Compact NIR Fluorescence Imaging System with Goggle Display for Intraoperative Guidance.....1622**
Shengkui Gao[2], Suman Mondal[2], Nan Zhu[1], Rongguang Liang[1], Samuel Achilefu[2], Viktor Gruev[2]
[1]University of Arizona, United States; [2]Washington University in St. Louis, United States

B3L-F.3 **A Fluorescence Based Endoscopic Microcancer Detection Capsule.....1626**
Panayiota Demosthenous, Julius Georgiou
University of Cyprus, Cyprus

B3L-F.4 **A CMOS Analog SiPM Front-End for Positron Emission Tomography Application.....1630**
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Fondazione Bruno Kessler, Italy

B3L-F.5 **Frame Adaptive ROI for Photoplethysmography Signal Extraction from Fingertip Video Captured by Smartphone.....1634**
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[1]Chu Hai College of Higher Education, Hong Kong; [2]City University of Hong Kong, Hong Kong

B3L-G: Data Converters III

Time: Tuesday, May 26 (11:20-12:50)
Room: S7: S. M. Breyner
Chair(s): Luis Hernandez, *Charles III University of Madrid*
Nuno Paulino, *UNINOVA*

B3L-G.1 **A Delta-Sigma ADC Using an LSB-First SAR Quantizer 1638**
Allen Waters, Jerry Leung, Manideep Gande, Un-Ku Moon
Oregon State University, United States

B3L-G.2 **Design of a Variable-Delay Window ADC for Switched-Mode DC-DC Converters 1642**
Yin Sun, Victor Adrian, Joseph Sylvester Chang
Nanyang Technological University, Singapore

B3L-G.3 **Design of a Low Power Time to Digital Converter for Flow Metering Applications 1646**
Alberto Demarziani[2], Edoardo Bonizzoni[2], Franco Maloberti[2], Alessandro D'Amato[1]
[1]Texas Instruments Inc., Italy; [2]Università degli Studi di Pavia, Italy

B3L-G.4 **A 9-Bit Body-Biased Vernier Ring Time-to-Digital Converter in 65 nm CMOS Technology 1650**
Jun Jie Kong, Liter Siek, Chiang Liang Kok
Nanyang Technological University, Singapore

B3L-G.5 **Selectable Starting Bit SAR ADC.....1654**
Jerry Leung, Allen Waters, Un-Ku Moon
Oregon State University, United States

B3L-H: High Efficiency Video Coding/Communication and Image Processing

Time: Tuesday, May 26 (11:20-12:50)
Room: S8: G. Quartim
Chair(s): Hsu-Feng Hsiao, *National Chiao Tung University*
Jiang Tao Wen, *Tsinghua University, Beijing*

B3L-H.1 **Adaptive Configuration of Cloud Video Transcoding 1658**
Ming Yang[1], Jianfei Cai[1], Weiwen Zhang[1], Yonggang Wen[1], Chuan Heng Foh[2]
[1]Nanyang Technological University, Singapore; [2]University Of Surrey, United Kingdom

B3L-H.2 **Kvazaar HEVC Encoder for Efficient Intra Coding..... 1662**
Marko Viitanen, Ari Koivula, Ari Lemmetti, Jarno Vanne, Timo Hämäläinen
Tampere University of Technology, Finland

B3L-H.3 **QoS-Driven Optimization for Video Streaming Using Layer-Aligned Multipriority Rateless Codes 1666**
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National Chiao Tung University, Taiwan

B3L-H.4 **Image Compressive Sensing Using Overlapped Block Projection and Reconstruction 1670**
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[1]Harbin Institute of Technology, China; [2]Peking University, China

B3L-H.5 **High Accuracy Sub-Pixel Image Registration Under Noisy Condition..... 1674**
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[1]Harbin Institute of Technology, China; [2]Peking University, China

B3L-J: Wireless Circuits II

Time: Tuesday, May 26 (11:20-12:50)
Room: S9: M.H.V. Silva
Chair(s): Luis Oliveira, *Universidade Nova de Lisboa*
Thierry Taris, *IMS*

B3L-J.1 **A Wide Band CMOS Radio Frequency RMS Power Detector with 42-dB Dynamic Range 1678**
Jiayi Wang, Yongan Zheng, Fan Yang, Fan Tian, Huailin Liao
Peking University, China

B3L-J.2 **Tunable Multiband RF CMOS Active Filter Arrays.....1682**
Nilan Udayanga[1], Arjuna Madanayake[1], Chamith Wijenayake[1], Peyman Ahmadi[2], Leonid Belostotski[2]
[1]University of Akron, United States; [2]University of Calgary, Canada

B3L-J.3 **A 2.4-GHz Low Complexity Polar Transmitter Using Dynamic Biasing for IEEE 802.15.6 .....1686**
Vladimir Kopta[1], Raghavasimhan Thirunarayanan[2], Franz Pengg[3], Erwan Le Roux[3], Christian Enz[1]
[1]École Polytechnique Fédérale de Lausanne, Switzerland; [2]École Polytechnique Fédérale de Lausanne / Swiss Center for Electronics and Microtechnology, Switzerland; [3]Swiss Center for Electronics and Microtechnology, Switzerland

B3L-J.4 **An Injection-Locked Oscillator-Multiplier Circuitry Suitable for MB-OFDM Clock Generation.....1690**
Tero Koivisto
University of Turku, Finland

B3L-J.5 **Loss Mechanisms and Switching Performance Analysis for Efficient mm-Waves Class-E PAs 1694**
Omar El-Aassar, Mohamed El-Nozahi, Hani Ragai
Ain Shams University, Egypt

B3L-K: Chaos, Bifurcation and Nonlinear Phenomena

Time: Tuesday, May 26 (11:20-12:50)
Room: S10: A.S. Cardoso
Chair(s): Zbigniew Galias, *AGH-University of Science and Technology*
Michael Tse, *Hong Kong Polytechnic University*

B3L-K.1 **Detection of All Low-Period Windows for the Logistic Map 1698**
Zbigniew Galias, Bartlomiej Garda
AGH University of Science and Technology, Poland

B3L-K.2 **Numerically Efficient Robustness Test for Nonlinear Circuit Models.....1702**
Alessandro Colombo
Politenico di Milano, Italy

B3L-K.3 **Universal Nonlinear Phenomena in a Class of Electronic Oscillators 1706**
Peter Harte[2], Eoghan O'Riordan[2], Elena Blokhina[2], Orla Feely[2], Dimitri Galayko[1]
[1]Université Pierre et Marie Curie / LIP6, France; [2]University College Dublin, Ireland

B3L-K.4 **Bifurcation Study of Three-Phase Inverter System with Interacting Loads.....1710**
Yining Li[1], Zhen Li[1], Siu-Chung Wong[2], Xi Chen[3], Zhen Chen[1], Xiangdong Liu[1]
[1]Beijing Institute of Technology, China; [2]Hong Kong Polytechnic University, Hong Kong; [3]State Grid Information & Telecommunication Company Ltd, China

B3L-K.5 **Analysis of Even-Order Terms in Memoryless and Quasi-Memoryless Polynomial Baseband Models 1714**
Harald Enzinger[2], Karl Freiberger[2], Christian Vogel[1]
[1]FH Joanneum - University of Applied Sciences and Graz University of Technology, Austria; [2]FTW Telecommunications Research Center Vienna, Austria

B3L-L: Sensory Systems and Processing

Time: Tuesday, May 26 (11:20-12:50)
Room: S11: C. Telmo
Chair(s): Teresa Serrano Gotarredona, *Instituto de Microlectronica de Sevilla*
Chen Shoushun, *Nanyang Technological University*

B3L-L.1 **GEMINI: a Triple-GEM Detector Read-Out Mixed-Signal ASIC in 180 nm CMOS.....1718**
Alessandro Pezzotta[2], Giovanni Corradi[1], Gabriele Croci[2], Marcello De Matteis[2], Fabrizio Murtas[1], Giuseppe Gorini[2], Andrea Baschirotto[2]
[1]INFN Laboratori Nazionali di Frascati, Italy; [2]Università degli Studi Milano-Bicocca, Italy

B3L-L.2 **A Novel on-Site Deployment, Commissioning and Debugging Technique to Assess and Validate WSN Based Smart Systems.....1722**
Gabriel Mujica, Alejandro Garcia, Javier Gordillo, Jorge Portilla, Teresa Riesgo
Universidad Politecnica de Madrid, Spain

B3L-L.3 **Distributed Anti-Flocking Control for Mobile Surveillance Systems.....1726**
Nuwan Ganganath, Chi-Tsun Cheng, Chi Kong Tse
Hong Kong Polytechnic University, Hong Kong

B3L-L.4 **An Automatic Tuning Technique for Background Frequency Calibration in Gyroscope Interfaces Based on High Order Bandpass Delta-Sigma Modulators.....1730**
Mohamed Nabil Afifi, Michael Maurer, Thorsten Hehn, Armin Taschwer, Yiannos Manoli
Albert-Ludwigs-Universität Freiburg / IMTEK, Germany

B3L-L.5 **Current-Mode Automated Quality Control Cochlear Resonator for Bird Identity Tagging.....1734**
Diederik Paul Moeys, Tobias Delbrück, Shih-Chii Liu
Universität Zürich and ETH Zürich, Switzerland

B3L-M: High Efficiency Converters and Drive Circuits

Time: Tuesday, May 26 (11:20-12:50)
Room: S12: D. Costa
Chair(s): Marian Kazimierczuk, *Wright State University*
Hirotaka Koizumi, *Tokyo University of Science*

B3L-M.1 **An All-Digital PWM Generator with 62.5ps Resolution in 28nm CMOS Technology.....1738**
Sebastian Höppner, Stefan Haenzsche, Stefan Scholze, René Schüffny
Technische Universität Dresden, Germany

B3L-M.2 **A 20 V, 8 MHz Resonant DCDC Converter with Predictive Control for 1 ns Resolution Soft-Switching 1742**
Tobias Funk[1], Juergen Wittmann[1], Thoralf Rosahl[2], Bernhard Wicht[1]
[1]Hochschule Reutlingen, Germany; [2]Robert Bosch GmbH, Germany

B3L-M.3 **Self-Adjustable Feed-Forward Control and Auto-Tracking Off-Time Control Techniques for 95% Accuracy and 95% Efficiency AC-DC Non-Isolated LED Driver ...1746**
Hsin Chen[2], Chi-Wei Chen[2], Hsueh-Yi Hsieh[2], Ke-Horng Chen[2], Tsung-Yen Tsai[3], Jian-Ru Lin[3], Ying-Hsi Lin[3], Chao-Cheng Lee[3], Pei-Ling Tseng[1]
[1]Industrial Technology Research Institute, Taiwan; [2]National Chiao Tung University, Taiwan; [3]Realtek Semiconductor Corp., Taiwan

B3L-M.4 **A 12A 50V Half-Bridge Gate Driver for Enhancement-Mode GaN HEMTs with Digital Dead-Time Correction.....1750**
Ziang Chen, Yat-To Wong, Tak-Sang Yim, Wing-Hung Ki
Hong Kong University of Science and Technology, Hong Kong

B3L-M.5 **99% High Accuracy Knee Voltage Detection for Primary-Side Control in Flyback Converter.....1754**
Tsung-Hsun Tsai, Ke-Horng Chen, Tsung-Yen Tsai, Jian-Ru Lin, Ying-Hsi Lin, Chao-Cheng Lee, Pei-Ling Tseng
National Chiao Tung University, Taiwan

B4L-B: SPECIAL SESSION: Wireless Bio-Electronic Interfaces for in-Vivo Studies

Time: Tuesday, May 26 (14:10-15:40)
Room: Small Auditorium
Chair(s): Maysam Ghovanloo, *Georgia Institute of Technology*
Benoit Gosselin, *Laval University*

B4L-B.1 **A Wireless Multichannel Optogenetic Headstage with on-the-Fly Spike Detection.....1758**
Gabriel Gagnon Turcotte, Charles-Olivier Dufresne Camaro, Alireza Avakh Kisomi, Reza Ameli, Benoit Gosselin
Université Laval, Canada

B4L-B.2 **A 64 Pixel ISFET-Based Biosensor for Extracellular pH Gradient Monitoring 1762**
Ghazal Nabovati[1], Ebrahim Ghafar-Zadeh[2], Mohamad Sawan[1]
[1]École polytechnique de Montréal, Canada; [2]York University, Canada

B4L-B.3 **An FPGA Platform for Generation of Stimulus Triggering Based on Intracortical Spike Activity in Brain-Machine-Body Interface (BMBI) Applications.....1766**
Shahab Shahdoost, Pedram Mohseni
Case Western Reserve University, United States

B4L-B.4 **Towards a Three-Phase Time-Multiplexed Planar Power Transmission to Distributed Implants 1770**
Byunghun Lee[1], Maysam Ghovanloo[1], Dukju Ahn[2]
[1]Georgia Institute of Technology, United States; [2]University of California, San Diego, United States

B4L-B.5 **Full System for Translational Studies of Personalized Medicine with Free-Moving Mice 1774**
Sandro Carrara, Camilla Baj-Rossi, Sara Seyedeh Ghoreishizadeh, Stefano Riario, Grégoire Surrel, Francesca Stradolini, Cristina Boero, Giovanni De Micheli, Enver G. Kilinc, Catherine Dehollain
École Polytechnique Fédérale de Lausanne, Switzerland

B4L-C: VLSI for Communication and Signal Processing

Time: Tuesday, May 26 (14:10-15:40)
Room: S1: Luis F. Branco
Chair(s): Hanho Lee, *Inha University*
Shuenn-Yuh Lee, *National Cheng Kung University*

B4L-C.1 **Memory-Efficient Discrete Wavelet Transform Architecture Based on Wordlength Optimization 1778**
Yusong Hu, Ching Chuen Jong
Nanyang Technological University, Singapore

B4L-C.2 **An Efficient Processor for Joint Barrel Distortion Correction and Color Demosaicking 1782**
Hui-Sung Jeong, Tae-Hwan Kim
Korea Aerospace University, Korea, South

B4L-C.3 **A Hardware-Efficient Deblocking Filter Design for HEVC 1786**
Chih-Chung Fang, I-Wen Chen Chen, Tian Sheuan Chang
National Chiao Tung University, Taiwan

B4L-C.4 **A 3.13nJ/Sample Energy-Efficient Speech Extraction Processor for Robust Speech Recognition in Mobile Head-Mounted Display Systems 1790**
Jinmook Lee, Seongwook Park, Injoon Hong, Hoi-Jun Yoo
Korea Advanced Institute of Science and Technology, Korea, South

B4L-C.5 **An Efficient Max-Log Map Algorithm for VLSI Implementation of Turbo Decoders 1794**
Arash Ardakani, Mahdi Shabany
Sharif University of Technology, Iran

B4L-D: Education in Circuits and Systems

Time: Tuesday, May 26 (14:10-15:40)
Room: S2: E. Andrade
Chair(s): Babak Ayazifar, *University of California, Berkeley*
Joos Vandewalle, *Katholieke Universiteit Leuven*

B4L-D.1 **XbarSim: an Educational Simulation Tool for Memristive Crossbar-Based Circuits....1798**
Ioannis Vourkas, Dimitrios Stathis, Georgios Ch. Sirakoulis
Dimocritus University of Thrace, Greece

B4L-D.2 **Teaching Delta-Sigma Modulators with PyDSM and Scientific Python 1802**
Sergio Callegari[2], Federico Bizzarri[1]
[1]Politecnico di Milano, Italy; [2]Università di Bologna, Italy

B4L-D.3 **A Systematic Approach to the Time-Domain Computation of the Impulse Response and Post-Initial Conditions of Causal LTI systems at the Origin.....1806**
Vedat Tavsanoglu
Isik University Istanbul, Turkey

B4L-D.4 **An Interactive Program for Automatic Network Function Generation with Insights.....1810**
Yanjie Gu, Guoyong Shi
Shanghai Jiao Tong University, China

B4L-J: Analog Signal Processing Circuits

Time: Tuesday, May 26 (14:10-15:40)
Room: S9: M.H.V. Silva
Chair(s): Robert Sobot, *University of Cergy-Pontoise*
Vadim Ivanov, *Texas Instruments*

B4L-J.1 **Energy Efficient Transconductor for Widely Programmable Analog Circuits and Systems 1814**
Alonso Morgado, Rocío Del Río, Jose M. de la Rosa
Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, Spain

B4L-J.2 **1-V Continuous-Time Linear Equalizer for Up to 2 Gb/s Over 50-m Si-POF 1818**
Cecilia Gimeno, Erick Guerrero, Carlos Sánchez-Azqueta, Guillermo Royo, Concepción Aldea, Santiago Celma
Universidad de Zaragoza, Spain

B4L-J.3 **A Second-Order Noise-Shaping Time-to-Digital Converter Using Switched-Ring Oscillator 1822**
Mohamed Atef, Mohamed El-Nozahi, Emad Hegazi
Ain Shams University, Egypt

B4L-J.4 **Wide Linear Range Voltage-Controlled Delay Unit for Time-Mode Signal Processing 1826**
Soheyl Ziabakhsh[1], Ghyslain Gagnon[1], Gordon Roberts[2]
[1]École de Technologie Supérieure, Canada; [2]McGill University, Canada

B4L-J.5 **An Integrated Time Register and Arithmetic Circuit with Combined Operation for Time-Domain Signal Processing 1830**
Daewoong Lee, Dongil Lee, Taeho Lee, Yong-Hun Kim, Lee-Sup Kim
Korea Advanced Institute of Science and Technology, Korea, South

B4L-K: Digital VLSI Circuits

Time: Tuesday, May 26 (14:10-15:40)
Room: S10: A.S. Cardoso
Chair(s): Oscar Gustafsson, *Linköping University, Sweden*
Magdy Bayoumi, *University of Louisiana at Lafayette*

B4L-K.1 **XOR-Decomposition Principle and its Use to Build a Glitch-Free Maximum-Speed Arbitrary Binary Waveform Generator and Deglitcher 1834**
Volnei Pedroni
Universidade Tecnológica Federal do Paraná, Brazil

B4L-K.2 **A Study for Replacing CMOS Gates by Equivalent Inverters 1838**
Christina Galani, Andreas Tsormpatzoglou, Panagiotis Chaourani, Ioannis Messaris, Spyridon Nikolaidis
Aristotle University of Thessaloniki, Greece

B4L-K.3 **MIL-STD-1553+: Integrated Remote Terminal and Bus Controller at 100-MB/s Data Rate 1842**
Prateek Pendyala[2], Vijaya Sankara Rao Pasupureddi[1]
[1]Indian Institute of Technology Ropar, India; [2]International Institute of Information Technology Hyderabad, India

B4L-K.4 **DPA Vulnerability Analysis on Trivium Stream Cipher Using an Optimized Power Model 1846**
Erica Tena-Sánchez, Antonio Acosta
Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, Spain

B4L-K.5 **An Overlap-Contention Free True-Single-Phase Clock Dual-Edge-Triggered Flip-Flop 1850**
Andrea Bonetti, Adam Teman, Andreas Burg
École Polytechnique Fédérale de Lausanne, Switzerland

B4L-L: Innovations in System Simulation, Testing and Verification

Time: Tuesday, May 26 (14:10-15:40)
Room: S11: C. Telmo
Chair(s): Fernando Moraes, *PUCRS (Rio Grande do Sul Catholic University, at Porto Alegre)*

B4L-L.1 **VHDL-AMS Virtual Prototyping of a Generator Circuit Breaker Ablation Monitoring System 1854**
Qianqian Ha[2], Yannick Maret[1], Juan Sebastian Rodriguez Estupiñan[2], Alain Vachoux[2]
[1]ABB Ltd., Switzerland; [2]École Polytechnique Fédérale de Lausanne, Switzerland

B4L-L.2 **Simple and Accurate Single Event Charge Collection Macro Modeling for Circuit Simulation 1858**
Aymeric Privat, Lawrence Clark
Arizona State University, United States

B4L-L.3 **Verification of Arithmetic Datapath Designs Using Word-Level Approach - a Case Study 1862**
Cunxi Yu, Walter Brown, Maciej Ciesielski
University of Massachusetts, Amherst, United States

B4L-L.4 **Comparative Review of NoCs in the Context of ASICs and FPGAs 1866**
Khaled A. Helal, Sameh Attia, Tawfik Ismail, Hassan Mostafa
Cairo University, Egypt

B4L-L.5 **Dynamic Nets-to-TSVs Assignment in 3D Floorplanning 1870**
Mohammad Ahmed, Sucheta Mohapatra, Malgorzata Chrzanowska-Jeske
Portland State University, United States

B4L-M: Circuits & Systems for Power Systems

Time: Tuesday, May 26 (14:10-15:40)
Room: S12: D. Costa
Chair(s): Chika Nwankpa, *Drexel University*
Luis Fernando Costa Alberto, *University of São Paulo, Brazil*

B4L-M.1 **MEMS Optical Position Sensor for Sun Tracking 1874**
David Welch, Jennifer Blain Christen
Arizona State University, United States

B4L-M.2 **Modeling Power Consumption for DVFS Policies 1879**
Fábio Diniz Rossi, Mauro Storch, Israel de Oliveira, César De Rose
Pontifícia Universidade Católica do Paraná, Brazil

B4L-M.3 **Measurement Location Analysis for Information Embedded Power Systems 1883**
Tiffany Lakins, Chika Nwankpa
Drexel University, United States

B4L-M.4 **Semidefinite Relaxations of Equivalent Optimal Power Flow Problems: an Illustrative Example 1887**
Daniel Molzahn, Sina Baghsorkhi, Ian Hiskens
University of Michigan, United States

B4L-M.5 **A Study of Time Window Selection for Electric Power Distribution System Analysis 1891**
Nicholas Coleman, Karen Miu
Drexel University, United States

B6P-N: Live Demos

Time: Tuesday, May 26 (15:40-17:15)
Room: 2nd Floor Foyer
Chair(s): Pantelis Georgiou, *Imperial College*
Joao Oliveira, *Universidade Nova de Lisboa*

B6P-N.1 **A Wireless Panoramic Endoscope System Design and Implementation for Minimally Invasive Surgery 1895**
Ching-Hwa Cheng[2], Sheng-Ping Hung[2], Jiun-In Guo[3], Kai-Che Liu[1], Chi-Hsiang Wu[1]
[1]Chang Bing Show Chwan Memorial Hospital, Taiwan; [2]Feng Chia University, Taiwan; [3]National Chiao-Tung University, Taiwan

B6P-N.2 **Live Demonstration: an Ultra-Low Power PFM IRUWB System for Short-Range Audio Streaming 1896**
Matteo Stoppa, Danilo Demarchi, Marco Crepaldi
Istituto Italiano di Tecnologia, Italy

B6P-N.3 **Live Demonstration : Efficient Event-Driven Approach Using Synchrony Processing for Hardware Spiking Neural Networks 1897**
Guillaume Séguin-Godin, Frédéric Mailhot, Jean Rouat
Université de Sherbrooke, Canada

B6P-N.4 **Live Demonstration: Mixed-Signal Network Analysis Characterization and Modeling Platform 1898**
Pedro Miguel Cruz[2], Diogo Ribeiro[2], André Prata[2], Nuno Borges Carvalho[2], Marc Vanden Bossche[1]
[1]National Instruments Belgium, Belgium; [2]Universidade de Aveiro, Portugal

B6P-N.5 **Live Demonstration: Gaussian Pyramid Extraction with a CMOS Vision Sensor 1899**
Manuel Suárez[2], Víctor Brea[2], Jorge Fernández-Berni[1], Ricardo Carmona-Galán[1], Diego Cabello[2], Ángel Rodríguez-Vázquez[1]
[1]Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, Spain; [2]Universidade de Santiago de Compostela, Spain

B6P-N.6 **Live Demonstration: Real-Time High Dynamic Range Video Acquisition Using in-Pixel Adaptive Content-Aware Tone Mapping Compression 1900**
Sonia Vargas-Sierra, Gustavo Liñán-Cembrano, Ángel Rodríguez-Vázquez
Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, Spain

B6P-N.7 **Live Demonstration: Handwritten Digit Recognition Using Spiking Deep Belief Networks on SpiNNaker 1901**
Evangelos Stromatias[3], Daniel Neil[1], Francesco Galluppi[2], Michael Pfeiffer[1], Shih-Chii Liu[1], Steve Furber[3]
[1]Universität Zürich and ETH Zürich, Switzerland; [2]Université Pierre et Marie Curie, France; [3]University of Manchester, United Kingdom

B6P-N.8 **Live Demonstration: a Dynamically Adaptable Image Processing Application Running in an FPGA-Based WSN Platform 1902**
Alfonso Rodríguez, Juan Valverde, Cesar Castañares, Jorge Portilla, Eduardo de la Torre, Teresa Riesgo
Universidad Politecnica de Madrid, Spain

B6P-N.9 **Live Demonstration: Real-Time Event-Driven Object Recognition on SpiNNaker 1903**
Garrick Orchard[1], Xavier Lagorce[2], Christoph Posch[2], Steve Furber[3], Ryad Benosman[2], Francesco Galluppi[2]
[1]National University of Singapore, Singapore; [2]Université Pierre et Marie Curie, France; [3]University of Manchester, United Kingdom

B6P-N.10 **Live Demonstration: a HMM-Based Real-Time Sign Language Recognition System with Multiple Depth Sensors 1904**
Kai Yin Fok, Chi-Tsun Cheng, Nuwan Ganganath
Hong Kong Polytechnic University, Hong Kong

B6P-N.11 **Live Demonstration: Spiking Neural Circuit Based Navigation Inspired by C. Elegans Thermotaxis 1905**
Chirag Shetty, Sri Nitchith, Rishabh Rawat, Nandakumar S. R., Pritesh Shah, Shruti Kulkarni, Bipin Rajendran
Indian Institute of Technology Bombay, India

B6P-N.13 **Live Demonstration: a CMOS ASIC for Precise Reading of a Magnetoresistive Sensor Array for NDT 1906**
Diogo Caetano[1], Moisés Piedade[1], João Graça[1], Jorge Fernandes[1], Luis Rosado[2], Tiago Costa[1]
[1]INESC-ID / Universidade de Lisboa, Portugal; [2]Universidade de Lisboa / Instituto Superior Técnico, Portugal

B6P-N.14 **Live Demonstration: Real-Time Motor Rotation Frequency Detection by Spike-Based Visual and Auditory AER Sensory Integration for FPGA 1907**
Antonio Rios-Navarro, Elena Cerezuela-Escudero, Manuel Dominguez-Morales, Angel Jimenez-Fernandez, Gabriel Jimenez-Moreno, Alejandro Linares-Barranco
Universidad de Sevilla, Spain

B6P-N.15 **Live Demonstration: Real-Time Free Viewpoint Synthesis Using Three-Camera Disparity Estimation Hardware 1908**
Abdulkadir Akin, Raffaele Capoccia, Jonathan Narinx, Jonathan Masur, Alexandre Schmid, Yusuf Leblebici
École Polytechnique Fédérale de Lausanne, Switzerland

B6P-N.16 **Live Demonstration: XbarSim: an Educational Simulation Tool for Memristive Crossbar-Based Circuits 1909**
Ioannis Vourkas, Dimitrios Stathis, Georgios Ch. Sirakoulis
Dimocritus University of Thrace, Greece

B6P-N.17 **Live Demonstration: a Compact NIR Fluorescence Imaging System Design with Goggle Display for Intraoperative Guidance 1910**
Shengkui Gao[2], Suman Mondal[2], Nan Zhu[1], Rongguang Liang[1], Samuel Achilefu[2], Viktor Gruev[2]
[1]University of Arizona, United States; [2]Washington University in St. Louis, United States

B6P-N.18 **Live Demonstration: a 1300 x 800, 700 mW, 30 fps Spectral Polarization Imager 1911**
Missael Garcia, Shengkui Gao, Christopher Edmiston, Timothy York, Viktor Gruev
Washington University in St. Louis, United States

B6P-N.19 **Live Demonstration: Wearable Electronics for a Smart Garment Aiding Rehabilitation 1912**
Irina Ionela Spulber[2], Yen-Ming Chen[2], Enrica Papi[2], Salzitsa Anastasova-Ivanova[3], Jeroen Bergmann[1], Alison McGregor[2], Pantelis Georgiou[2]
[1]Brain Sciences Foundation and Massachusetts Institute of Technology, United States; [2]Imperial College London, United Kingdom; [3]Queen Marry University of London, United Kingdom

C1L-A: Emerging Device and Circuit Technologies I

Time: Wednesday, May 27 (09:30-11:00)
Room: Main Auditorium
Chair(s): Chen-Hao Chang, *National Chung Hsing University*
Koushik Maharatna, *University of Southampton*

C1L-A.1 **High Robustness Energy- and Area-Efficient Dynamic-Voltage-Scaling 4-Phase 4-Rail Asynchronous-Logic Network-on-Chip (ANoC) 1913**
Weng-Geng Ho, Kwen-Siong Chong, Kyaw Zwa Lwin Ne, Bah-Hwee Gwee, Joseph Sylvester Chang
Nanyang Technological University, Singapore

C1L-A.2 **New Triple-Transistor Based Defect-Tolerant Systems for Reliable Digital Architectures 1917**
Atin Mukherjee, Anindya Dhar
Indian Institute of Technology Kharagpur, India

C1L-A.3 **Redesigning Commercial Floating-Gate Memory for Analog Computing Applications 1921**
Farnood Merrikh Bayat[3], Xinjie Guo[3], Henry A. Om'mani[1], Nhan Do[1], Konstantin K. Likharev[2], Dmitri B. Strukov[3]
[1]Microchip Technology Inc., United States; [2]Stony Brook University, United States; [3]University of California, Santa Barbara, United States

C1L-A.4 **Evaluation of Interconnect Fabrics for an Embedded MPSoC in 28 nm FD-SOI 1925**
Gregor Sievers[2], Johannes Ax[2], Nils Kucza[2], Martin Flaßkamp[2], Thorsten Jungeblut[2], Wayne Kelly[1], Mario Porrmann[2], Ulrich Rückert[2]
[1]Queensland University of Technology, Australia; [2]Universität Bielefeld, Germany

C1L-A.5 **Multilayer Molybdenum Disulfide (MoS2) Based Tunnel Transistor 1929**
Muhammad Sanaullah, Masud Chowdhury
University of Missouri-Kansas City, United States

C1L-B: SPECIAL SESSION: Advances in Analog CAD Tools

Time: Wednesday, May 27 (09:30-11:00)
Room: Small Auditorium
Chair(s): Esteban Tlelo-Cuautle, *INAOE, Mexico*
Nuno Horta, *Instituto Superior Técnico, Lisboa, Portugal*

C1L-B.1 **OCBA in the Yield Optimization of Analog Integrated Circuits by Evolutionary Algorithms 1933**
Ivick Guerra-Gomez[3], Esteban Tlelo-Cuautle[2], Luis Gerardo de la Fraga[1]
[1]Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional, Mexico; [2]Instituto Nacional de Astrofísica, Óptica y Electrónica, Mexico; [3]SEMTECH-Snowbush IP, Mexico

C1L-B.2 **Automatic Design of High-Order SC Filter Circuits 1937**
Hugo Serra, Rui Santos-Tavares, João Goes
Universidade Nova de Lisboa, Portugal

C1L-B.3 **Design Space Exploration Using Hierarchical Composition of Performance Models 1941**
Manuel Velasco-Jiménez, Rafael Castro-López, Elisenda Roca, Francisco Vidal Fernández
Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, Spain

C1L-B.4 **Extraction and Application of Wiring Symmetry Rules to Route Analog Multiport Terminals 1945**
Ricardo Martins, Nuno Lourenço, António Canelas, Nuno Horta
Instituto de Telecomunicações/Instituto Superior Técnico, Portugal

C1L-B.5 **A Symbolic SC Integrator Model for Fast Time-Response Simulation 1949**
Ailin Zhang, Guoyong Shi
Shanghai Jiao Tong University, China

C1L-C: 3D Integrated Circuits

Time: Wednesday, May 27 (09:30-11:00)
Room: S1: Luis F. Branco
Chair(s): Yehea Ismail, *American University in Cairo*
Ricardo Reis, *Universidade Federal do Rio Grande do Sul*

C1L-C.1 **Design of Adiabatic TSV, SWCNT TSV, and Air-Gap Coaxial TSV 1953**
Khaled Salah[2], Yehea Ismail[1]
[1]American University in Cairo & Zewail City of Science and Technology, Egypt; [2]Mentor Graphics Corporation, Egypt

C1L-C.2 **Performance Analysis of Through Silicon via (TSV) and Through Glass via (TGV) for Different Materials 1957**
Abdul Yousuf, Nahid Hossain, Masud Chowdhury
University of Missouri-Kansas City, United States

C1L-C.3 **Performance Evaluation of Hierarchical NoC Topologies for Stacked 3D ICs 1961**
Debora Matos[2], Max Prass[2], Marcio Kreutz[1], Luigi Carro[3], Altamiro Susin[3]
[1]Federal University of Rio Grande do Norte, Brazil; [2]Universidade Estadual do Rio Grande do Sul, Brazil; [3]Universidade Federal do Rio Grande do Sul, Brazil

C1L-C.4 **Low Swing TSV Signaling Using Novel Level Shifters with Single Supply Voltage..... 1965**
Shiwei Fang, Emre Salman
Stony Brook University, United States

C1L-C.5 **Physical Characterization of Steady-State Temperature Profiles in Three-Dimensional Integrated Circuits 1969**
Sumeet Kumar, Amir Zjajo, Rene van Leuken
Technische Universiteit Delft, Netherlands

C1L-D: SPECIAL SESSION: Parallel Processor Array Architectures and their Applications for Complex Problems

Time: Wednesday, May 27 (09:30-11:00)
Room: S2: E. Andrade
Chair(s): Peter Szolgay, *Pazmany Peter Catholic University*
Akos Zarandy, *Computer and Automation Research Institute of the Hungarian Academy of Sciencies*

C1L-D.1 **Cellular Sensor-Processor Array Based Visual Collision Warning Sensor 1973**
Akos Zarandy[2], Mate Nemeth[2], Borbala Pencz[1], Zoltán Nagy[1], Tamas Zsedrovits[2]
[1]Computer and Automation Research Institute of the Hungarian Academy of Sciences, Hungary; [2]Pázmány Péter Catholic University, Hungary

C1L-D.2 **Analysis of Parallel Processor Architectures for the Solution of the Black-Scholes PDE 1977**
Endre László[3], Zoltán Nagy[1], Michael Giles[4], István Reguly[4], Jeremy Appleyard[2], Péter Szolgay[3]
[1]Computer and Automation Research Institute of the Hungarian Academy of Sciences, Hungary; [2]NVIDIA Corporation, United Kingdom; [3]Pázmány Péter Catholic University, Hungary; [4]University of Oxford, United Kingdom

C1L-D.3 **Emulating Massively Parallel Non-Boolean Operators on FPGA 1981**
Andras Kiss[2], Zoltán Nagy[1], Péter Szolgay[2], György Csaba[3], Xiaobo Sharon Hu[3], Wolfgang Porod[3]
[1]Computer and Automation Research Institute of the Hungarian Academy of Sciences, Hungary; [2]Pázmány Péter Catholic University, Hungary; [3]University of Notre Dame, United States

C1L-D.4 **Online Seam Tracking for Laser Welding with a Vision Chip and FPGA Enabled Camera System 1985**
Tero Säntti, Jonne Poikonen, Olli Lahdenoja, Mika Laiho, Ari Paasio
University of Turku, Finland

C1L-E: Circuits for Error Correcting Codes

Time: Wednesday, May 27 (09:30-11:00)
Room: S5: F. Pessoa
Chair(s): Wei Xing Zheng, *University of Western Sydney*
Chuan Zhang, *Southeast University*

C1L-E.1 **A 630 Mbps Non-Binary LDPC Decoder for FPGA 1989**
Jesús Omar Lacruz[1], Francisco García-Herrero[2], Maria Jose Canet[2], Javier Valls[2], Asunción Pérez-Pascual[2]
[1]Universidad de Los Andes, Venezuela; [2]Universitat Politècnica de València, Spain

C1L-E.2 **On Metric Sorting for Successive Cancellation List Decoding of Polar Codes.....1993**
Alexios Balatsoukas-Stimming, Mani Bastani Parizi, Andreas Burg
École Polytechnique Fédérale de Lausanne, Switzerland

C1L-E.3 **A Hybrid Multimode BCH Encoder Architecture for Area Efficient Re-Encoding Approach.....1997**
Hoyoung Tang, Gihoon Jung, Jongsun Park
Korea University, Korea, South

C1L-E.4 **TTCN: a New Approach for Low-Power Split-Row LDPC Decoders.....2001**
Mohammad Shahrad[1], Mahdi Shabany[2]
[1]Princeton University, United States; [2]Sharif University of Technology, Iran

C1L-E.5 **The Joint Detect and Decoding Approach for MIMO Systems with Turbo Codes.....2005**
Po-Hsiang Hsiung, Chung-An Shen, Huan-Chun Wang
National Taiwan University of Science and Technology, Taiwan

C1L-F: SPECIAL SESSION: Design of Secure and Side Channel Resistant Cryptographic Processors

Time: Wednesday, May 27 (09:30-11:00)
Room: S6: A. Negreiros
Chair(s): Hector Pettenghi Roldan, *Universidade Federal de Santa Catarina*
Nele Mentens, *Katholieke Universiteit Leuven*

C1L-F.1 **Challenges in Designing Trustworthy Cryptographic Co-Processors.....2009**
Ricardo Chaves[1], Giorgio Di Natale[3], Lejla Batina[4], Shivam Bhasin[7], Baris Ege[4], Apostolos Fournaris[6], Nele Mentens[2], Stjepan Picek[5], Francesco Regazzoni[8], Vladimir Rozic[2], Nicolas Sklavos[6], Bohan Yang[2]
[1]INESC-ID / Universidade de Lisboa, Portugal; [2]Katholieke Universiteit Leuven, Belgium; [3]Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, France; [4]Radboud University, Netherlands; [5]Radboud University Nijmegen, Net

C1L-F.2 **Improving DPA Resistance of S-Boxes: How Far Can We Go?.....2013**
Baris Ege[1], Kostas Papagiannopoulos[1], Lejla Batina[1], Stjepan Picek[2]
[1]Radboud University, Netherlands; [2]University of Zagreb, Croatia

C1L-F.3 **On-the-Fly Tests for Non-Ideal True Random Number Generators.....2017**
Bohan Yang, Vladimir Rožic, Nele Mentens, Ingrid Verbauwhede
Katholieke Universiteit Leuven, Belgium

C1L-F.4 **A Survey on Hardware Trojan Detection Techniques 2021**
Shivam Bhasin[1], Francesco Regazzoni[2]
[1]Télécom ParisTech, France; [2]University of Lugano / Advanced Learning and Research Institute, Switzerland

C1L-F.5 **Designing Efficient Elliptic Curve Diffie-Hellman Accelerators for Embedded Systems.....2025**
Apostolos Fournaris[3], Ioannis Zafeirakis[3], Christos Koulamas[1], Nicolas Sklavos[2], Odysseas Koufopavlou[3]
[1]Industrial Systems Institute, Greece; [2]Technological Educational Institute of Western Greece, Greece; [3]University of Patras, Greece

C1L-G: Sigma-Delta Modulators I

Time: Wednesday, May 27 (09:30-11:00)
Room: S7: S. M. Breyner
Chair(s): Luis Hernandez, *Charles III University of Madrid*
José M de la Rosa, *IMSE-CNM (CSIC/University of Seville), Spain*

C1L-G.1 **A Single Op-Amp 0+2 Sigma-Delta Modulator 2029**
Yao Liu, Edoardo Bonizzoni, Franco Maloberti
Università degli Studi di Pavia, Italy

C1L-G.2 **Highly Linear Continuous-Time MASH Delta-Sigma ADC with Dual VCO-Based Quantizers 2033**
Yang Xu, Spencer Leuenberger, Un-Ku Moon
Oregon State University, United States

C1L-G.3 **A Current-Mode VCO-Based Amplifier-Less 2nd-Order Delta-Sigma Modulator with Over 85dB SNDR 2037**
Somayeh Abdollahvand, Nuno Paulino, Luis Gomes, João Goes
Universidade Nova de Lisboa, Portugal

C1L-G.4 **A 94-dB SFDR Multi-Bit Audio-Band Delta-Sigma Converter with DAC Nonlinearity Suppression 2041**
Swetha George[2], Yu Song[1], Zeljko Ignjatovic[2]
[1]Qualcomm Inc, United States; [2]University of Rochester, United States

C1L-G.5 **A Noise-Coupled Time-Interleaved Delta-Sigma Modulator with Shifted Loop Delays 2045**
Xin Meng, Yi Zhang, Tao He, Pedram Payandehnia, Gabor C. Temes
Oregon State University, United States

C1L-H: Intelligent Visual Signal Processing and Systems Design

Time: Wednesday, May 27 (09:30-11:00)
Room: S8: G. Quartim
Chair(s): Fei Qiao, *Tsinghua University*
Wen-Hsiao Peng, *National Chiao Tung University*

C1L-H.1 **Design for an Intelligent Surveillance System Based on System-on-a-Programmable-Chip Platform 2049**
Tsung-Han Tsai, Chih-Hao Chang
National Central University, Taiwan

C1L-H.2 **Hardware Design and FPGA Implementation for Road Plane Extraction Based on V-Disparity Approach 2053**
Imad Benacer[1], Aicha Hamissi[1], Abdelhakim Khouas[2]
[1]Ecole Militaire Polytechnique, Algeria; [2]University of Boumerdès, Algeria

C1L-H.3 **Physical Computing Circuit with No Clock to Establish Gaussian Pyramid of SIFT Algorithm 2057**
Yi Li, Fei Qiao, Qi Wei, Huazhong Yang
Tsinghua University, China

C1L-H.4 **Toward Joint Approximate Inference of Visual Quantities on Cellular Processor Arrays 2061**
Julien N.P. Martel[1], Miguel Chau[1], Piotr Dudek[2], Matthew Cook[1]
[1]Universität Zürich and ETH Zürich, Switzerland; [2]University of Manchester, United Kingdom

C1L-H.5 **Two-Dimensional Discriminant Multi-Manifolds Locality Preserving Projection for Facial Expression Recognition 2065**
Ning Zheng[3], Xin Guo[3], Lin Qi[2], Ling Guan[1]
[1]Ryerson University, Canada; [2]Zhengzhou Universitt, China; [3]Zhengzhou University, China

C1L-J: Amplifiers I

Time: Wednesday, May 27 (09:30-11:00)
Room: S9: M.H.V. Silva
Chair(s): Thierry Taris, *IMS*

C1L-J.1 **A Voltage-Combiners-Biased Amplifier with Enhanced Gain and Speed Using Current Starving 2069**
Ricardo Póvoa[1], Nuno Lourenço[1], Nuno Horta[1], João Goes[2]
[1]Instituto de Telecomunicações/Instituto Superior Técnico, Portugal; [2]Universidade Nova de Lisboa, Portugal

C1L-J.2 **Gain and Slew Rate Enhancement for Amplifiers Through Current Starving and Feeding 2073**
Shi Bu[1], Hing Wa Tse[1], Ka Nang Leung[1], Jianping Guo[2], Marco Ho[1]
[1]Chinese University of Hong Kong, Hong Kong; [2]Sun Yat-sen University, China

C1L-J.3 **Cascode and Transconductance with Capacitances Feedback Compensation for Multistage Amplifiers Driving No Load and 1nF Capacitive Load 2077**
Xu Zhang[1], Chongli Cai[1], Degang Chen[1], Gregory Blum[2]
[1]Iowa State University, United States; [2]Skyworks Solutions, Inc., United States

C1L-J.4 **Class-AB Single-Stage OpAmp for Low-Power Switched-Capacitor Circuits 2081**
Stepan Sutula, Michele Dei, Lluís Terés, Francisco Serra-Graells
IMB-CNM-CSIC, Spain

C1L-J.5 **Gain Enhanced High Frequency OTA with on-Chip Tuned Negative Conductance Load 2085**
Imon Mondal, Nagendra Krishnapura
Indian Institute of Technology Madras, India

C1L-K: Modeling, Dynamics, and Control of Power Converters I

Time: Wednesday, May 27 (09:30-11:00)
Room: S10: A.S. Cardoso
Chair(s): Adrian Ioinovici, *Holon Institute of Technology*
Abdelali El Aroudi, *Universitat Rovira i Virgili*

C1L-K.1 **Subharmonic Instability Boundary in DC-AC H-Bridge Inverters with Double Edge PWM 2089**
Abdelali El Aroudi[3], Wei-Guo Lu[1], Mohammed S. AL-Numay[2], Herbert Ho-Ching Iu[4]
[1]Chongqing University, China; [2]King Saud University, Saudi Arabia; [3]Universitat Rovira i Virgili, Spain; [4]University of Western Australia, Australia

C1L-K.2 **Dynamic Performance Analysis of 3-Level Integrated Buck Converters 2093**
Xun Liu, Cheng Huang, Philip Mok
Hong Kong University of Science and Technology, Hong Kong

C1L-K.3 **A High Step-Up DC-DC Converter Using Transformer with Intrinsic Voltage-Doubler 2097**
Koichi Furukawa, Taro Takiguchi, Ryuga Hosoki, Hirotaka Koizumi
Tokyo University of Science, Japan

C1L-K.4 **Simple Switched-Capacitor-Boost Converter with Large DC Gain and Low Voltage Stress on Switches 2101**
Yafei Hu[1], Adrian Ioinovici[2]
[1]Sun Yat-sen University, China; [2]Sun Yat-sen University / Holon Institute of Technology, Israel

C1L-K.5 **New Phase Shift Modulator for Resonant Converters 2105**
Carlos Ferreira[2], Beatriz Borges[1]
[1]Instituto de Telecomunicações/Instituto Superior Técnico, Portugal; [2]Instituto Politécnico de Tomar, Portugal

C1L-L: Sensors

Time: Wednesday, May 27 (09:30-11:00)
Room: S11: C. Telmo
Chair(s): Tim Constandinou, *Imperial college*
Piotr Dudek, *University of Manchester*

C1L-L.1 **A 486k S/s CMOS Time-Domain Smart Temperature Sensor with -0.85°C/0.78°C Voltage-Calibrated Error 2109**
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National Taiwan University of Science and Technology, Taiwan

C1L-L.2 **A Low-Power RFID Enabled Temperature Sensor for Cold Chain Management 2113**
Francisco Gomes[1], Luciano de Paula[1], Joao Santos[2], Laurent Courcelle[1], Daniel Piovani[1], Filipe Viera[1]
[1]CEITEC S.A Semiconductors, Brazil; [2]Pontifícia Universidade Católica do Rio Grande do Sul, Brazil

C1L-L.3 **Ground Penetrating Radar Utilizing Compressive Sampling and OFDM Techniques 2117**
Mohamed Metwally, Nicholai L'Esperance, Tian Xia
University of Vermont, United States

C1L-L.4 **Sensing by Growing Antennas: a Novel Approach for Designing Passive RFID Based Biosensors 2121**
Mingquan Yuan, Premjeet Chahal, Evangelyn Alocilja, Shantanu Chakrabartty
Michigan State University, United States

C1L-L.5 **A Programmable Vision Chip with Pixel-Neighborhood Level Parallel Processing 2125**
Joseph A. Schmitz[2], Mahir Kabeer Gharzai[2], Sina Balkir[2], Michael Hoffman[2], Daniel White[3], Nathan Schemm[1]
[1]Texas Instruments Inc., United States; [2]University of Nebraska-Lincoln, United States; [3]Valparaiso University, United States

C1L-M: Innovations in Logic & Physical Synthesis

Time: Wednesday, May 27 (09:30-11:00)
Room: S12: D. Costa
Chair(s): Philippe Coussy, *Universite de Bretagne Sud*

C1L-M.1 **A Floorplan-Driven High-Level Synthesis Algorithm with Multiple-Operation Chainings Based on Path Enumeration 2129**
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Waseda University, Japan

C1L-M.2 **3-D Floorplanning Algorithm to Minimize Thermal Interactions 2133**
Boris Vaisband, Eby Friedman
University of Rochester, United States

C1L-M.3 **Lithography-Friendly Analog Layout Migration 2137**
Xuan Dong, Lihong Zhang
Memorial University of Newfoundland, Canada

C1L-M.4 **Effective Two-Dimensional Pattern Generation for Self-Aligned Double Patterning 2141**
Takeshi Ihara[1], Atsushi Takahashi[1], Chikaaki Kodama[2]
[1]Tokyo Institute of Technology, Japan; [2]Toshiba Corporation, Japan

C1L-M.5 **A Compact Representation of a Quantum Controlled Ternary Barrel Shifter 2145**
Nusrat Jahan Lisa, Hafiz Md Hasan Babu
University of Dhaka, Bangladesh

C2P-N: Signal and Image Processing

Time: Wednesday, May 27 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Wei Xing Zheng, *University of Western Sydney*
David Tay, *La Trobe University*

C2P-N.1 **Image Denoising Utilizing the Scale-Dependency in the Contourlet Domain.....2149**
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Concordia University, Canada

C2P-N.2 **Real-Valued ESPRIT for Two-Dimensional DOA Estimation of Noncircular Signals for Acoustic Vector Sensor Array.....2153**
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Concordia University, Canada

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[1]Fuzhou University, China; [2]University of Western Sydney, Australia

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Hong Kong Polytechnic University, Hong Kong

C2P-N.5 **Gradient-Weighted Structural Similarity for Image Quality Assessments.....2165**
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[1]Jiangxi University of Finance and Economics, China; [2]Nanyang Technological University, Singapore

C2P-P: DSP Application

Time: Wednesday, May 27 (11:00-12:50)
Room: 2nd Floor Foyer
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Xiao-Ping Zhang, *Ryerson University*

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Eldorado Research Institute, Brazil

C2P-P.3 **Encoding Compressive Sensing Measurements with Golomb-Rice Codes 2177**
Walter Leon-Salas
Purdue University, United States

C2P-P.4 **Hardware Implementation of All Digital Calibration for Undersampling TIADCs 2181**
Han Le Duc[2], Duc Minh Nguyen[2], Chadi Jabbour[2], Tarik Graba[2], Patricia Desgreys[2], Olivier Jamin[1], Van Tam Nguyen[3]
[1]NXP Semiconductors, France; [2]Télécom ParisTech, France; [3]Télécom ParisTech and University of California at Berkeley, France

C2P-P.5 **Efficient Radix Conversions for Classes of Radices.....2185**
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University of Windsor, Canada

C2P-Q: Digital Filters

Time: Wednesday, May 27 (11:00-12:50)
Room: 2nd Floor Foyer
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Oscar Gustafsson, *Linköping University, Sweden*

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[1]Christopher Newport University, United States; [2]Florida Atlantic University, United States; [3]Johnson C. Smith University, United States

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Takao Hinamoto[1], Akimitsu Doi[1], Wu-Sheng Lu[2]
[1]Hiroshima University, Japan; [2]University of Victoria, Canada

C2P-Q.3 **A General Expression of the Low-Pass Maximally Flat FIR Digital Differentiators 2197**
Takashi Yoshida, Yosuke Sugiura, Naoyuki Aikawa
Tokyo University of Science, Japan

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Dinesh Kumar Chobey, Yong Ching Lim
Nanyang Technological University, Singapore

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C2P-R: Communication Circuits

Time: Wednesday, May 27 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Thierry Taris, *IMS*

C2P-R.1 **A 1Gbps - 10 Gbps Multi-Standard Auto-Calibrated All Digital Phase Interpolator in 14nm CMOS 2209**
Anupjyoti Deka, Venkatesh Prasanna
Intel India Tech Pvt Ltd, India

C2P-R.2 **Inductorless Linearization of Low-Power Active Mixers 2213**
Li Xu, Kainan Wang, Chun-Hsiang Chang, Marvin Onabajo
Northeastern University, United States

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Ying Guo, Ling Shen, Fan Yang, Yongan Zheng, Long Chen, Xing Zhang, Huailin Liao
Peking University, China

C2P-S: Analog Circuits I

Time: Wednesday, May 27 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Thierry Taris, *IMS*

C2P-S.1 **An Integrated Circuit Solution of Thermal Noise Thermometer with Cascaded Pre-Amplifier and 6-Bit Resolution Analog-to-Digital Converter.....2221**
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C2P-S.2 **A Wide-Range Dual-Modulus Prescaler Using a Novel SCL Biasing Technique.....2225**
Cristina Azcona, Belén Calvo, Nicolás Medrano, Santiago Celma, Cecilia Gimeno
Universidad de Zaragoza, Spain

C2P-S.3 **A Quad-Mode DCO for Multi-Standard Communication Application 2229**
Bo Jiang, Tian Xia
University of Vermont, United States

C2P-S.4 **A MEMS Microphone Interface Based on a CMOS LC Oscillator and a Digital Sigma-Delta Modulator.....2233**
Fernando Cardes[2], Ruzica Jevtic[2], Luis Hernandez[2], Andreas Wiesbauer[1], Dietmar Straeussnigg[1], Richard Gaggl[1]
[1]Infineon Technologies AG, Austria; [2]Universidad Carlos III de Madrid, Spain

C2P-S.5 **An FSK Modulator at 23.2MHz with +/-0.9% Accuracy for the USB Power Delivery Standard.....2237**
Antonio D'Amico[3], Angelo Nagari[1], Piero Malcovati[2], Andrea Baschirotto[3]
[1]STMicroelectronics, France; [2]Università degli Studi di Pavia, Italy; [3]Università degli Studi Milano-Bicocca, Italy

C2P-T: Analog Circuits II

Time: Wednesday, May 27 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Vadim Ivanov, *Texas Instruments*

C2P-T.1 **An Energy-Efficient Level Shifter for Low-Power Applications 2241**
Seyed Rasool Hosseini[1], Mehdi Saberi[1], Reza Lotfi[2]
[1]Ferdowsi university of mashhad, Iran; [2]Technische Universiteit Delft, Netherlands

C2P-T.2 **A Subthreshold, Low-Power, RHBD Reference Circuit, for Earth Observation and Communication Satellites 2245**
Charalambos Andreou[6], Alessandro Paccagnella[5], Diego González-Castaño[3], Faustino Gómez[3], Valentino Liberali[4], Alexander Prokofiev[8], Cristiano Calligaro[1], Arto Javanainen[7], Ari Virtanen[7], Daniel Nahmad[2], Julius Georgiou[6]
[1]RedCat Devices, Italy; [2]Tower Semiconductor, Israel; [3]Universidade de Santiago de Compostela, Spain; [4]Universita degli Studi di Milano, Italy; [5]Università degli Studi di Padova, Italy; [6]University of Cyprus, Cyprus; [7]University of Jyvaskyla

C2P-T.3 **Time-Interleaved Integrating Quantizer Incorporating Channel Coupling for Speed and Linearity Enhancement 2249**
Yue Hu, Spencer Leuenberger, Yang Xu, Un-Ku Moon
Oregon State University, United States

C2P-T.4 **High-Speed and High-Linearity Ring Oscillator Based Pulse Width Modulator 2253**
Taewook Kim, Jun Liu, Nima Maghari
University of Florida, United States

C2P-T.5 **Charge-Compensation-Based Reference Technique for Switched-Capacitor ADCs 2257**
Ya Wang, Fule Li, Chunying Xue, Zhihua Wang
Tsinghua University, China

C2P-U: Analog Circuits Testing and Verification II

Time: Wednesday, May 27 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Joseph Chang, *Nanyang Technological University*

C2P-U.1 **DLL Based Test Solution for Interposers in 2.5-D ICs 2261**
Vladimir Mashkovtsev, Ali Attaran, Rashid Rashidzadeh
University of Windsor, Canada

C2P-U.2 **Accurate Spectral Testing of Analog-to-Digital Converters with Frequency Drift Using Phase Correction and Averaging 2265**
Li Xu, Degang Chen
Iowa State University, United States

C2P-U.3 **Thermal-Aware Floorplanning and Layout Generation of MOSFET Power Stages 2269**
David Guilherme[1], João Pereira[4], Nuno Horta[2], Jorge Guilherme[3]
[1]Instituto de Telecomunicações, Portugal; [2]Instituto de Telecomunicações/Instituto Superior Técnico, Portugal; [3]Instituto Politécnico de Tomar, Portugal; [4]Instituto Superior Tecnico, Portugal

C2P-U.4 **Voltage-Based Wideband Measurement of Transmission Characteristics Using an Integrated Receiver IC 2273**
Mehran Bakhshiani, Pedram Mohseni
Case Western Reserve University, United States

C2P-U.5 **A Low Cost Jitter Estimation and ADC Spectral Testing Method 2277**
Li Xu, Degang Chen
Iowa State University, United States

C2P-V: Calibration Techniques

Time: Wednesday, May 27 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Shu Wei, *Nanyang Technological University*

C2P-V.1 **1.1-V 200 MS/s 12-Bit Digitally Calibrated Pipeline ADC in 40 nm CMOS 2281**
Hussein Adel[2], Marc Sabut[1], Marie-Minerve Louerat[3]
[1]STMicroelectronics, France; [2]Université Pierre et Marie Curie, France; [3]Université Pierre et Marie Curie / LIP6, France

C2P-V.2 **A High-Speed High-Accuracy Voltage-to-Time-Difference Converter for Time Domain Analog-to-Digital Converters 2285**
Yu-Chuan Lin, Hen-Wai Tsao
National Taiwan University, Taiwan

C2P-V.3 **A Digital to Time Converter with Fully Digital Calibration Scheme for Ultra-Low Power ADPLL in 40 nm CMOS 2289**
Bindi Wang[1], Yao-Hong Liu[2], Pieter Harpe[1], Johan van den Heuvel[2], Bo Liu[1], Hao Gao[1], Robert Bogdan Staszewski[3]
[1]Eindhoven University of Technology, Netherlands; [2]IMEC - Holst Centre, Netherlands; [3]Technische Universiteit Delft, Netherlands

C2P-V.4 **Bitstream Switching Rate Based Calibration of Delta-Sigma Modulators 2293**
Jingjing Hu[1], Hans Hegt[1], Arthur van Roermund[1], Sotir Ouzounov[2]
[1]Eindhoven University of Technology, Netherlands; [2]Philips Research, Netherlands

C2P-V.5 **A Digital Time Skew Calibration Technique for Time-Interleaved ADCs 2297**
Lei Qiu, Kai Tang, Yuanjin Zheng, Liter Siek
Nanyang Technological University, Singapore

C2P-W: Nano-Electronics IV

Time: Wednesday, May 27 (11:00-12:50)
Room: 2nd Floor Foyer
Chair(s): Chen-Hao Chang, *National Chung Hsing University*

C2P-W.2 **An Energy-Efficient Heterogeneous Dual-Core Processor for Internet of Things 2301**
Zhibo Wang, Yongpan Liu, Yinan Sun, Yang Li, Daming Zhang, Huazhong Yang
Tsinghua University, China

C2P-W.3 **NoC Router Using STT-MRAM Based Hybrid Buffers with Error Correction and Limited Flit Retransmission 2305**
Turbo Majumder, Manan Suri, Vinay Shekhar
Indian Institute of Technology Delhi, India

C3L-A: Emerging Device and Circuit Technologies II

Time: Wednesday, May 27 (11:20-12:50)
Room: Main Auditorium
Chair(s): Vasilis Pavlidis, *University of Manchester*
Magdy Bayoumi, *University of Louisiana at Lafayette*

C3L-A.1 **Analysis of Subthreshold Swing in Multichannel Tunneling Carbon Nanotube Field Effect Transistor (MT-CNTFET).....2309**
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University of Missouri-Kansas City, United States

C3L-A.2 **Modeling the Impact of Dynamic Voltage Scaling on 1T-1J STT-RAM Write Energy and Performance 2313**
Kien Trinh Quang[2], Sergio Ruocco[1], Massimo Alioto[2]
[1]Agency for Science, Technology and Research, Singapore; [2]National University of Singapore, Singapore

C3L-A.3 **A Design Methodology for Minimizing Power Loss in Integrated DC-DC Converter with Spiral Inductors 2317**
Sami Smaili, Shuang Li, Yehia Massoud
Worcester Polytechnic Institute, United States

C3L-A.4 **A Footprint-Constrained Efficiency Roadmap for on-Chip Switched-Capacitor DC-DC Converters.....2321**
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University of California, San Diego, United States

C3L-A.5 **Evaluation of TFET and FinFET Devices and 32-Bit CLA Circuits Considering Work Function Variation and Line-Edge Roughness 2325**
Chien-Ju Chen, Yin-Nien Chen, Ming-Long Fan, Vita Pi-Ho Hu, Pin Su, Ching-Te Chuang
National Chiao Tung University, Taiwan

C3L-B: SPECIAL SESSION: Fractors and Fractional Order Systems

Time: Wednesday, May 27 (11:20-12:50)
Room: Small Auditorium
Chair(s): Munmun Khanra, *National Institute of Technology, Silchar*
Karabi Biswas, *IIT Kharagpur, India*

C3L-B.1 **Realization of a Carbon Nanotube Based Electrochemical Fractor 2329**
Avishek Adhikary, Munmun Khanra, Siddhartha Sen, Karabi Biswas
Indian Institute of Technology Kharagpur, India

C3L-B.2 **Fractional Order Noise Identification with Application to Temperature Sensor Data ...2333**
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Warsaw University of Technology, Poland

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Georgia Tsirimokou[1], Costas Psychalinos[1], Ahmed Elwakil[2]
[1]University of Patras, Greece; [2]University of Sharjah, U.A.E.

C3L-B.4 **A Physical Experimental Study of the Fractional Harmonic Oscillator.....2341**
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St. Cloud State University, United States

C3L-C: Low-Power Logic & Architectures

Time: Wednesday, May 27 (11:20-12:50)
Room: S1: Luis F. Branco
Chair(s): Koushik Maharatna, *University of Southampton*
Vasily Moshnyaga, *Fukuoka University*

C3L-C.1 **Introducing Deglitched-Feedback Plus Convergent Encoding for Straight Hardware Implementation of Asynchronous Finite State Machines 2345**
Volnei Pedroni
Universidade Tecnológica Federal do Paraná, Brazil

C3L-C.2 **AES Architectures for Minimum-Energy Operation and Silicon Demonstration in 65nm with Lowest Energy Per Encryption 2349**
Wenfeng Zhao[2], Yajun Ha[1], Massimo Alioto[2]
[1]Agency for Science, Technology and Research, Singapore; [2]National University of Singapore, Singapore

C3L-C.3 **Area-Sharing Cyclic Structure MRF Cirucits Design in Ultra-Low Supply Voltage 2353**
Yan Li, Xiaoqian Li, Jianhao Hu, Sheng Yang
University of Electronic Science and Technology of China, China

C3L-C.4 **Exploiting Bit-Depth Scaling for Quality-Scalable Energy Efficient Display Processing 2357**
Qiubo Chen, Hengyu Zhao, Hongbin Sun, Nanning Zheng
Xi'an Jiaotong University, China

C3L-C.5 **Error-Energy Analysis of Hardware Logarithmic Approximation Methods for Low Power Applications 2361**
Alicia Klinefelter[2], Joseph Ryan[1], James Tschanz[1], Benton Calhoun[2]
[1]Intel Corporation, United States; [2]University of Virginia, United States

C3L-D: SPECIAL SESSION: Recent Advances in Multidimensional Systems and Signal Processing

Time: Wednesday, May 27 (11:20-12:50)
Room: S2: E. Andrade
Chair(s): Zhiping Lin, *Nanyang Technological University*
Arjuna Madanayake, *University of Akron*

C3L-D.1 **Recent Advances in Multidimensional Systems and Signal Processing: an Overview.....2365**
Arjuna Madanayake[2], Chamith Wijenayake[3], Zhiping Lin[1], Nathan Dornback[2]
[1]Nanyang Technological University, Singapore; [2]University of Akron, United States; [3]University of New South Wales, Australia

C3L-D.2 **2-D Zero-Phase IIR Notch Filters Design Based on State-Space Representation of 2-D Frequency Transformation.....2369**
Shi Yan[2], Lijun Sun[2], Li Xu[1]
[1]Akita Prefectural University, Japan; [2]Lanzhou University, China

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Alfred Fettweis[2], Sankar Basu[1]
[1]National Science Foundation, United States; [2]Ruhr-Universität Bochum, Germany

C3L-D.4 **2-D Signal Theoretic Investigation of Background Elimination in Visual Tomographic Reconstruction for Safety and Enabling Health Applications.....2377**
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Universität Wuppertal, Germany

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Chamira Edussooriya[2], Leonard Bruton[1], Panajotis Agathoklis[2]
[1]University of Calgary, Canada; [2]University of Victoria, Canada

C3L-E: Communications Circuits

Time: Wednesday, May 27 (11:20-12:50)
Room: S5: F. Pessoa
Chair(s): Jongsun Park, *Korea University*
Jaehyouk Choi, *UNIST*

C3L-E.1 **A High-Voltage DC Bias Architecture Implementation in a 17 Gbps Low-Power Common-Cathode VCSEL Driver in 80 nm CMOS 2385**
Laszlo Szilágyi, Guido Belfiore, Ronny Henker, Frank Ellinger
Technische Universität Dresden, Germany

C3L-E.2 **A 10 Gb/s Hybrid PLL-Based Forwarded Clock Receiver in 65-nm CMOS 2389**
Kwanseo Park, Woorham Bae, Haram Ju, Jinhyung Lee, Gyu-Seob Jeong, Yoonsoo Kim, Deog-Kyoon Jeong
Seoul National University, Korea, South

C3L-E.3 **A 8.1/5.4/2.7/1.62 Gb/s Receiver for DisplayPort Version 1.3 with Automatic Bit-Rate Tracking Scheme 2393**
Chien Ai, Shuo-Hong Hung, Kuan-I Wu, Chang-Yi Liu, Min-Han Hsieh, Charlie Chung-Ping Chen
National Taiwan University, Taiwan

C3L-E.4 **A 2 x 50-Gb/s Receiver with Adaptive Channel Loss Equalization and Far-End Crosstalk Cancellation 2397**
Jerry Han, Michael M. Green
University of California, Irvine, United States

C3L-E.5 **A 64dB Gain 60GHz Receiver with 7.1dB Noise Figure for 802.11ad Applications in 90nm CMOS 2401**
Jun Luo, Lei Zhang, Wei Zhu, Li Zhang, Yan Wang, Zhiping Yu
Tsinghua University, China

C3L-F: SPECIAL SESSION: Real-Time Event-Based Sensor Processing

Time: Wednesday, May 27 (11:20-12:50)
Room: S6: A. Negreiros
Chair(s): Jörg Conradt, *Technische Universitat Munchen (TUM), Germany*
Shih-Chii Liu, *ETHZ*

C3L-F.1 **ConvNets Experiments on SpiNNaker 2405**
Teresa Serrano-Gotarredona[1], Bernabé Linares-Barranco[1], Francesco Galluppi[2], Luis Plana[3], Steve Furber[3]
[1]Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, Spain; [2]Université Pierre et Marie Curie, France; [3]University of Manchester, United Kingdom

C3L-F.2 **Human Vs. Computer Slot Car Racing Using an Event and Frame-Based DAVIS Vision Sensor 2409**
Tobi Delbruck[4], Michael Pfeiffer[4], Raphael Juston[1], Garrick Orchard[2], Elias Müggler[4], Alejandro Linares-Barranco[3], Mark W. Tilden[5]
[1]Aix-Marseille University, France; [2]National University of Singapore, Singapore; [3]Universidad de Sevilla, Spain; [4]Universität Zürich and ETH Zürich, Switzerland; [5]WowWee Group Limited, Hong Kong

C3L-F.3 **Real-Time Event-Driven Spiking Neural Network Object Recognition on the SpiNNaker Platform 2413**
Garrick Orchard[1], Xavier Lagorce[2], Christoph Posch[2], Steve Furber[3], Ryad Benosman[2], Francesco Galluppi[2]
[1]National University of Singapore, Singapore; [2]Université Pierre et Marie Curie, France; [3]University of Manchester, United Kingdom

C3L-F.4 **A USB3.0 FPGA Event-Based Filtering and Tracking Framework for Dynamic Vision Sensors 2417**
Alejandro Linares-Barranco[2], Francisco Gómez- Rodríguez[2], Vicente Villanueva[1], Luca Longinotti[1], Tobias Delbrück[3]
[1]Inilabs GmbH, Switzerland; [2]Universidad de Sevilla, Spain; [3]Universität Zürich and ETH Zürich, Switzerland

C3L-F.5 **Scene Stitching with Event-Driven Sensors on a Robot Head Platform 2421**
Philipp Klein[2], Joerg Conradt[1], Shih-Chii Liu[2]
[1]Technische Universität München, Germany; [2]Universität Zürich and ETH Zürich, Switzerland

C3L-G: Successive Approximation ADCs

Time: Wednesday, May 27 (11:20-12:50)
Room: S7: S. M. Breyner
Chair(s): George Yuan, *Hong Kong University of Science and Technology*

C3L-G.1 **A 10-Bit 50-MS/s SAR ADC for Dual-Voltage Domain Portable Systems 2425**
Wei-Hao Tsai[2], Che-Hsun Kuo[2], Soon-Jyh Chang[2], Li-Tse Lo[1], Ying-Cheng Wu[1], Chun-Jen Chen[1]
[1]Industrial Technology Research Institute, Taiwan; [2]National Cheng Kung University, Taiwan

C3L-G.2 **A 1.2V 1MS/s 7.65fJ/Conversion-Step 12-Bit Hybrid SAR ADC with Time-to-Digital Converter 2429**
Sung-En Hsieh, Cheng-Kang Ho, Chih-Cheng Hsieh
National Tsing Hua University, Taiwan

C3L-G.3 **A Split Transconductor High-Speed SAR ADC 2433**
Dante Gabriel Muratore, Edoardo Bonizzoni, Franco Maloberti
Università degli Studi di Pavia, Italy

C3L-G.4 **A 4.5fJ/Conversion-Step 9-Bit 35MS/s Configurable-Gain SAR ADC in a Compact Area 2437**
Ye Xu[2], Pieter Harpe[1], Trond Ytterdal[2]
[1]Eindhoven University of Technology, Netherlands; [2]Norwegian University of Science and Technology, Norway

C3L-G.5 **Reference-Less SAR ADC for on-Chip Thermal Monitoring in CMOS 2441**
Sami Rehman, Ayman Shabra
Masdar Institute of Science and Technology, U.A.E.

C3L-H: SPECIAL SESSION: Cross -Layer Technology and Design Solutions for Resilience

Time: Wednesday, May 27 (11:20-12:50)
Room: S8: G. Quartim
Chair(s): Runsheng Wang, *Peking University, China*

C3L-H.1 **Characterization and Modeling of Reliability Issues in Nanoscale Devices 2445**
Gerhard Rzepa[2], Wolfgang Goes[2], Ben Kaczer[1], Tibor Grasser[2]
[1]IMEC - Holst Centre, Belgium; [2]Technische Universität Wien, Austria

C3L-H.2 **Unified Approach for Simulation of Statistical Reliability in Nanoscale CMOS Transistors from Devices to Circuits 2449**
Asen Asenov[2], J. Ding[3], D. Reid[2], P. Asenov[1], S. Amoroso[3], F. Adamu-Lema[3], L. Gerrer[3]
[1]ARM, Ltd., United Kingdom; [2]Gold Standard Simulations, United Kingdom; [3]University of Glasgow, United Kingdom

C3L-H.3 **Impact of Temporal Transistor Variations on Circuit Reliability 2453**
Runsheng Wang[2], Yu Cao[1]
[1]Arizona State University, United States; [2]Peking University, China

C3L-H.4 **Cross-Layer Resilient System Design Flow 2457**
Fabian Oboril, Mojtaba Ebrahimi, Saman Kiamehr, Mehdi Tahoori
Karlsruher Institut für Technologie, Germany

C3L-J: Amplifiers II

Time: Wednesday, May 27 (11:20-12:50)
Room: S9: M.H.V. Silva
Chair(s): Luis Hernandez, *Charles III University of Madrid*

C3L-J.1 **Constant Gm Rail-to-Rail CMOS OpAmp with Only One Differential Pair and Switched Level Shifters.....2461**
Maria de Rodanas Valero[3], Alejandro Román-Loera[1], Jaime Ramírez-Angulo[1], Antonio J. López-Martín[4], Ramon G. Carvajal[2]
[1]New Mexico State University, United States; [2]Universidad de Sevilla, Spain; [3]Universidad de Zaragoza, Spain; [4]Universidad Pública de Navarra, Spain

C3L-J.2 **Design Considerations of STCB OTA in CMOS 65nm with Large Capacitive Loads 2465**
Kai Ho Mak[1], Marco Ho[1], Ka Nang Leung[1], Wang Ling Goh[2]
[1]Chinese University of Hong Kong, Hong Kong; [2]Nanyang Technological University, Singapore

C3L-J.3 **Low-Voltage Amplifier with Improved Linearity Using Triode Region MOSFET 2469**
Hiroki Sato, Shigetaka Takagi
Tokyo Institute of Technology, Japan

C3L-J.4 **An Improved Recycling Folded Cascode Amplifier with Gain Boosting and Phase Margin Enhancement.....2473**
Moaaz Ahmed[2], Ikramullah Shah[2], Fang Tang[1], Amine Bermak[2]
[1]Chongqing University, China; [2]Hong Kong University of Science and Technology, Hong Kong

C3L-J.5 **A Low Noise Amplifier Chain for Digital Satellite Radio Applications 2477**
Juergen Roeber, Andreas Baenisch, Georg Fischer, Robert Weigel
Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany

C3L-K: Modeling, Dynamics and Control of Power Converters II

Time: Wednesday, May 27 (11:20-12:50)
Room: S10: A.S. Cardoso
Chair(s): Herbert Iu, *The University of Western Australia*
Le-Ren Chang-Chien, *National Cheng Kung University*

C3L-K.1 **Stabilization of Fast-Scale Instabilities in PCM Boost PFC Converter with Dynamic Slope Compensation 2481**
Yidi Yang[1], Wei-Guo Lu[1], Herbert Ho-Ching Iu[2], Tyrone Fernando[2]
[1]Chongqing University, China; [2]University of Western Australia, Australia

C3L-K.2 **A New Semi-Analytic Approach for Class-E Resonant DC-DC Converter Design 2485**
Nicola Bertoni[2], Giovanni Frattini[1], Roberto Massolini[1], Fabio Pareschi[2], Riccardo Rovatti[3], Gianluca Setti[2]
[1]Texas Instruments Inc., Italy; [2]Università degli Studi di Ferrara, Italy; [3]Università di Bologna, Italy

C3L-K.3 **Bifurcation Behavior in a Two-Loop DC-DC Quadratic Boost Converter 2489**
Abdelali El Aroudi[4], Germain García[2], Danièle Fournier[2], Mohammed S. AL-Numay[1], Khalifa Al Hosani[3], Luis Martinez-Salamero[4]
[1]King Saud University, Saudi Arabia; [2]LAAS-CNRS, France; [3]Petroleum Institute, U.A.E.; [4]Universitat Rovira i Virgili, Spain

C3L-K.4 **Design of a Non-Isolated Single-Switch Three-Port DC-DC Converter for Standalone PV-Battery Power System 2493**
Junkai Zhao[2], Herbert Ho-Ching Iu[2], Tyrone Fernando[2], Le An[1], Dylan Dah-Chuan Lu[1]
[1]University of Sydney, Australia; [2]University of Western Australia, Australia

C3L-K.5 **Digitally Controlled Low Cross-Regulation Single-Inductor Dual-Output (SIDO) Buck Converter 2497**
Bu-Wei Chen, Le-Ren Chang-Chien
National Cheng-Kung University, Taiwan

C3L-L: Neural Networks Circuits and Systems

Time: Wednesday, May 27 (11:20-12:50)
Room: S11: C. Telmo
Chair(s): Maysam Ghovanloo, *Georgia Institute of Technology*
Shantanu Chakrabartty, *Michigan State University*

C3L-L.1 **Algorithm and Implementation of an Associative Memory for Oriented Edge Detection Using Improved Clustered Neural Networks 2501**
Robin Danilo[3], Hooman Jarollahi[1], Vincent Gripon[2], Philippe Coussy[3], Laura Conde-Canencia[3], Warren Gross[1]
[1]McGill University, Canada; [2]Télécom Bretagne, France; [3]Université Bretagne Sud, France

C3L-L.2 **Energy-Efficient and High Throughput Sparse Distributed Memory Architecture.....2505**
Mingu Kang, Eric Kim, Min-Sun Keel, Naresh R. Shanbhag
University of Illinois at Urbana Champaign, United States

C3L-L.3 **Neural Approximating Architecture Targeting Multiple Application Domains 2509**
Fengbin Tu, Shouyi Yin, Peng Ouyang, Leibo Liu, Shaojun Wei
Tsinghua University, China

C3L-L.4 **A Continuous-Time Varactor-Based Temperature Compensation Circuit for Floating-Gate Multipliers and Inner-Product Circuits 2513**
Liang Zhou, Shantanu Chakrabartty
Michigan State University, United States

C3L-L.5 **Winner-Take-All Neural Network with Digital Frequency-Locked Loop.....2517**
Hiroomi Hikawa
Kansai University, Japan

C3L-M: Algorithms and Architectures for 3D Media Processing

Time: Wednesday, May 27 (11:20-12:50)
Room: S12: D. Costa
Chair(s): Shao-Yi Chien, *National Taiwan University*
Mladen Berekovic, *Technische Universität Braunschweig*

C3L-M.1 **Memory Efficient Architecture for Belief Propagation Based Disparity Estimation.....2521**
Sih-Sian Wu, Hong-Hui Chen, Chen-Han Tsai, Liang-Gee Chen
National Taiwan University, Taiwan

C3L-M.2 **Real-Time Free Viewpoint Synthesis Using Three-Camera Disparity Estimation Hardware 2525**
Abdulkadir Akin, Raffaele Capoccia, Jonathan Narinx, Jonathan Masur, Alexandre Schmid, Yusuf Leblebici
École Polytechnique Fédérale de Lausanne, Switzerland

C3L-M.3 **Frame Compatible Format Fast Encoder with Stereo Matching.....2529**
Wen Xin Yu[2], Liang Yu[2], Weichen Wang[1], Jiu Xu[3]
[1]KLab Inc., Japan; [2]Southwest University of Science and Technology, China; [3]Waseda University, Japan

C3L-M.4 **Scene-Adaptive Parallax Adjustment for Parallel Stereoscopic Imaging ..... N/A**
Chunhui Cui, Qichang Li, Lei Song, Ning Liu
SuperD Co., Ltd, China

C3L-M.5 **An Efficient and High Quality Rasterization Algorithm and Architecture in 3D Graphics Systems 2537**
Yeong-Kang Lai, Yu-Chieh Chung
National Chung Hsing University, Taiwan

C4L-A: Memory Circuits and Architectures I

Time: Wednesday, May 27 (14:10-15:40)
Room: Main Auditorium
Chair(s): Mohsin Jamali, *University of Toledo*
Leonel Sousa, *INESC-ID*

C4L-A.1 **Robust Via-Programmable ROM Design Based on 45nm Process Considering Process Variation and Enhancement Vmin and Yield 2541**
Byung Jun Jang[2], Chan Ho Lee[1], Sung Hun Sim[1], Kyu Won Choi[1], Do Hun Byun[1], Yeon Ho Jung[1], Ki Man Park[1], Dong Yeon Heo[1], Gyu Hong Kim[1], Joon Sung Yang[3]
[1]Samsung Electronics Co. Ltd, Korea, South; [2]Samsung Electronics Co. Ltd & Sungkyunkwan University, Korea, South; [3]Sungkyunkwan University, Korea, South

C4L-A.2 **Design of High-Temperature SRAM for Reliable Operation Beyond 250°C 2545**
Radisav Cojbasic, Yusuf Leblebici
École Polytechnique Fédérale de Lausanne, Switzerland

C4L-A.3 **A 28nm 36kb High Speed 6T SRAM with Source Follower PMOS Read and Bit-Line Under-Drive 2549**
Chi-Hao Hong[2], Yi-Wei Chiu[2], Chun-Kai Zhao[2], Shyh-Jye Jou[2], Wen-Tai Wang[1], Reed Lee[1]
[1]Global Unichip Corporation, Taiwan; [2]National Chiao Tung University, Taiwan

C4L-A.4 **A 32kb 9T SRAM with PVT-Tracking Read Margin Enhancement for Ultra-Low Voltage Operation 2553**
Anh Tuan Do, Kiat Seng Yeo, Tony Kim
Nanyang Technological University, Singapore

C4L-A.5 **A Control Scheme for Eliminating Garbage Collection During High-Speed Analysis of Big-Graph Data Stored in NAND Flash Memory 2557**
Hiroshi Uchigaito, Seiji Miura, Takumi Nito
Central Research Laboratory of Hitachi, Ltd., Japan

C4L-B: SPECIAL SESSION: Digitally Intensive Frequency Synthesizers for All-Digital Transmitters in the Nano

Time: Wednesday, May 27 (14:10-15:40)
Room: Small Auditorium
Chair(s): Paul Sotiriadis, *Johns Hopkins University*
Michael Peter Kennedy, *University College Cork*

C4L-B.1 **Spurs-Free Single-Bit-Output Frequency Synthesizers for Fully-Digital RF Transmitters 2561**
Paul Sotiriadis
National Technical University of Athens, Greece

C4L-B.2 **Fractional Spur Suppression in All-Digital Phase-Locked Loops 2565**
Peng Chen[2], Coby Huang[1], Bogdan Staszewski[3]
[1]IMEC - Holst Centre, Netherlands; [2]Technische Universiteit Delft, Netherlands; [3]University College Dublin, Ireland

C4L-B.3 **DPLL with Hybrid Delta-Sigma Phase/Frequency Detector 2569**
Ioannis Syllaios, Henrik Jensen
Broadcom Corporation, United States

C4L-B.4 **Enabling Highly Energy Efficient WSN Through PLL-Free, Fast Wakeup Radios..... 2573**
Raghavasimhan Thirunarayanan[2], David Ruffieux[3], Christian Enz[1]
[1]École Polytechnique Fédérale de Lausanne, Switzerland; [2]École Polytechnique Fédérale de Lausanne / Swiss Center for Electronics and Microtechnology, Switzerland; [3]Swiss Center for Electronics and Microtechnology, Switzerland

C4L-B.5 **The Noise and Spur Delusion in Fractional-N Frequency Synthesizer Design 2577**
Michael Kennedy[2], Hongjia Mo[2], Zhida Li[2], Guosheng Hu[2], Paolo Scognamiglio[1], Ettore Napoli[1]
[1]Università degli Studi di Napoli Federico II, Italy; [2]University College Cork, Ireland

C4L-C: Low Power Circuits I

Time: Wednesday, May 27 (14:10-15:40)
Room: S1: Luis F. Branco
Chair(s): Oscar Gustafsson, *Linköping University, Sweden*
Ram Krishnamurthy, *Intel Corporation*

C4L-C.1 **Linearity Efficiency Factor and Power-Efficient Operational Transconductance Amplifier in Subthreshold Operation 2581**
Tzu-Yun Wang, Li-Han Liu, Min-Rui Lai, Sheng-Yu Peng
National Taiwan University of Science and Technology, Taiwan

C4L-C.2 **A 6.42 mW Low-Power Feed-Forward FxLMS ANC VLSI Design for in-Ear Headphones 2585**
Hong-Son Vu, Kuan-Hung Chen, Shih-Feng Sun, Tien-Mau Fong, Che-Wei Hsu, Lei Wang
Feng Chia University, Taiwan

C4L-C.3 **A Single-VDD Half-Clock-Tolerant Fine-Grained Dynamic Voltage Scaling Pipeline 2589**
Rong Zhou, Kwen-Siong Chong, Tong Lin, Bah-Hwee Gwee, Joseph Sylvester Chang
Nanyang Technological University, Singapore

C4L-C.4 **Power Optimization Design for Probabilistic Logic Circuits 2593**
Ran Xiao, Chunhong Chen
University of Windsor, Canada

C4L-C.5 **Ultra-Low-Energy Adiabatic Dynamic Logic Circuits Using NanoElectroMechanical Switches 2596**
Christopher Ayala[2], Antonios Bazigos[1], Daniel Grogg[4], Yu Pu[3], Christoph Hagleitner[2]
[1]Ecole Polytechnique Fédérale de Lausanne, Switzerland; [2]IBM Research - Zurich, Switzerland; [3]Qualcomm Inc, United States; [4]TE Connectivity Ltd., Switzerland

C4L-D: Digital Filter Banks and Transforms

Time: Wednesday, May 27 (14:10-15:40)
Room: S2: E. Andrade
Chair(s): Yong Ching Lim, *Nanyang Technological University*
Tapio Saramäki, *Tampere University of Technology, Finland*

C4L-D.1 **Graph QMF with Flatness Constraints 2600**
David Tay[1], Zhiping Lin[2]
[1]LaTrobe University, Australia; [2]Nanyang Technological University, Singapore

C4L-D.2 **Multi-Window Real-Valued Discrete Gabor Transform for Long and Infinite Sequences 2604**
Liang Tao[1], Hon-Keung Kwan[2]
[1]Anhui University, China; [2]University of Windsor, Canada

C4L-D.3 **Efficient Filter Bank Multicarrier Realizations for 5G 2608**
Leonardo Gomes Baltar, Israa Slim, Josef A. Nossek
Technische Universität München, Germany

C4L-D.4 **Integer-to-Integer Complex Extended Lapped Transform 2612**
Juuso Alhava, Markku Renfors
Tampere University of Technology, Finland

C4L-D.5 **Multi-Beamforming with Uniform Linear Array and Algebraic Integer Quantization Based DCT 2616**
Ziad Gias, Md. Mehedi Hasan, Khan A Wahid
University of Saskatchewan, Canada

C4L-F: Wearable Circuits and Systems

Time: Wednesday, May 27 (14:10-15:40)
Room: S6: A. Negreiros
Chair(s): Wouter Serdijn, *TU Delft*
Joachim Rodrigues, *Lund University*

C4L-F.1 **A Hybrid OFDM Body Coupled Communication Transceiver for Binaural Hearing Aids in 65nm CMOS 2620**
Wala Saadeh, Yonatan Kifle, Jerald Yoo
Masdar Institute of Science and Technology, U.A.E.

C4L-F.2 **A 1.3µW 0.7µVrms Chopper Current-Reuse Instrumentation Amplifier for EEG Applications 2624**
Guocheng Huang, Tao Yin, Qingsong Wu, Yuanming Zhu, Haigang Yang
Chinese Academy of Sciences, University of the Chinese Academy of Science, China

C4L-F.3 **A 400mV Atrial Fibrillation Detector with 0.56 pJ/Operation in 65 nm CMOS 2628**
Oskar Andersson, Joachim Rodrigues
Lund University, Sweden

C4L-F.4 **A 5-Tissue-Layer Lumped-Element Based HBC Circuit Model Compatible to IEEE802.15.6 ..... 2632**
Jingna Mao[1], Bo Zhao[1], Yong Lian[2], Huazhong Yang[1]
[1]Tsinghua University, China; [2]York University, Canada

C4L-F.5 **An Inertial Sensor Based Balance and Gait Analysis System 2636**
Wei-Hsin Wang[2], Pau-Choo Chung[2], Guo-Liang Yang[2], Chien-Wen Lin[2], Yu-Liang Hsu[1], Ming-Chyi Pai[2]
[1]Feng Chia University, Taiwan; [2]National Cheng Kung University, Taiwan

C4L-G: Tools for Analog Design

Time: Wednesday, May 27 (14:10-15:40)
Room: S7: S. M. Breyner
Chair(s): Nuno Horta, *Instituto Superior Técnico, Lisboa, Portugal*
Igor Filanovsky, *University of Alberta*

C4L-G.1 **Determining Potentially Unstable Operating Points Using Time-Varying Root-Locus 2640**
Jani Järvenhaara[1], Nikolay Tchamov[1], Igor Filanovsky[2]
[1]Tampere University of Technology, Finland; [2]University of Alberta, Canada

C4L-G.2 **Topological Symbolic Simplification for Analog Design 2644**
Hanbin Hu[1], Guoyong Shi[1], Andy Tai[2], Frank Lee[2]
[1]Shanghai Jiao Tong University, China; [2]Synopsys, Inc., United States

C4L-G.3 **A Low-Voltage, Low-Power Amplifier Created by Reasoning-Based, Systematic Topology Synthesis 2648**
Fanshu Jiao, Alex Doboli
Stony Brook University, United States

C4L-G.4 **A Novel Yield Aware Multi-Objective Analog Circuit Optimization Tool 2652**
Gönenç Berkol, Engin Afacan, Günhan Dündar, Ali Emre Pusane, Ismail Faik Baskaya
Bogazici University, Turkey

C4L-J: Analog Filtering I

Time: Wednesday, May 27 (14:10-15:40)
Room: S9: M.H.V. Silva
Chair(s): Nuno Paulino, *UNINOVA*
Hyongsuk Kim, *Chonbuk National University*

C4L-J.1 **A 4th-Order Low-Power Diode-C-Based Filter with 12 dBm-IIP3 at the Cut-Off Frequency 2656**
Antonio D'Amico[2], Marcello De Matteis[2], Stefano D'Amico[3], Lorenzo Crespi[1], Andrea Baschirotto[2]
[1]Conexant Systems, Inc., United States; [2]Università degli Studi Milano-Bicocca, Italy; [3]Università del Salento, Italy

C4L-J.2 **An Analog Adaptive Notch Filter Based on the Noise Cancellation Principle..... 2660**
Ahmad Rezazadehreyhani[2], Chetan Jayanthmurthy[2], Bill Gillman[1], Jeffrey Walling[2], John Belz[2], Behrouz Farhang-Boroujeny[2]
[1]Gillman & Associates, United States; [2]University of Utah, United States

C4L-J.3 **LC Filters with Enhanced Memristive Damping..... 2664**
Vasileios Ntinas, Ioannis Vourkas, Georgios Ch. Sirakoulis
Dimocritus University of Thrace, Greece

C4L-J.4 **Pole Frequency and Pass-Band Gain Tunable Novel Fully-Differential Current-Mode All-Pass Filter..... 2668**
Norbert Herencsar[1], Jan Jerabek[1], Jaroslav Koton[1], Kamil Vrba[1], Shahram Minaei[2], Izzet Cem Göknar[2]
[1]Brno University of Technology, Czech Rep.; [2]Dogus University, Turkey

C4L-J.5 **Design of Wide-Band Amplifiers/Filters Using Lommel Polynomials 2672**
Igor Filanovsky
University of Alberta, Canada

C4L-K: Complex Networks Analysis and Applications I

Time: Wednesday, May 27 (14:10-15:40)
Room: S10: A.S. Cardoso
Chair(s): Jinhu Lu, *Academy of Mathematics and Systems Science, Chinese Academy of Sciences*
Yoshifumi Nishio, *Tokushima University*

C4L-K.1 **Optimal Resource Allocation Under TCP Reno and Vegas in Complex Communication Networks 2676**
Huiyun Liu, Yongxiang Xia
Zhejiang University, China

C4L-K.2 **Cooperative Design of Networked Observers for Stabilizing LTI Plants 2680**
Kexin Liu[1], Henghui Zhu[1], Jinhu Lü[1], Maciej J. Ogorzalek[2]
[1]Chinese Academy of Sciences, University of the Chinese Academy of Science, China; [2]Jagiellonian University, Poland

C4L-K.3 **Assessment of Robustness of Power Systems from the Perspective of Complex Networks 2684**
Xi Zhang, Chi Kong Tse
Hong Kong Polytechnic University, Hong Kong

C4L-K.4 **Topological Bifurcations in Networks of Proximity Kuramoto Oscillators 2688**
Pietro DeLellis, Francesco Garofalo, Francesco Lo Iudice, Giovanni Pugliese Carratelli
Università di Napoli Federico II, Italy

C4L-K.5 **Cluster-Based Informed Agents Selection for Flocking with a Virtual Leader 2692**
Nuwan Ganganath[1], Chi-Tsun Cheng[1], Chi Kong Tse[1], Xiaofan Wang[2]
[1]Hong Kong Polytechnic University, Hong Kong; [2]Shanghai Jiao Tong University, China

C4L-L: Neuromorphic and Spiking Neural Systems

Time: Wednesday, May 27 (14:10-15:40)
Room: S11: C. Telmo
Chair(s): Chiara Bartolozzi, *Istituto Italiano di Tecnologia*
Tobi Delbruck, *Institute of Neuroinformatics, UZH / ETH-Zurich*

C4L-L.1 **Efficient Event-Driven Approach Using Synchrony Processing for Hardware Spiking Neural Networks 2696**
Guillaume Séguin-Godin, Frédéric Mailhot, Jean Rouat
Université de Sherbrooke, Canada

C4L-L.2 **Case Study: Bio-Inspired Self-Adaptive Strategy for Spike-Based PID Controller 2700**
Junxiu Liu[2], Jim Harkin[2], Malachy McElholm[2], Liam McDaid[2], Angel Jimenez-Fernandez[1], Alejandro Linares-Barranco[1]
[1]Universidad de Sevilla, Spain; [2]University of Ulster, United Kingdom

C4L-L.3 **Gibbs Sampling with Low-Power Spiking Digital Neurons 2704**
Srinjoy Das[2], Bruno Umbria Pedroni[2], Paul Merolla[1], John Arthur[1], Andrew Cassidy[1], Bryan Jackson[1], Dharmendra Modha[1], Gert Cauwenberghs[2], Ken Kreutz-Delgado[2]
[1]IBM Research Almaden, United States; [2]University of California, San Diego, United States

C4L-L.4 **Decision Making and Perceptual Bistability in Spike-Based Neuromorphic VLSI Systems 2708**
Federico Corradi[2], Hongzhi You[3], Massimiliano Giulioni[1], Giacomo Indiveri[2]
[1]Istituto Superiore di Sanita, Italy; [2]Universität Zürich and ETH Zürich, Switzerland; [3]University of Electronic Science and Technology of China, China

C4L-L.5 **Design of a QDI Asynchronous AER Serializer/Deserializer Link in 180nm for Event-Based Sensors for Robotic Applications 2712**
Giovanni Rovere[2], Chiara Bartolozzi[2], Nabil Imam[1], Rajit Manohar[1]
[1]Cornell Tech, United States; [2]Istituto Italiano di Tecnologia, Italy

C4L-M: Nano-Electronics III

Time: Wednesday, May 27 (14:10-15:40)
Room: S12: D. Costa
Chair(s): Antonio Rubio, *UPC Barcelona, Spain*

C4L-M.1 **Design Exploration of Graphene-FET Based Ring-Oscillator Circuits: a Test-Bench for Large-Signal Compact Models 2716**
Mario Iannazzo[3], Valerio Lo Muzzo[2], Saul Rodriguez[1], Ana Rusu[1], Max Lemme[4], Eduard Alarcón[3]
[1]KTH Royal Institute of Technology, Sweden; [2]Politecnico di Milano, Italy; [3]Universitat Politècnica de Catalunya, Spain; [4]Universität Siegen, Germany

C4L-M.2 **Carbon-Based Sleep Switch Dynamic Logic Circuits with Variable Strength Keeper for Lower-Leakage Currents and Higher-Speed 2720**
Yanan Sun, Volkan Kursun
Hong Kong University of Science and Technology, China

C4L-M.3 **Low Cost and Energy, Thermal Noise Driven, Probability Modulated Random Number Generator 2724**
Nicoleta Cucu Laurenciu, Sorin Dan Cotofana
Technische Universiteit Delft, Netherlands

C4L-M.4 **Towards Probabilistic Analog Behavioral Modeling 2728**
André Lange[2], Ihor Harasymiv[2], Oliver Eisenberger[1], Frédéric Roger[1], Joachim Haase[2], Rainer Minixhofer[1]
[1]ams AG, Austria; [2]Fraunhofer Institute for Integrated Circuits, Germany

C4L-M.5 **Fault-Aware Configurable Logic Block for Reliable Reconfigurable FPGAs 2732**
Chagun Basha Basheer[3], Sébastien Pillement[1], Stanislaw J. Piestrak[2]
[1]L'UNAM University, France; [2]University of Lorraine, France; [3]University of Rennes 1, France

C5P-N: Media Coding and Processing

Time: Wednesday, May 27 (14:10-16:00)
Room: 2nd Floor Foyer
Chair(s): Maria Trocan, *Institut Supérieur d'Électronique de Paris*
Ce Zhu, *University of Electronic Science and Technology of China*

C5P-N.1 **Down-Sampling Based Embedded Compression in Video Systems 2736**
Yuxiang Shen, Xiaolin Wu
McMaster University, Canada

C5P-N.2 **Reordering-Based Transform for Compressing Human Motion Capture Data.....2740**
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Nanyang Technological University, Singapore

C5P-N.3 **Joint Quantization and Diffusion for Compressed Sensing Measurements of Natural Images 2744**
Leo Yu Zhang[1], Kwok-Wo Wong[1], Yushu Zhang[3], Qiuzhen Lin[2]
[1]City University of Hong Kong, Hong Kong; [2]Shenzhen University, China; [3]Southwest University, China

C5P-N.4 **An Efficient HEVC to H.264/AVC Transcoding System 2748**
Minhao Tang, Jiangtao Wen
Tsinghua University, China

C5P-N.5 **Massively Parallel KD-Tree Construction and Nearest Neighbor Search Algorithms...2752**
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[1]Michigan Tech, United States; [2]University of Windsor, Canada

C5P-N.6 **Adapting Hierarchical Als Algorithms for Temporal Psychovisual Modulation.....2756**
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[1]Institute of Image Communication and Information Processing, Shanghai Jiao Tong University, China; [2]Shanghai Jiao Tong University, China; [3]Universidade de Macau, China

C5P-N.7 **High-Quality Texture Compression Using Adaptive Color Grouping and Selection Algorithm.....2760**
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[1]Himax Technologies, Inc., Taiwan; [2]National Cheng Kung University, Taiwan

C5P-P: 3D Visual Signal Coding and Advanced Video Coding

Time: Wednesday, May 27 (14:10-16:00)
Room: 2nd Floor Foyer
Chair(s): Lap-Pui Chau, *Nanyang Technological University*
Guangtao Zhai, *Shanghai Jiaotong University*

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[1]Beijing Institute of Technology, China; [2]Beijing University, China; [3]Peking University, China

C5P-P.2 **A Linear Dependent Rate-Quantization Model for Scalable Video Enhancement Layer Encoding.....2768**
Junhui Hou[1], Shuai Wan[2], Zhan Ma[3], Lap-Pui Chau[1]
[1]Nanyang Technological University, Singapore; [2]Northwestern Polytechnical University, China; [3]Samsung Research America, United States

C5P-P.3 **Improvements on Intra Block Copy in Natural Content Video Coding.....2772**
Haoming Chen[2], Yu-Sheng Chen[2], Ming-Ting Sun[2], Ankur Saxena[1], Madhukar Budagavi[1]
[1]Samsung Research America, United States; [2]University of Washington, United States

C5P-P.4 **Disparity-Compensated Inter-Layer Motion Prediction Using Standardized HEVC Extensions 2776**
Li Chen[2], Miska Hannuksela[1], Houqiang Li[2]
[1]Nokia Technologies, Finland; [2]University of Science and Technology of China, China

C5P-P.5 **Fast Segment-Wise DC Coding for 3D Video Compression 2780**
Zhouye Gu[2], Jianhua Zheng[1], Nam Ling[2], Philipp Zhang[1]
[1]Huawei Technologies Co., Ltd. / HiSilicon, United States; [2]Santa Clara University, United States

C5P-Q: HEVC and Standard Video Coding

Time: Wednesday, May 27 (14:10-16:00)
Room: 2nd Floor Foyer
Chair(s): Lap-Pui Chau, *Nanyang Technological University*
Guangtao Zhai, *Shanghai Jiaotong University*

C5P-Q.2 **Context-Adaptive Fast Motion Estimation of HEVC 2784**
Xufeng Li, Ronggang Wang, Xiaole Cui, Wenmin Wang
Peking University, China

C5P-Q.3 **Lambda Domain Based Optimal Bit Allocation for Scalable High Efficiency Video Coding 2788**
Li Li, Houqiang Li
University of Science and Technology of China, China

C5P-Q.4 **Hierarchical Fast Mode Decision Algorithm for Intra Prediction in HEVC 2792**
Tae Sun Kim[1], Myung Hoon Sunwoo[1], Jin-Gyun Chung[2]
[1]Ajou University, Korea, South; [2]Chonbuk National University, Korea, South

C5P-R: Efficient Visual Signal Analysis and Identification

Time: Wednesday, May 27 (14:10-16:00)
Room: 2nd Floor Foyer
Chair(s): Jing-Ming Guo, *National Taiwan University of Science and Technology*
Ming-Jen Tsai, *National Chiao Tung University*

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Yazhong Zhang, Jinjian Wu, Guangming Shi, Xuemei Xie
Xidian University, China

C5P-R.2 **Japanese Character Based Printed Source Identification 2800**
Min-Jen Tsai, Chien-Lun Hsu, Jin-Sheng Yin, Imam Yuadi
National Chiao Tung University, Taiwan

C5P-R.3 **Real-Time Vehicle Color Identification Using Symmetrical SURFs and Chromatic Strength..... 2804**
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[1]Lee-Ming Institute of Technology, Taiwan; [2]National Taiwan Ocean University, Taiwan

C5P-R.4 **Real-Time Visual Play-Break Detection in Sport Events Using a Context Descriptor ..2808**
Marc-Andre Carbonneau, Alexandre Jonathan Raymond, Eric Granger, Ghyslain Gagnon
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Time: Wednesday, May 27 (14:10-16:00)
Room: 2nd Floor Foyer
Chair(s): Lap-Pui Chau, *Nanyang Technological University*
Guangtao Zhai, *Shanghai Jiaotong University*

C5P-S.1 **Parameter-Free View Synthesis Distortion Model with Application to Depth Video Coding 2812**
Meng Yang[2], Ce Zhu[1], Xuguang Lan[2], Nanning Zheng[2]
[1]University of Electronic Science and Technology of China, China; [2]Xi'an Jiaotong University, China

C5P-S.2 **A General Histogram Modification Framework for Efficient Contrast Enhancement ... 2816**
Ke Gu[2], Guangtao Zhai[2], Shiqi Wang[4], Min Liu[1], Jiantao Zhou[3], Weisi Lin[1]
[1]Nanyang Technological University, Singapore; [2]Shanghai Jiao Tong University, China; [3]Universidade de Macau, China; [4]University of Waterloo, Canada

C5P-S.3 **Image Guided Label Map Propagation in Video Sequences 2820**
Shuolin Di[2], Zhebin Zhang[2], Shiqi Wang[2], Nan Zhang[1], Siwei Ma[2]
[1]Capital Medical University, China; [2]Peking University, China

C5P-S.4 **Path Optimization for Terrestrial Robots Using Homotopy Path Planning Method 2824**
Gerardo Diaz-Arango[1], Arturo Sarmiento-Reyes[1], Luis Hernandez-Martinez[1], Antonio Marin-Hernandez[2], Hector Vazquez-Leal[2], Damian Dario Lopez-Hernandez[2]
[1]Instituto Nacional de Astrofísica, Óptica y Electrónica, Mexico; [2]Universidad Veracruzana, Mexico

C5P-T: Visual Signal Processing and Communications

Time: Wednesday, May 27 (14:10-16:00)
Room: 2nd Floor Foyer
Chair(s): Chris Lee, *National Cheng Kung University*
Cai Jianfei, *Nanyang Technological University*

C5P-T.1 **High Performance IP Core for HEVC Quantization.....2828**
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INESC-ID / Universidade de Lisboa, Portugal

C5P-T.2 **An FPGA Processor for Real-Time, Fixed-Point Refinement of CDVS Keypoints.....2832**
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Università degli Studi di Napoli Federico II, Italy

C5P-T.3 **Using the Cs Decomposition to Compute the 8-Point DCT 2836**
Marek Parfieniuk
Bialystok University of Technology, Poland

C5P-U: Millimeter-Wave & Optical Communications Circuits

Time: Wednesday, May 27 (14:10-16:00)
Room: 2nd Floor Foyer
Chair(s): Wei Xing Zheng, *University of Western Sydney*
Maire O'Neill, *Queens University*

C5P-U.1 **A 24GHz Low Power and Low Phase Noise PLL Frequency Synthesizer with Constant KVCO for 60GHz Wireless Applications.....2840**
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Tsinghua University, China

C5P-U.3 **Design and Optimization of a 94GHz Rotary Traveling Wave Oscillator for mm-Wave Applications.....2844**
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Cairo University, Egypt

C5P-U.4 **A Wideband Transformer-Coupled Frequency Quadrupler Using an Asymmetrical Balun in 0.25μm SiGe for Backhaul Communication 2848**
Sudipta Chakraborty, Xi Zhu, Oya Sevimli, Michael Heimlich
Macquarie University, Australia

C5P-V: Wireline Communications I

Time: Wednesday, May 27 (14:10-16:00)
Room: 2nd Floor Foyer
Chair(s): Wei Xing Zheng, *University of Western Sydney*
An-Yeu Andy Wu, *National Taiwan University*

C5P-V.1 **A Fast-Settling High Linearity Auto Gain Control for Broadband OFDM-Based PLC System.....2852**
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National Taiwan University, Taiwan

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[1]Electronics and Telecommunications Research Institute, Korea, South; [2]Seoul National University, Korea, South

C5P-V.3 **A 0.38 pJ/Bit 1.24 nW Chip-to-Chip Serial Link for Ultra-Low Power Systems.....2860**
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University of Virginia, United States

C5P-V.4 **20-Gb/s 3.6-Vpp-Swing Source-Series-Terminated Driver with 2-Tap FFE in 65-nm CMOS.....2864**
Jun-Eun Park[2], Yoonsoo Kim[2], Sungwoo Kim[2], Gyungock Kim[1], Deog-Kyoon Jeong[2]
[1]Electronics and Telecommunications Research Institute, Korea, South; [2]Seoul National University, Korea, South

C5P-V.5 **Minimum Jitter Adaptive Decision Feedback Equalizer for 4PAM Serial Links 2868**
Alaa Al-Taee, Fei Yuan, Andy Ye
Ryerson University, Canada

C5P-W: CANDE (Computer-Aided Network Design) Posters

Time: Wednesday, May 27 (14:10-16:00)
Room: 2nd Floor Foyer
Chair(s): Philippe Coussy, *Universite de Bretagne-Sud*

C5P-W.1 **Multicore Power Proxies Using Least-Angle Regression 2872**
Rupesh Karn, Ibrahim Elfadel
Masdar Institute of Science and Technology, U.A.E.

C5P-W.2 **Combinational Fault Simulation in Sequential Circuits 2876**
Raimund Ubar[1], Jaak Kõusaar[1], Maksim Gorev[1], Sergei Devadze[2]
[1]Tallinn University of Technology, Estonia; [2]University of Technology, Estonia

C5P-W.3 **Optimization of Memory Banking in Embedded Multidimensional Signal Processing Applications 2880**
Florin Balasa[1], Noha Abuaesh[1], Cristian V. Gingu[3], Hongwei Zhu[2]
[1]American University in Cairo, Egypt; [2]ARM, Inc., United States; [3]Fermilab, United States

C5P-W.4 **Approximation of Multiple Constant Multiplications Using Minimum Look-Up Tables on FPGA 2884**
Levent Aksoy, Paulo Flores, José Monteiro
INESC-ID / Universidade de Lisboa, Portugal

C5P-W.5 **Inductive Coupling Effects in Large TSV Arrays 2888**
Kan Xu, Eby Friedman
University of Rochester, United States

C6L-A: Memory Circuits and Architectures II

Time: Wednesday, May 27 (16:00-17:30)
Room: Main Auditorium
Chair(s): Mohsin Jamali, *University of Toledo*
Alexander Fish, *Ben-Gurion University of the Negev*

C6L-A.1 **0.5-V Sub-ns Open-BL SRAM Array with Mid-Point-Sensing Multi-Power 5T Cell 2892**
Kiyoo Itoh, Khajaahmad Shaik, Amara Amara
Institut supérieur d'électronique de Paris, France

C6L-A.2 **Analysis of Radiation Effect on the Threshold Voltage of Flash Memory Device 2896**
Nahid Hossain, Jitendra Koppu, Masud Chowdhury
University of Missouri-Kansas City, United States

C6L-A.3 **Delay and Power Tradeoffs for Static and Dynamic Register Files.....2900**
Vinay Vashishtha, Aditya Gujja, Lawrence Clark
Arizona State University, United States

C6L-A.4 **A Low Power 6T-4C Non-Volatile Memory Using Charge Sharing and Non-Precharge Techniques 2904**
Tomoki Nakagawa[1], Shintaro Izumi[1], Koji Yanagida[1], Yuki Kitahara[1], Shusuke Yoshimoto[1], Yohei Umeki[1], Haruki Mori[1], Hiroto Kitahara[1], Hiroshi Kawaguchi[1], Hiromitsu Kimura[2], Kyoji Marumoto[2], Takaaki Fuchikami[2], Yoshikazu Fujimori[2],
[1]Kobe University, Japan; [2]Rohm Co. Ltd., Japan

C6L-A.5 **Parallel Pipelining Configurable Multi-Port Memory Controller for Multimedia Applications 2908**
Xuan-Thuan Nguyen, Hong-Thu Nguyen, Cong-Kha Pham
University of Electro-Communications, Japan

C6L-B: SPECIAL SESSION: Carbon-Based Circuits and Systems

Time: Wednesday, May 27 (16:00-17:30)
Room: Small Auditorium
Chair(s): Ana Rusu, *KTH Sweden*
José M de la Rosa, *IMSE-CNM (CSIC/University of Seville), Spain*

C6L-B.1 **Overview of Carbon-Based Circuits and Systems 2912**
Saul Rodriguez[2], Ana Rusu[2], Jose M. de la Rosa[1]
[1]Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, Spain; [2]KTH Royal Institute of Technology, Sweden

C6L-B.2 **Graphene Based GHz Flexible Nanoelectronics and Radio Receiver Systems (Invited)..... 2916**
Maruthi Yogeesh, Saungeun Park, Deji Akinwande
University of Texas at Austin , United States

C6L-B.3 **Graphene FET Evaluation for RF and mmWave Circuit Applications 2920**
Sebastien Frégonèse, Jorgue Daniel Aguirre Morales, Magali de Matos, Cristell Maneux, Thomas Zimmer
Université de Bordeaux, France

C6L-B.4 **Time-Based Sensor Interface Circuits in Carbon Nanotube Technology 2924**
Georges Gielen[1], Jelle Van Rethy[1], Max Shulaker[2], Gage Hills[2], Philip Wong[2], Subhasish Mitra[2]
[1]Katholieke Universiteit Leuven, Belgium; [2]Stanford University, United States

C6L-B.5 **Near-Threshold CNTFET SRAM Cell Design with Removed Metallic CNT Tolerance ... 2928**
Jose Delgado-Frias[2], Zhe Zhang[2], Michael Turi[1]
[1]Pacific Lutheran University, United States; [2]Washington State University, United States

C6L-C: Low Power Circuits II

Time: Wednesday, May 27 (16:00-17:30)
Room: S1: Luis F. Branco
Chair(s): Kwen-Siong Chong, *Nanyang Technological University*
Yeong-Kang Lai, *National Chung Hsing University*

C6L-C.1 **2-Phase High-Frequency Clock Distribution with SPLIT-IO Dual-Vt Repeaters for Suppressed Leakage Currents 2932**
Hong Zhu, Volkan Kursun
Hong Kong University of Science and Technology, Hong Kong

C6L-C.2 **STT-RAM Write Energy Consumption Reduction by Differential Write Termination Method 2936**
Hooman Farkhani[3], Ali Peiravi[3], Jens Kargaard Madsen[1], Farshad Moradi[2]
[1]Aarhus University, Denmark; [2]Aarhus Universtiy, Denmark; [3]Ferdowsi University of Mshhad, Iran

C6L-C.3 **Improved Bus-Shift Coding for Low-Power I/O 2940**
Mohammed Alamgir, Iftekhar Basith, Tareq Supon, Rashid Rashidzadeh
University of Windsor, Canada

C6L-C.4 **Reactive Rejuvenation of CMOS Logic Paths Using Self-Activating Voltage Domains 2944**
Rizwan A. Ashraf, Ahmad Al-Zahrani, Navid Khoshavi, Ramtin Zand, Soheil Salehi, Arman Roohi, Mingjie Lin, Ronald F. Demara
University of Central Florida, United States

C6L-C.5 **A 0.19-V Minimum Input Low Energy Level Shifter for Extremely Low-Voltage VLSIs 2948**
Ryo Matsuzuka, Tetsuya Hirose, Yuzuru Shizuku, Nobutaka Kuroki, Masahiro Numa
Kobe University, Japan

C6L-D: FIR and IIR Digital Filters

Time: Wednesday, May 27 (16:00-17:30)
Room: S2: E. Andrade
Chair(s): Wu-Sheng Lu, *University of Victoria, Canada*
Takao Hinamoto, *Hiroshima Institute of Technology*

C6L-D.1 **Optimal Design of Composite Digital Filters Using Convex-Concave Procedure.....2952**
Wu-Sheng Lu[2], Takao Hinamoto[1]
[1]Hiroshima University, Japan; [2]University of Victoria, Canada

C6L-D.2 **Optimal Error Feedback and Realization for Roundoff Noise Minimization in Linear Discrete-Time Systems with Full-Order State Observer Feedback 2956**
Takao Hinamoto[1], Akimitsu Doi[1], Wu-Sheng Lu[2]
[1]Hiroshima University, Japan; [2]University of Victoria, Canada

C6L-D.3 **Design of Low Complexity Programmable FIR Filters Using Multiplexers Array Optimization 2960**
Weiao Ding, Jiajia Chen
Singapore University of Technology and Design, Singapore

C6L-D.4 **Design of High-Speed Multiplierless Linear-Phase FIR Filters.....2964**
Wenbin Ye, Xin Lou, Ya Jun Yu
Nanyang Technological University, Singapore

C6L-D.5 **IIR Filter Design with Novel Stability Condition.....2968**
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[1]Changzhou University, China; [2]Hohai University, China; [3]University of Windsor, Canada

C6L-E: MIMO Communication Systems

Time: Wednesday, May 27 (16:00-17:30)
Room: S5: F. Pessoa
Chair(s): Joe Cavallaro, *Rice University*
An-Yeu Andy Wu, *National Taiwan University*

C6L-E.1 **Hardware Implementation of the SUMIS Detector Using High-Level Synthesis.....2972**
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Johannes Kepler Universität Linz, Austria

C6L-E.2 **A Customized Lattice Reduction Multiprocessor for MIMO Detection.....2976**
Shahriar Shahabuddin, Janne Janhunen, Zaheer Khan, Markku Juntti, Amanullah Ghazi
University of Oulu, Finland

C6L-E.3 **Multi-Mode Sorted QR Decomposition for 4x4 and 8x8 Single-User/Multi-User MIMO Precoding 2980**
Chi-Mao Chen, Chih-Hsiang Lin, Pei-Yun Tsai
National Central University, Taiwan

C6L-E.4 **A 350 µW Sign-Bit Architecture for Multi-Parameter Estimation During OFDM Acquisition in 65 nm CMOS 2984**
Isael Diaz[2], Siyu Tan[2], Yun Miao[2], Leif Wilhelmsson[1], Ove Edfors[2], Viktor Öwall[2]
[1]Ericsson Research, Sweden; [2]Lund University, Sweden

C6L-E.5 **A 8-mW 77-GHz Band CMOS LNA by Using Reduced Simultaneous Noise and Impedance Matching Technique.....2988**
Chun-Lin Ko[2], Chun-Hsing Li[3], Chien-Nan Kuo[4], Ming-Ching Kuo[1], Da-Chiang Chang[5]
[1]Industrial Technology Research Institute, Taiwan; [2]National Applied Research Laboratories, Taiwan; [3]National Central University, Taiwan; [4]National Chiao Tung University, Taiwan; [5]National Nano Device Laboratories / National Applied Research Lab

C6L-F: Neural Recording Circuits and Systems

Time: Wednesday, May 27 (16:00-17:30)
Room: S6: A. Negreiros
Chair(s): Arindam Basu, *Nanyang Technological University*
Tim Constandinou, *Imperial college*

C6L-F.1 **A 16-Channel 24-V 1.8-Ma Power Efficiency Enhanced Neural/Muscular Stimulator with Exponentially Decaying Stimulation Current.....2992**
Xu Liu[4], Lei Yao[1], Peng Li[3], Mei Yan[3], Shih-Cheng Yen[4], Hao Yu[3], Minkyu Je[2], Yong Ping Xu[4]
[1]Agency for Science, Technology and Research, Singapore; [2]Daegu Gyeongbuk Institute of Science and Technology, Korea, South; [3]Nanyang Technological University, Singapore; [4]National University of Singapore, Singapore

C6L-F.2 **Design of a Low-Noise, High Power Efficiency Neural Recording Front-End with an Integrated Real-Time Compressed Sensing Unit 2996**
Xilin Liu, Hongjie Zhu, Milin Zhang, Andrew Richardson, Timothy Lucas, Jan Van der Spiegel
University of Pennsylvania, United States

C6L-F.3 **A Novel Neural Recording System Utilising Continuous Time Energy Based Compression.....3000**
Konstantinos Faliagkas, Lieuwe Leene, Timothy Constandinou
Imperial College London, United Kingdom

C6L-F.4 **A 128 Channel 290 GMACs/W Machine Learning Based Co-Processor for Intention Decoding in Brain Machine Interfaces 3004**
Yi Chen, Enyi Yao, Arindam Basu
Nanyang Technological University, Singapore

C6L-F.5 **Power Optimization of Neural Frontend Interfaces 3008**
Majid Zamani, Andreas Demosthenous
University College London, United Kingdom

C6L-G: Analog Circuits Testing and Verification I

Time: Wednesday, May 27 (16:00-17:30)
Room: S7: S. M. Breyner
Chair(s): Vadim Ivanov, *Texas Instruments*
Igor Filanovsky, *University of Alberta*

C6L-G.1 **Subblock-Level Matching Layout for Analog Block-Pair and its Manufacturability Evaluation 3012**
Takuya Hirata[2], Ryuta Nishino[2], Shigetoshi Nakatake[2], Masaya Shimoyama[3], Masashi Miyagawa[3], Tanno Koichi[3], Akihiro Yamada[1]
[1]A.LSI.Design Co, Japan; [2]University of Kitakyushu, Japan; [3]University of Miyazaki, Japan

C6L-G.2 **High-Constancy Offset Generator Robust to CDAC Nonlinearity for SEIR-Based ADC BIST 3016**
Yan Duan, Tao Chen, Zhiqiang Liu, Xu Zhang, Degang Chen
Iowa State University, United States

C6L-G.3 **Performance Enhancement Induced Trojan States in Op-Amps, Their Detection and Removal 3020**
Chongli Cai, Degang Chen
Iowa State University, United States

C6L-G.4 **A Calibration Technique for SAR Analog-to-Digital Converter Based on INL Testing with Quantization Bits and Redundant Bit 3024**
Xu Zhang[1], Chongli Cai[1], Hao Meng[1], Siva Sudani[2], Randall Geiger[1], Degang Chen[1]
[1]Iowa State University, United States; [2]Texas Instruments Inc., United States

C6L-G.5 **A 10Gbps Eye Opening Monitor in 65 nm CMOS 3028**
Sandeep Krishnan, Shanthi Pavan
Indian Institute of Technology Madras, India

C6L-H: SPECIAL SESSION: Emerging Channel Decoder Design Techniques for Communication and Memory Systems

Time: Wednesday, May 27 (16:00-17:30)
Room: S8: G. Quartim
Chair(s): Chuan Zhang, *Southeast University*
Yun Chen, *Fudan University, China.*

C6L-H.1 **Pipelined Implementations of Polar Encoder and Feed-Back Part for SC Polar Decoder 3032**
Chuan Zhang[3], Junmei Yang[2], Xiaohu You[2], Shugong Xu[1]
[1]Institute on Mobile Networking and Computing ICRI-MNC, China; [2]National Mobile Communications Research Laboratory, Southeast University, China; [3]Southeast University, China

C6L-H.2 **A Coding Scheme for Improving Random Read Performance in Multi-Bit Flash Memory ..... N/A**
Changkyu Seol, Dongwhan Lee, Dongsup Jin, Hyejeong So, Hongrak Son, Jun Jin Kong
Samsung Electronics Co. Ltd, Korea, South

C6L-H.3 **Successive Cancellation Decoding of Polar Codes Using Stochastic Computing 3040**
Bo Yuan, Keshab K. Parhi
University of Minnesota, United States

C6L-H.4 **Latency-Optimized Stochastic LDPC Decoder for High-Throughput Applications 3044**
Di Wu[1], Yun Chen[1], Qichen Zhang[1], Lirong Zheng[1], Xiaoyang Zeng[1], Yeong-Luh Ueng[2]
[1]Fudan University, China; [2]National Tsing Hua University, Taiwan

C6L-J: Frequency Synthesizers and Oscillators

Time: Wednesday, May 27 (16:00-17:30)
Room: S9: M.H.V. Silva
Chair(s): Luis Oliveira, *Universidade Nova de Lisboa*
Shahriar Mirabbasi, *University of British Columbia*

C6L-J.1 **A 0.6ps Jitter 2-16 GHz 130nm CMOS Frequency Synthesizer for Broadband Applications 3048**
Yung-Chung Lo[2], Negar Rashidi[3], Yin-Huan Hwang[1], Jose Silva-Martinez[3]
[1]Intel Corporation, United States; [2]Qualcomm Inc, United States; [3]Texas A&M University, United States

C6L-J.2 **Design of a Digital Harmonic-Cancelling Sine-Wave Synthesizer with 100 MHz Output Frequency, 43.5 dB SFDR, and 2.26 mW Power 3052**
Pasindu Aluthwala[3], Neil Weste[2], Andrew Adams[1], Torsten Lehmann[3], Sri Parameswaran[3]
[1]Broadcom Corporation, Australia; [2]NHEW R&D Pty. Ltd., Australia; [3]University of New South Wales, Australia

C6L-J.3 **Quadrature Oscillator Solution Suitable with Arbitrary and Electronically Adjustable Phase Shift 3056**
Roman Sotner[1], Jan Jerabek[1], Jiri Petrzela[1], Roman Prokop[1], Kamil Vrba[1], Aslihan Kartci[3], Tomas Dostal[2]
[1]Brno University of Technology, Czech Rep.; [2]College of Polytechnics Jihlava, Czech Rep.; [3]Yildiz Technical University, Turkey

C6L-J.4 **A 1.7-GHz Wide-Band CMOS LC-VCO with 7-Bit Coarse Control 3060**
Carlos Sánchez-Azqueta, Javier Aguirre, Cecilia Gimeno, Concepción Aldea, Santiago Celma
Universidad de Zaragoza, Spain

C6L-J.5 **A 2GHz Direct Digital Frequency Synthesizer Based on Multi-Channel Structure 3064**
Ling Yuan, Qiang Zhang, Yin Shi
Institute of Semiconductors, Chinese Academy of Sciences, China

C6L-K: Analysis and Control of Nonlinear Circuits and Systems

Time: Wednesday, May 27 (16:00-17:30)
Room: S10: A.S. Cardoso
Chair(s): Wei Xing Zheng, *University of Western Sydney*
Abdelali El Aroudi, *Universitat Rovira i Virgili*

C6L-K.1 **An Efficient Method for Control of Continuous-Time Systems Subject to Input Saturation and External Disturbance 3068**
Yunliang Wei[1], Wei Xing Zheng[2]
[1]Nanjing University of Science and Technology, China; [2]University of Western Sydney, Australia

C6L-K.2 **Some Results on Design of Second-Order Sliding Mode Controller for Nonlinear Systems 3072**
Shihong Ding[1], Wei Xing Zheng[2]
[1]Jiangsu University, China; [2]University of Western Sydney, Australia

C6L-K.3 **A New Approach to Finite-Time Tracking of Coupled Continuous Networks 3076**
Wenjun Xiong[1], Wei Xing Zheng[2]
[1]Southwest Petroleum University, China; [2]University of Western Sydney, Australia

C6L-K.4 **Phase and Amplitude Dynamics of Noisy Oscillators Described by Itô Stochastic Differential Equations 3080**
Michele Bonnin, Fabio Traversa, Fernando Corinto, Fabrizio Bonani
Politecnico di Torino, Italy

C6L-K.5 **Cycle Slipping in Nonlinear Circuits Under Periodic Nonlinearities and Time Delays 3084**
Vera Smirnova[1], Anton Proskurnikov[2], Natalia Utina[1]
[1]St.Petersburg State University of Architecture and Civil Engineering, Russia; [2]University of Groningen, Netherlands