

2015 IEEE 23rd Annual International Symposium on Field-Programmable Custom Computing Machines

(FCCM 2015)

**Vancouver, British Columbia, Canada
2-6 May 2015**



IEEE Catalog Number: CFP15054-POD
ISBN: 978-1-4799-9970-5

2015 IEEE 23rd Annual International Symposium on Field-Programmable Custom Computing Machines

FCCM 2015

Table of Contents

Message from the General and Program Chairs.....	xi
Organizing and Technical Program Committees.....	xiii

Trends, Revisits, and Overlays

Technology Scaling in FPGAs: Trends in Applications and Architectures	1
<i>Lesley Shannon, Veronica Cojocaru, Cong Nguyen Dao, and Philip H.W. Leong</i>	
Revisiting Serial Arithmetic: A Performance and Tradeoff Analysis for Parallel	
Applications on Modern FPGAs	9
<i>Aaron Landy and Greg Stitt</i>	
Rapid Overlay Builder for Xilinx FPGAs	17
<i>Michael Xi Yue, Dirk Koch, and Guy G.F. Lemieux</i>	
Adjustable-Cost Overlays for Runtime Compilation	21
<i>James Coole and Greg Stitt</i>	
Efficient Overlay Architecture Based on DSP Blocks	25
<i>Abhishek Kumar Jain, Suhaib A. Fahmy, and Douglas L. Maskell</i>	

Poster Session I

High Performance Sparse LU Solver FPGA Accelerator Using a Static Synchronous	
Data Flow Model	29
<i>Mohamed W. Hassan, Ahmed E. Helal, and Yasser Y. Hanafy</i>	
Cycle-Accurate Replay and Debugging of Running FPGA Systems	30
<i>Sunil Shukla and David F. Bacon</i>	
Heterogeneous Platform to Accelerate Compute Intensive Applications	31
<i>Santhosh Kumar Rethinagiri, Oscar Palomar, Javier Arias Moreno, Osman Unsal,</i>	
<i>and Adrian Cristal</i>	

High Performance Memory Accesses on FPGA-SoCs: A Quantitative Analysis	32
<i>Matthias Göbel, Chi Ching Chi, Mauricio Alvarez-Mesa, and Ben Juurlink</i>	
Sparse Graph Processing with Soft-Processors	33
<i>Nachiket Kapre</i>	
Improving Data Partitioning Performance on OpenCL-Based FPGAs	34
<i>Zeke Wang, Bingsheng He, and Wei Zhang</i>	
Performance and Energy Optimization on MPSoCs by Enabling STT-MRAM LUTs	35
<i>Hongyuan Ding and Miaoqing Huang</i>	

Networking and Compression

Scalable 10Gbps TCP/IP Stack Architecture for Reconfigurable Hardware	36
<i>David Sidler, Gustavo Alonso, Michaela Blott, Kimon Karras, Kees Vissers, and Raymond Carley</i>	
Enabling High Throughput and Virtualization for Traffic Classification on FPGA	44
<i>Yun R. Qu and Viktor K. Prasanna</i>	
A Scalable High-Bandwidth Architecture for Lossless Compression on FPGAs	52
<i>Jeremy Fowers, Joo-Young Kim, Doug Burger, and Scott Hauck</i>	
Enabling Fast and Accurate Emulation of Large-Scale Network on Chip Architectures on a Single FPGA	60
<i>Thiem Van Chu, Shimpei Sato, and Kenji Kise</i>	
Accelerating SpMV on FPGAs by Compressing Nonzero Values	64
<i>Paul Grigoras, Pavel Burovskiy, Eddie Hung, and Wayne Luk</i>	

Power and Energy

Zedwulf: Power-Performance Tradeoffs of a 32-Node Zynq SoC Cluster	68
<i>Pradeep Moorthy and Nachiket Kapre</i>	
Energy-Efficient Acceleration of OpenCV Saliency Computation Using Soft Vector Processors	76
<i>Gopalakrishna Hegde and Nachiket Kapre</i>	
Autotuning FPGA Design Parameters for Performance and Power	84
<i>Azamat Mametjanov, Prasanna Balaprakash, Chekuri Choudary, Paul D. Hovland, Stefan M. Wild, and Gerald Sabin</i>	
FIR Filter Based on Stochastic Computing with Reconfigurable Digital Fabric	92
<i>Mohammed Alawad and Mingjie Lin</i>	

Poster Session II

Accelerating Interconnect Analysis Using High-Level HDLs and FPGA, SpiNNaker as a Case Study	96
<i>Mohsen Ghasempour, Jonathan Heathcote, Javier Navaridas, Luis A. Plana, Jim Garside, and Mikel Luján</i>	
Fast Design Space Exploration Using Vivado HLS: Non-binary LDPC Decoders	97
<i>Joao Andrade, Nithin George, Kimon Karras, David Novo, Vitor Silva, Paolo Ienne, and Gabriel Falcao</i>	
Design of a Distributed Compressor for Astronomy SSD	98
<i>Bo Peng, Xi Jin, Tianqi Wang, and Xueliang Du</i>	
Scalable Key/Value Search in Datacenters	99
<i>John W. Lockwood</i>	
Function Proxies for Improved Resource Sharing in High Level Synthesis	100
<i>Marco Minutoli, Vito Giovanni Castellana, Antonino Tumeo, and Fabrizio Ferrandi</i>	
Automatic Soft CGRA Overlay Customization for High-Productivity Nested Loop Acceleration on FPGAs	101
<i>Cheng Liu and Hayden Kwok-Hay So</i>	
Adaptive Configurable Transactional Memory for Multi-processor FPGA Platforms	102
<i>Jeevan Sirkunam, Chia Yee Ooi, N. Shaikh-Husin, Yuan Wen Hau, and M.N. Marsono</i>	

Machine Learning Techniques

Pipelined Genetic Propagation	103
<i>Liucheng Guo, Ce Guo, David B. Thomas, and Wayne Luk</i>	
FPGA Acceleration of Recurrent Neural Network Based Language Model	111
<i>Sicheng Li, Chunpeng Wu, Hai (Helen) Li, Boxun Li, Yu Wang, and Qinru Qiu</i>	
Driving Timing Convergence of FPGA Designs through Machine Learning and Cloud Computing	119
<i>Nachiket Kapre, Bibin Chandrashekaran, Harnhua Ng, and Kirvy Teo</i>	

Debug, Test, and Fault Detection

Using Dynamic Signal-Tracing to Debug Compiler-Optimized HLS Circuits on FPGAs	127
<i>Jeffrey Goeders and Steve J.E. Wilton</i>	
High-Level Debugging and Verification for FPGA-Based Multicore Architectures	135
<i>Oriol Arcas Abella, Adrián Cristal, and Osman S. Unsal</i>	
Estimating Soft Processor Soft Error Sensitivity through Fault Injection	143
<i>Nathan A. Harward, Michael R. Gardiner, Luke W. Hsiao, and Michael J. Wirthlin</i>	

Protecting against Cryptographic Trojans in FPGAs	151
<i>Pawel Swierczynski, Marc Fyrbiak, Christof Paar, Christophe Huriaux, and Russell Tessier</i>	
Automatic High-Level Hardware Checkpoint Selection for Reconfigurable Systems	155
<i>Alban Bourge, Olivier Muller, and Frédéric Rousseau</i>	
Offline Synthesis of Online Dependence Testing: Parametric Loop Pipelining for HLS	159
<i>Junyi Liu, Samuel Bayliss, and George A. Constantinides</i>	

Poster Session III

HATCH: Hash Table Caching in Hardware for Efficient Relational Join on FPGA	163
<i>Behzad Salami, Oriol Arcas-Abella, and Nehir Sonmez</i>	
Accelerating Big Data Analytics Using FPGAs	164
<i>Katayoun Neshatpour, Maria Malik, Mohammad Ali Ghodrat, and Houman Homayoun</i>	
Massively Parallel Dynamically Reconfigurable Multi-FPGA Computing System	165
<i>Venkatasubramanian Viswanathan, Rabie Ben Atitallah, and Jean-Luc Dekeyser</i>	
A System on Reconfigurable Chip for Handwritten Digit Recognition	166
<i>Luca B. Saldanha and Christophe Bobda</i>	
An Efficient KNN Algorithm Implemented on FPGA Based Heterogeneous Computing System Using OpenCL	167
<i>Yuliang Pu, Jun Peng, Letian Huang, and John Chen</i>	

Applications

Architectures and Precision Analysis for Modelling Atmospheric Variables with Chaotic Behaviour	171
<i>Francis P. Russell, Peter D. Düben, Xinyu Niu, Wayne Luk, and T.N. Palmer</i>	
Fast and Flexible Conversion of Geohash Codes to and from Latitude/Longitude Coordinates	179
<i>Roger Moussalli, Mudhakar Srivatsa, and Sameh Asaad</i>	
SSketch: An Automated Framework for Streaming Sketch-Based Analysis of Big Data on FPGA	187
<i>Bita Darvish Rouhani, Ebrahim M. Songhori, Azalia Mirhoseini, and Farinaz Koushanfar</i>	
An Open-Source Tool Flow for the Composition of Reconfigurable Hardware Thread Pool Architectures	195
<i>Jens Korinth, David de la Chevallerie, and Andreas Koch</i>	
A Novel High-Throughput Acceleration Engine for Read Alignment	199
<i>Yu-Ting Chen, Jason Cong, Jie Lei, and Peng Wei</i>	
A Parallel and Pipelined Architecture for Accelerating Fingerprint Computation in High Throughput Data Storages	203
<i>Dongyang Li, Qing Yang, Qingbo Wang, Cyril Guyot, Ashwin Narasimha, Dejan Vucinic, and Zvonimir Bandic</i>	

Implementation I

Modular SRAM-Based Binary Content-Addressable Memories	207
<i>Ameer M.S. Abdelhadi and Guy G.F. Lemieux</i>	
A Low-Latency, Low-Area Hardware Oblivious RAM Controller	215
<i>Christopher W. Fletcher, Ling Ren, Albert Kwon, Marten van Dijk, Emil Stefanov, Dimitrios Serpanos, and Srinivas Devadas</i>	
Measuring the Accuracy of Minimum Width Transistor Area in Estimating FPGA Layout Area	223
<i>Farheen Fatima Khan and Andy Ye</i>	
Offset Pipelined Scheduling: Conditional Branching for CGRAs	227
<i>Aaron Wood and Scott Hauck</i>	

Poster Session IV

A Highly-Efficient, Adaptive and Fault-Tolerant SoC Implementation of a Fourier Transform Spectrometer Data Processing	231
<i>Xabier Iturbe, Didier Keymeulen, Patrick Yiu, Dan Berisford, Kevin Hand, Robert Carlson, and Emre Ozer</i>	
FPGA Design for PCANet Deep Learning Network	232
<i>Yuteng Zhou, Wei Wang, and Xinning Huang</i>	
Functional Locking Modules for Design Protection of Intellectual Property Cores	233
<i>Brice Colombier and Lilian Bossuet</i>	
Virtual Channel and Switch Allocation for Low Latency Network-on-Chip Routers	234
<i>Alireza Monemi, Chia Yee Ooi, and Muhammad Nadzir Marsono</i>	
Early Experiences with OpenCL on FPGAs: Convolution Case Study	235
<i>C. Rodriguez-Donate, G. Botella, C. Garcia, E. Cabal-Yepez, and M. Prieto-Matias</i>	

Implementation II

Optimizing Residue Number Reverse Converters through Bitwise Arithmetic on FPGAs	236
<i>Bangtian Liu, Haohuan Fu, Lin Gan, Wenlai Zhao, and Guangwen Yang</i>	
A Reconfigurable Multiclass Support Vector Machine Architecture for Real-Time Embedded Systems Classification	244
<i>Jason Kane, Robert Hernandez, and Qing Yang</i>	
Floorplanning for Partially-Reconfigurable FPGAs via Feasible Placements Detection	252
<i>Marco Rabozzi, Antonio Miele, and Marco D. Santambrogio</i>	
Designing Partial Bitstreams for Multiple Xilinx FPGA Partitions	256
<i>Victor M. Gonçalves Martins, João Gabriel Reis, Horácio C.C. Neto, and Eduardo Augusto Bezerra</i>	

Author Index	260
---------------------	-------	-----