2015 20th International Mixed-Signal Testing Workshop

(IMSTW 2015)

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2015 20th International Mixed-Signals Testing Workshop (IMSTW)

Paris, France, June 24th– 26th, 2015

Technical Program

JUNE 24, 2015

8:30 – 8:55	**OPENING SESSION**
	Welcome message Haralampos-G. STRATIGOPOULOS, *TIMA Laboratory (CNRS – Grenoble INP – UJF) – France* **Program Introduction** Gildas LEGER, *IMSE-CNM-CSIC – Spain* Carsten WEGENER, *Dialog Semiconductor – Germany*
8:55 – 9:40	**KEYNOTE TALK 1** Moderator: Carsten WEGENER, *Dialog Semiconductor – Germany*
	Two decades of IMSTW – looking back and one decade ahead Gordon W. ROBERTS, *McGill Univ. – Canada*
9:40 – 10:30	**SESSION 1** Moderator: Yolanda LECHUGA, *ETSIIT Universidad de Cantabria - Spain*
	Using IJTAG Digital Islands in Analog Circuits to Perform Trim and Test Functions Hans Martin VON STAUDT and Alexios SPYRONASIOS, *Dialog Semiconductor – Germany* **Digitally-Compatible Ring Oscillator Frequency Driven Tuning of CN-TFT Amplifiers: Performance Compensation Under Statistical and Morphological Variations** Suvadeep BANERJEE[*], Man Prakash GUPTA[*], Aritra BANERJEE[‡], Satish KUMAR[*], and Abhijit CHATTERJEE[*], [*]*Georgia Institute of Technology – USA,* [‡]*Texas Instruments – USA*
10:30 – 11:00	Coffee break

11:00 – 13:00	**SPECIAL SESSION 1: ANALOG AND MIXED-SIGNAL CAD AND VERIFICATION TECHNIQUES** Moderator: Krishnendu CHAKRABARTY, *Duke University – USA*
	Verification and validation of AMS Systems: towards higher coverage Christoph GRIMM, *TU Kaiserslautern – Germany* **How to Benefit from Formal Verification for Analog Transistor Level Circuits** Lars HEDRICH, *Univ. Frankfurt – Germany* **Automated Triangular Wave Generator Design with Process Corners Compensation** Marie-Minerve LOUERAT, *LIP6 Laboratory (CNRS – Univ. Pierre et Marie Curie) – France* **A simulation methodology for the reliability-aware design of analog circuits** Rafael CASTRO, *IMSE-CNM-CSIC, Univ. of Sevilla – Spain*
13:00 – 14:00	Lunch break
14:00 – 15:15	**SESSION 2** Moderator: Salvador MIR, *TIMA Laboratory (CNRS – Grenoble INP – UJF) – France*
	ACR BER Correlation to ATE for a COFDM VHF RX Peter SARSON, *ams AG – Austria* **Considerations For Light Sources For Semiconductor Test** Martin BUCK, *ams AG – United Kingdom* **Sensitivity Calibration and Test of a 3D Hall integrated Sensor device with an external magnetic field source on a new ATE concept** Luca GIORGI, *ams AG – Italy*
15:15 – 16:30	**SESSION 3** Moderator: Emmanuel SIMEU, *TIMA Laboratory (CNRS – Grenoble INP – UJF) – France*
	Efficient contact screening of compact NVMs designed for high reliability automotive applications Friedrich Peter LEISENBERGER and Gregor SCHATZBERGER, *ams AG – Austria* **Buck Converter Modeling in SystemVerilog for Verification and Virtual Test Applications** Elvis SHERA and Carsten WEGENER, *Dialog Semiconductor – Germany*

	Structure Preserving Modeling for Safety Critical Systems Gurkan UYGUR and Sebastian M. SATTLER, *Friedrich-Alexander-University Erlangen-Nuremberg – Germany*
16:30 – 17:00	Coffee break
17:00 – 18:30	**PANEL**
	Am I willing to share my benchmark circuits, algorithms and databases? How can I convince myself, my colleagues and industrial partners of the quality of my test solutions? Moderator: Gildas LEGER, *IMSE-CNM-CSIC – Spain* Panelists: Jacob A. ABRAHAM, *Univ. of Texas at Austin – USA* Abhijit CHATTERJEE, *Georgia Institute of Technology – USA* Bozena KAMINSKA, *Simon Fraser Univ. – Canada* Sebastian M. SATTLER, *Friedrich-Alexander-University Erlangen-Nuremberg – Germany* Stephen SUNTER, *Mentor Graphics – Canada* Salvador MIR, *TIMA Laboratory (CNRS – Grenoble INP – UJF) – France*
18:30 – 21:00	Welcome reception

JUNE 25, 2015

8:30 – 9:15	**KEYNOTE TALK 2** Moderator: Gildas LEGER, *IMSE-CNM-CSIC – Spain*
	The Growing Importance of Mixed-Signal in Mobile Hand-held Devices Mark BENNETT, *Dialog Semiconductor – UK*
9:15 – 10:30	**SESSION 4** Moderator: Sebastian SATTLER, *Friedrich-Alexander-University Erlangen-Nuremberg – Germany*
	Experiences with an industrial analog fault simulator and engineering intuition Stephen SUNTER, *Mentor Graphics – Canada* **An Approach to Generate Test Signals for Analog Circuits – A Control-Theoretic Perspective** Wolfgang VERMEIREN, Fabian HOPSCH, Roland JANCKE, *Fraunhofer IIS/EAS Dresden – Germany*

	Modeling static analog behavior for determining mixed-signal test coverage using digital tools Carsten WEGENER, *Dialog Semiconductor – Germany*
10:30 – 11:00	Coffee break
11:00 – 13:00	**SPECIAL SESSION 2: INDUSTRY ELEVATOR TALKS** Moderator: Florence AZAIS, *LIRMM, CNRS/Univ. Montpellier – France*
	Internet Of Thing production test challenges François LEFEVRE, *NXP Semiconductors – France* **What is the path to Analogue SCAN?** Peter SARSON, *ams AG – Austria* **Two-point self-trim (and self-test) of offset-gain pairs** Hans-Martin VON STAUDT, *Dialog Semiconductor – Germany* **The Need for Speed! How and When Can We Make Tbps Data Rates Mainstream?** Bill EKLOW, *Cisco – USA* **Design and test requirements of mixed signal automotive circuits towards sub-ppm level** Ronny VANHOOREN, *ON Semiconductor – Belgium* **Test coverage in the analog domain regarding the metal open and shorts** Dieter HAERLE*, Infineon – Austria* **In schematic netlists, how should we represent manufacturing defects for analog fault simulation?** Stephen SUNTER, *Mentor Graphics – Canada*
13:00 – 14:00	Lunch break
14:00 – 15:15	**SESSION 5** Moderator: José MACHADO DA SILVA, *Univ. of Porto – Portugal*
	Reliability of SAR ADCs and Associated Embedded Instrument Detection Jinbo WAN and HANS KERKHOFF, *Univ. of Twente – The Netherlands* **Determination of the Aging Offset Voltage of AMR Sensors Based on Accelerated Degradation Test** Andreina ZAMBRANO and Hans KEKHOFF, *Univ. of Twente – The Netherlands*

	Impact of Stress Acceleration on Mixed-Signal Gate Oxide Lifetime Kexin YANG and Linda MILOR, *Georgia Institute of Technology – USA*
15:15 – 16:30	**SESSION 6** Moderator: Linda MILOR, *Georgia Tech. - USA*
	A generic methodology for building efficient prediction models in the context of alternate testing Syhem LARGUECH, Florence AZAIS, Serge BERNARD, Mariane COMPTE, Vincent KERZEHO and Michel RENOVELL, *LIRMM, CNRS/Univ. Montpellier – France* **A fuzzy logic approach for highly dependable medical wearable systems** Cristina C. OLIVEIRA and José MACHADO DA SILVA, *Univ. of Porto – Portugal* **Digital on-chip measurement circuit for built-in phase noise testing** Stephane DAVID-GRIGNOT[*], Florence AZAIS[*], Laurent LATORRE[*] and François LEFEVRE[ǂ], [*]*LIRMM, CNRS/Univ. of Montpellier – France,* [ǂ]*NXP Semiconductors – France*
16:30 – 19:30	Free time
19:30 – 23:00	Social event

JUNE 26, 2015

9:15 – 10:30	**SESSION 7** Moderator: Hans-Martin VON STAUDT, *Dialog Semiconductor – Germany*
	Design of an on-chip stepwise ramp generator for ADC static BIST applications Guillaume RENAU, Manuel BARRAGAN and Salvador MIR, *TIMA Laboratory (CNRS – Grenoble INP – UJF) – France* **Evaluation of Harmonic Cancellation Techniques for Sinusoidal Signal Generation in Mixed-Signal BIST** Hani MALLOUG, Manuel BARRAGAN and Salvador MIR, *TIMA Laboratory (CNRS – Grenoble INP – UJF) – France* **Oscillation-based Approach Applied to a Low-Power Analog Front-End for an Implantable Cardiac Device** Jose Angel MIGUEL, David RIVAS, Yolanda LECHUGA, Miguel Angel ALLENDE and Mar MARTINEZ, *University of Cantabria – Spain*
10:30 – 11:00	Coffee break

11:00 – 13:00	**SPECIAL SESSION 3: FP7 AUTOMICS PROJECT** Moderator: Marie-Minerve LOUERAT, *Laboratoire LIP6 – France*
	AUTOMICS: Pragmatic solution for parasitic-immune design of electronics ICs for automotive Yasser MOURSY[*], Hao ZOU[*], Pietro BUCCELLA[†], Camillo STEFANUCCI[†], Ramy ISKANDER[*], Maher KAYAL[†], Jean-Michel SALLESE[†], Marie-Minerve LOUERAT[*], Jean-Paul CHAPUT[*], Veljko TOMAMAEVIC[‡], Sonia BEN-DHIA[‡], Alexandre BOYER[‡], Bruno GUEGAN[§], Vanni POLETTO[¶], Andrea ROGGERO[¶], Tiziana CAVIONI[¶], Enrico NOVARINI[¶], Ehrenfried SEEBACHER[$$], Alexander STEINMAR[$$],Pierre TISSERAND[**], Dieu-My TON[**],Thierry BOUSQUET[††] and Thomas GNEITING[‡‡], *[*]Université Pierre et Marie Curie, Laboratoire LIP6 – France*, *[†]Ecole Polytechnique Fédérale de Lausanne – Switzerland*, *[‡]INSA de Toulouse, CNRS LAAS – France, [§]STMicroelectronics – France*, *[¶]STMicroelectronics – Italy*, *[$$] ams AG – Austria*, *[**]Valeo – France, [††]Continental Automotive – France, [‡‡]AdMOS – Germany* **Truck Alternator Controlled by a System On Chip: Development of High Voltage, High Temperature, High Current Technology; Discussion on Design Bricks and Analysis of Parasitics Components using AUTOMICS Tool** *Pierre TISSERAND and Dieu-My TON, Valeo – France* **Substrate Modeling to Improve Reliability of High Voltage Technologies** Camillo STEFANUCCI[*], Pietro BUCCELLA[*], Yasser MOURSY[†], Hao ZOU[†], Ramy ISKANDER[†], Maher KAYAL[*] and Jean Michel SALLESE[*], *[*]Ecole Polytechnique Fédérale de Lausanne – Switzerland, [†] Université´ Pierre et Marie Curie, Laboratoire LIP6 – France* **An Integrated CAD Solution of Parasitic Substrate Modeling for industrial IC design** Hao ZOU[†], Yasser MOURSY[†], Ramy ISKANDER[†], Jean-Paul CHAPUT[†], Marie-Minerve LOUERAT[†], Camillo STEFANUCCI[*], Pietro BUCCELLA[*], Maher KAYAL[*] , Jean Michel SALLESE[*], Heidrun ALIUS[‡‡], Thomas GNEITING[‡‡], Alexander STEINMAR[**] and Ehrenfried SEEBACHER[**], *[†] Université´ Pierre et Marie Curie, Laboratoire LIP6 – France, [*]Ecole Polytechnique Fédérale de Lausanne – Switzerland, [‡‡]AdMOS – Germany, [**] ams AG – Austria* **Smart Power Mixed ICs parasitic bipolar coupling issues analysis with a dedicated On-Chip sensor** VeljkoTOMASEVIC[‡], Alexander STEINMAR[**], Alexandre BOYER[‡], Sonia BEN DHIA[‡], Ehrenfried SEEBACHER[**], Bernhard WEISS[**], Peter RUST[**], *[‡] INSA de Toulouse, CNRS LAAS – France, [**] ams AG – Austria*
13:00 – 14:00	Lunch break

14:00 – 15:15	**SESSION 8** Moderator: Wolfgang VERMEIREN, *Fraunhofer IIS/EAS Dresden – Germany*
	Real-time adaptive test algorithm including test escape estimation method Christian STREITWIESER, *ams AG – Austria* **A Jitter Injection Signal Generation and Extraction System For Embedded Test Of High-Speed Data I/O** Yan LI, Steven BIELBY, Azhar CHOWDHURY and Gordon W. ROBERTS, *McGill Univ. – Canada* **Timing Measurement BOST With Multi-bit Delta-Sigma TDC** Takeshi CHUJO[*], Daiki Daiki HIRABAYASHI[*], Takuya ARAFUNE[*], Shohei SHIBUYA[*], Shu SASAKI[*], Haruo KOBAYASHI[*], Masanobu TSUJI[ǂ], Ryoji SHIOTA[ǂ], Masafumi WATANABE[ǂ], Noriaki DOBASHI[ǂ], Sadayoshi UMEDA[ǂ], Hideyuki NAKAMURA[ǂ] and Koshi SATO[≠], [*]Gunma Univ. – Japan, [ǂ]Semiconductor Technology Academic Research Center – Japan, [≠]Hikari Science – Japan
15:15 – 15:30	**CLOSING REMARKS**