

# **2015 IEEE 21st International On-Line Testing Symposium (IOLTS 2015)**

**Halkidiki, Greece  
6-8 July 2015**



**IEEE Catalog Number: CFP15OLT-POD  
ISBN: 978-1-4673-7906-9**

## Technical Papers

<b>Session 1</b>	<b>Reliability Evaluation</b>
<b>Date/Time</b>	Monday July 6, 2015 / 10:35 – 11:35
<b>Moderator</b>	S.Hellebrand, <i>U Paderborn</i>

- **Efficient Multilevel Formal Analysis and Estimation of Design Vulnerability to Single Event Transients....1**  
*G. B. Hamad, O. A. Mohamed and Y. Savaria*
- **Bayesian Network Early Reliability Evaluation Analysis for both permanent and transient faults....7**  
*A. Vallero, A. Savino, S. Tselonis, N. Foutris, M. Kaliorakis, G. Politano, D. Gizopoulos, S. Di Carlo*
- **Laser Fault Injection into SRAM cells: Picosecond versus Nanosecond pulses....13**  
*M. Lacruche, N. Borrel, C. Champeix, C. Roscian, A. Sarafianos, Jean-B. Rigaud, Jean-M. Dutertre and E. Kussener*

<b>Session 2</b>	<b>Posters</b>
<b>Date/Time</b>	Monday July 6, 2015 / 11:35 – 13:00

- **A Call for Cross-Layer and Cross-Domain Reliability Analysis and Management....19**  
*D. Alexandrescu, A. Evans, E. Costenaro and M. Glorieux*
- **An Accurate Soft Error Propagation Analysis Technique Considering Temporal Masking Disablement....23**  
*Y. Kimi, G. Matsukawa, S. Yoshida, S. Izumi, H. Kawaguchi and M. Yoshimoto*
- **An Hybrid Architecture for Consolidating Mixed Criticality Applications on Multicore Systems....26**  
*S. Avramenko, S. Esposito, M. Violante, M. Sozzi, M. Traversone, M. Binello and M. Terrone*
- **Fault Modeling and Testing of Through Silicon Via Interconnections....30**  
*V. Gerakis, L. Katselas and A. Hatzopoulos*
- **Identifying Aging-Aware Representative Paths in Processors....32**  
*C. Sandionigi and O. Heron*
- **On the Maximization of the Sustained Switching Activity in a Processor....34**  
*R. Cantoro, M. Sonza Reorda, A. Rohani and H. G. Kerkhoff*
- **Optimization of SEU Emulation on SRAM FPGAs Based on Sensitiveness Analysis....36**  
*A. Souari, C. Thibeault, Y. Blaqui  re and R. Velasco*
- **Power Analysis Attacks on ARX: An Application to Salsa20....40**  
*B. Mazumdar, S. Subidh Ali and O. Sinanoglu*
- **Simplification of Fully Delay Testable Combinational Circuits....44**  
*A. Matrosova, E. Mitrofanov and T. Shah*
- **Soft Error Immune Latch Under SEU Related Double-Node Charge Collection....46**  
*K. Katsarou and Y. Tsiatouhas*
- **Towards Trojan Circuit Detection with Maximum State Transition Exploration....50**  
*J. Lenox and S. Tragoudas*

<b>Session 3</b>	<b>Reliable Filters and Sensors</b>
<b>Date/Time</b>	Monday July 6, 2015 / 14:00 – 15:00
<b>Moderator</b>	Z. Stamenkovic, <i>IHP</i>

- **Concurrent Error Detection in Nonlinear Digital Filters Using Checksum Linearization and Residue Prediction....53**  
*S. Banerjee, Md I. Momtaz and A. Chatterjee*

 **Adaptive Healing Procedure for Lifetime Improvement in Wireless Sensor Networks....59**

*D. T. Tchakonte, E. Simeu and M. Tchuente*

 **Fault-Tolerant System for Catastrophic Faults in AMR Sensors....65**

*A. Zambrano and H. G. Kerkhoff*

Session 4	Fault Tolerant On-Chip Networks
Date/Time	Monday July 6, 2015 / 15:20 – 16:20
Moderator	A. Grasset, Thales

 **MUGEN: A High-Performance Fault-Tolerant Routing Algorithm for Unreliable Networks-on-Chip....71**

*A. Charif, N.-E. Zergainoh and M. Nicolaidis*

 **Timing-Resilient Network-on-Chip Architectures....77**

*A. Panteloukas, A. Psarras, C. Nicopoulos and G. Dimitrakopoulos*

 **Defect Diagnosis Algorithms for a Field Programmable Interconnect Network Embedded in a Very Large Area Integrated Circuit....83**

*G. Sion, Y. Blaqui  re and Y. Savaria*

Session 5	Fault Tolerance
Date/Time	Monday July 6, 2015 / 16:50 – 17:50
Moderator	G. Georgakos, Infineon

 **Design Space Exploration and Optimization of a Hybrid Fault-Tolerant Architecture....89**

*I. Wali, A. Virazel, A. Bosio, P. Girard and M. Sonza Reorda*

 **Efficient On-Line Fault-Tolerance for the Preconditioned Conjugate Gradient Method....95**

*A. Sch  ll, C. Braun, M. A. Kochte and H.-J. Wunderlich*

 **Mitigation Of Fail-Stop Failures In Integer Matrix Products Via Numerical Packing....101**

*I. Anarado and Y. Andreopoulos*

Special Session 1	The Future of Fault Tolerant Computing
Date/Time	Monday July 6, 2015 / 18:00 – 19:30
Organizers/Moderators	D. Gizopoulos, U Athens and D. Alexandrescu, iRoC

 **The Future of Fault Tolerant Computing....108**

*J. Abraham, R. Iyer, D. Gizopoulos, D. Alexandrescu and Y. Zorian*

Session 6	Error Tolerance and Prediction
Date/Time	Tuesday July 7, 2015 / 09:00 – 10:00
Moderator	A. Paschalidis, U Athens

 **Toward Efficient Check-Pointing and Rollback Under On-Demand SBST in Chip Multi-Processors....110**

*M. A. Skitsas, C. A. Nicopoulos, M. K. Michael*

 **Workload Characterization and Prediction: A Pathway to Reliable Multi-core Systems....116**

*M. Zaman, A. A. and Y. Makris*

 **Failure Mitigation in Linear, Sesquilinear and Bijective Operations On Integer Data Streams Via Numerical Entanglement....122**

*M. A. Anam and Y. Andreopoulos*

<b>Special Session 2</b>	<b>Self-Awareness for Resilient System Design</b>
<b>Date/Time</b>	Tuesday July 7, 2015 / 10:30 – 11:30
<b>Organizer/Moderator</b>	M. Tahoori, <i>U Karlsruhe</i>

- S2 **Self-Awareness and Self-Learning for Resiliency in Real-Time Systems....128**  
*M. B. Tahoori, A. Chatterjee, K. Chakrabarty, A. Koneru, A. Vijayan and D. Banerjee*

<b>Session 7</b>	<b>Application-Specific Dependability</b>
<b>Date/Time</b>	Tuesday July 7, 2015 / 12:00 – 13:00
<b>Moderator</b>	M. Maniatakos, NYUAD

- ⌚ **Filtering-Based Error-Tolerability Evaluation of Image Processing Circuits....132**  
*Tong-Y. Hsieh and Yi-H. Peng*
- ⌚ **A Single Chip Dependable and Adaptable Payload Data Processing Unit....138**  
*N. Kranitis, A. Tsigkanos, G. Theodorou, I. Sideris and A. Paschalidis*
- ⌚ **Characterizing Fault Propagation in Safety-Critical Processor Designs....144**  
*J. Espinosa, C. Hernandez and J. Abella*

<b>Session 8</b>	<b>Secure and Reliable Design</b>
<b>Date/Time</b>	Wednesday July 8, 2015 / 09:00 – 10:00
<b>Moderator</b>	C. Lopez Ongil, <i>U Carlos III de Madrid</i>

- ⌚ **Experimental Validation of a Bulk Built-In Current Sensor for Detecting Laser-Induced Currents....150**  
*C. Champeix, N. Borrel, Jean-M. Dutertre, B. Robisson, M. Lisart and A. Sarafianos*
- ⌚ **OPUF: Obfuscation Logic Based Physical Unclonable Function....156**  
*J. Ye, Y. Hu and X. Li*
- ⌚ **Flip-Flop SEU Reduction through Minimization of the Temporal Vulnerability Factor (TVF)....162**  
*A. Evans, E. Costenaro and A. Bramnik*

<b>Special Session 3</b>	<b>DFx Techniques</b>
<b>Date/Time</b>	Monday July 6, 2015 / 10:30 – 11:30
<b>Organizer/Moderator</b>	M. Nicolaidis, <i>TIMA</i>

- ⌚ **An Effective Embedded Test & Diagnosis Solution for External Memories....168**  
*G. Harutyunyan and Y. Zorian*
- ⌚ **Low-Power Memory Repair for High Defect Densities....171**  
*P. Papavramidou and M. Nicolaidis*
- ⌚ **Reliability/Yield Trade-Off in Mitigating ``No Trouble Found'' Field Returns....174**  
*A. Haggag, N. Sumikawa and A. Shaukat*

<b>Session 9</b>	<b>Failure Prediction and Diagnosis</b>
<b>Date/Time</b>	Wednesday July 8, 2015 / 12:00 – 13:00
<b>Moderator</b>	E. Ibe, <i>Hitachi</i>

- ⌚ **Efficient Observation Point Selection for Aging Monitoring....176**  
*C. Liu, M. A. Kochte and H.-J. Wunderlich*
- ⌚ **Mining Simulation Metrics for Failure Triage in Regression Testing....182**  
*Z. Poulos and A. Veneris*
- ⌚ **Real-Time On-Chip Supply Voltage Sensor and Its Application to Trace-Based Timing Error Localization....188**  
*M. Ueno, M. Hashimoto and T. Onoye*

<b>Session 10</b>	<b>Memory Reliability</b>
<b>Date/Time</b>	Wednesday July 8, 2015 / 14:00 – 15:00
<b>Moderator</b>	R.Canal, <i>UPC</i>

- ⌚ **BTI and Leakage Aware Dynamic Voltage Scaling for Reliable Low Power Cache Memories....194**  
*D. Rossi, V. Tenentes, S. Khursheed and B. M. Al-Hashimi*
- ⌚ **New Byte Error Correcting Codes with Simple Decoding for Reliable Cache Design....200**  
*L. Bu, M. Karpovsky and Z. Wang*
- ⌚ **Low Leakage Radiation Tolerant CAM/TCAM Cell....206**  
*N. Eftaxiopoulos, N. Axelos and K. Pekmestzi*