

2015 IEEE 26th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2015)

**Toronto, Ontario, Canada
27-29 July 2015**



**IEEE Catalog Number: CFP15063-POD
ISBN: 978-1-4799-1926-0**

TABLE OF CONTENTS

Session M1 : Architecture and Technologies 1

REGULAR PAPERS

Automatic Design of Domain-Specific Instructions for Low-Power Processors	1
<i>Cecilia González-Álvarez, Jennifer B. Sartor, Carlos Álvarez, Daniel Jiménez-González, Lieven Eeckhout</i>	
Custom FPGA-Based Soft-Processors for Sparse Graph Acceleration.....	9
<i>Nachiket Kapre</i>	
A Soft-Core Processor Array for Relational Operators	17
<i>Raphael Polig, Heiner Giefers, Walter Stechele</i>	

SHORT PAPERS

Atomic Stream Computation Unit Based on Micro-Thread Level Parallelism	25
<i>Nasim Farahini, Ahmed Hemani</i>	
Timing Speculation-Aware Instruction Set Extension for Resource-Constrained Embedded Systems	30
<i>Tanvir Ahmed, Yuko Hara-Azumi</i>	

Session M2 : Application Acceleration 1

REGULAR PAPERS

A GPU-Based Correlator X-Engine Implemented on the CHIME Pathfinder.....	35
<i>Nolan Denman, Mandana Amiri, Kevin Bandura, Liam Connor, Matt Dobbs, Mateus Fandino, Mark Halpern, Adam D. Hincks, Gary Hinshaw, Carolin Höfer, Peter Klages, Kiyoshi Masui, Juan Mena Parra, Laura Newburgh, Andre Recnik, J. Richard Shaw, Kris Sigurdson, Kendrick Smith, Keith Vanderlinde</i>	
Power and Performance Trade-Offs for Space Time Adaptive Processing	41
<i>Nitin A. Gawande, Joseph B. Manzano, Antonino Tumeo, Nathan R. Tallent, Darren J. Kerbyson, Adolfy Hoisie</i>	
Accelerating Persistent Scatterer Pixel Selection for InSAR Processing.....	49
<i>Tahsin Reza, Aaron Zimmer, Parwant Ghuman, Tanuj Kr. Aasawat, Matei Ripeanu</i>	

SHORT PAPER

An Efficient Real-Time Data Pipeline for the CHIME Pathfinder Radio Telescope X-Engine	57
<i>Andre Recnik, Kevin Bandura, Nolan Denman, Adam D. Hincks, Gary Hinshaw, Peter Klages, Ue-Li Pen, Keith Vanderlinde</i>	

Poster Session 1

An IEEE 754 Double-Precision Floating-Point Multiplier for Denormalized and Normalized Floating-Point Numbers	62
<i>Ross Thompson, James E. Stine</i>	
Dual-Rail Active Protection System Against Side-Channel Analysis in FPGAs.....	64
<i>Wei He, Dirmanto Jap</i>	
Does Arithmetic Logic Dominate Data Movement? A Systematic Comparison of Energy-Efficiency for FFT Accelerators.....	66
<i>Tung Thanh-Hoang, Amirali Shambayati, Henry Hoffmann, Andrew A. Chien</i>	
An FPGA Implementation of a Restricted Boltzmann Machine Classifier Using Stochastic Bit Streams.....	68
<i>Bingzhe Li, M. Hassan Najafi, David J. Lilja</i>	
Application-Set Driven Exploration for Custom Processor Architectures.....	70
<i>Mehmet Ali Arslan, Flavius Gruian, Krzysztof Kuchcinski</i>	
Speeding up Graph-Based SLAM Algorithm: A GPU-Based Heterogeneous Architecture Study.....	72
<i>Abdelhamid Dine, Abdelhafid Elouardi, Bastien Vincke, Samir Bouaziz</i>	

Session M3 : Arithmetic

REGULAR PAPERS

Range Reduction Based on Pythagorean Triples for Trigonometric Function Evaluation	74
<i>Hugues de Lassus Saint-Geniès, David Defour, Guillaume Revy</i>	
LightSpMV: Faster CSR-Based Sparse Matrix-Vector Multiplication on CUDA-Enabled GPUs.....	82
<i>Yongchao Liu, Bertil Schmidt</i>	
GPU-Based Multifrontal Optimizing Method in Sparse Cholesky Factorization.....	90
<i>Ran Zheng, Wei Wang, Hai Jin, Song Wu, Yong Chen, Han Jiang</i>	

Session T1 : Architecture and Technologies 2

REGULAR PAPER

A Metamorphotic Network-on-Chip for Various Types of Parallel Applications.....	98
<i>Seiichi Tade, Hiroki Matsutani, Hideharu Amano, Michihiro Koibuchi</i>	

SHORT PAPERS

Dynamic Pipeline-Partitioned Video Decoding on Symmetric Stream Multiprocessors	106
<i>Ming-Ju Wu, Yan-Ting Chen, Chun-Jen Tsai</i>	
Stochastic Circuit Design and Performance Evaluation of Vector Quantization.....	111
<i>Ran Wang, Jie Han, Bruce Cockburn, Duncan Elliott</i>	
Mixed-Signal Implementation of Differential Decoding Using Binary Message Passing Algorithms.....	116
<i>Glenn Cowan, Kevin Cusson, Warren J. Gross</i>	

Session T2 : Crypto/Security

REGULAR PAPERS

Hardware Acceleration of Private Information Retrieval Protocols Using GPUs	120
<i>Mihai Maruseac, Gabriel Ghinita, Ming Ouyang, Razvan Rughinis</i>	
Accelerating Bootstrapping in FHEW Using GPUs	128
<i>Moon Sung Lee, Yongje Lee, Jung Hee Cheon, Yunheung Paek</i>	
Multi-Task Support for Security-Enabled Embedded Processors	136
<i>Tedy Thomas, Arman Pouraghily, Kekai Hu, Russell Tessier, Tilman Wolf</i>	

SHORT PAPERS

Towards Secure Cryptographic Software Implementation Against Side-Channel Power Analysis Attacks.....	144
<i>Pei Luo, Liwei Zhang, Yunsi Fei, A. Adam Ding</i>	
Programmable RNS Lattice-Based Parallel Cryptographic Decryption	149
<i>Paulo Martins, Leonel Sousa, Julien Eynard, Jean-Claude Bajard</i>	

Poster Session 2

Balance Power Leakage to Fight Against Side-Channel Analysis at Gate Level in FPGAs	154
<i>Xin Fang, Pei Luo, Yunsi Fei, Miriam Leeser</i>	
How Can Garbage Collection be Energy Efficient by Dynamic Offloading?	156
<i>Jie Tang, Chen Liu, Jean-Luc Gaudiot</i>	
Automatic Frame Rate-Based DVFS of Game.....	158
<i>Zhinan Cheng, Xi Li, Beilei Sun, Ce Gao, Jiachen Song</i>	

MultiExplorer: A Tool Set for MultiCore System-on-Chip Design Exploration	160
<i>Rodrigo Devigo, Liana Duenha, Rodolfo Azevedo, Ricardo Santos</i>	
Noxim: An Open, Extensible and Cycle-Accurate Network on Chip Simulator	162
<i>Vincenzo Catania, Andrea Mineo, Salvatore Monteleone, Maurizio Palesi, Davide Patti</i>	
GPU Kernels for High-Speed 4-Bit Astrophysical Data Processing.....	164
<i>Peter Klages, Kevin Bandura, Nolan Denman, Andre Recnik, Jonathan Sievers, Keith Vanderlinde</i>	

Session T3 : Tools and Design Methodologies

REGULAR PAPERS

Loop Coarsening in C-Based High-Level Synthesis	166
<i>Moritz Schmid, Oliver Reiche, Frank Hannig, Jürgen Teich</i>	
An Interpolation-Based Approach to Multi-Parameter Performance Modeling for Heterogeneous Systems	174
<i>Dylan Rudolph, Greg Stitt</i>	
Mixed-Length SIMD Code Generation for VLIW Architectures with Multiple Native Vector-Widths	181
<i>Erkan Diken, Martin J. O'Riordan, Roel Jordans, Lech Jozwiak, Henk Corporaal, David Moloney</i>	

SHORT PAPER

Comparative Analysis of OpenCL vs. HDL with Image-Processing Kernels on Stratix-V FPGA.....	189
<i>Kenneth Hill, Stefan Craciun, Alan George, Herman Lam</i>	

Session W1 : Fault Tolerance

REGULAR PAPERS

On-Demand Fault-Tolerant Loop Processing on Massively Parallel Processor Arrays	194
<i>Alexandru Tanase, Michael Witterauf, Jürgen Teich, Frank Hannig, Vahid Lari</i>	
A Scheduling and Binding Heuristic for High-Level Synthesis of Fault-Tolerant FPGA Applications.....	202
<i>Aniruddha Shastri, Greg Stitt, Eduardo Riccio</i>	

Session W2 : Application Acceleration 2 and Power

REGULAR PAPERS

Reconfigurable Acceleration of Fitness Evaluation in Trading Strategies.....	210
<i>Andreea Ingrid Funie, Paul Grigoras, Pavel Burovskiy, Wayne Luk, Mark Salmon</i>	
An Efficient Architecture Solution for Low-Power Real-Time Background Subtraction	218
<i>Hamed Tabkhi, Majid Sabbagh, Gunar Schirner</i>	
Large-Scale Packet Classification on FPGA	226
<i>Shijie Zhou, Yun R. Qu, Viktor K. Prasanna</i>	

SHORT PAPERS

Efficient Implementation of Structured Long Block-Length LDPC Codes.....	234
<i>Andrew J. Wong, Saied Hemati, Warren J. Gross</i>	
Energy Optimization of Parallel k-Means Clustering Algorithm on FPGA.....	B#5
<i>Andrea Sanny, Yi-Hua E. Yang, Viktor K. Prasanna</i>	