

2015 37th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD 2015)

**Reno, Nevada, USA
27 September – 2 October 2015**



IEEE Catalog Number: CFP15413-POD
ISBN: 978-1-4799-8895-2

TABLE OF CONTENTS

1A. ESD Protection in Advanced Technologies

Moderator: Gene Worley, Qualcomm, Inc.

1A.1 Innovative High-Density ESD Protection Device in State of the Art FDSOI UTBB Technologies... 1

Pascal Fonteneau, Yohann Solaro, David Marin-Cudraz, Charles-Alexandre Legrand, STMicroelectronics; Claire Fenouillet-Beranger, CEA-LETI MINATEC

1A.2 Design and Optimization of ESD Lateral NPN Device in 14nm FinFET SOI CMOS Technology .. 8

You Li, Rahul Mishra, Liyang Song, Robert Gauthier, IBM

1A.3 VFTLP Characteristics of ESD Protection Diodes in Advanced Bulk FinFET Technology 15

Shih-Hung Chen, Dimitri Linten, Mirko Scholz, Geert Hellings, Aaron Thean, imec; Roman Boschke, Guido Groeseneken, KU Leuven

1A.4 ESD Characterization of Diodes and ggMOS in Germanium FinFET Technologies..... 21

Roman Boschke, Guido Groeseneken, imec, Katholieke Universiteit Leuven; Geert Hellings, Dimitri Linten, Mirko Scholz, Shih-Hung Chen, Jerome Mitard, Liesbeth Witters, Nadine Collaert, Aaron Thean, imec

1B: Factory Control I

Moderator: Wolfgang Stadler, Intel Deutschland GmbH

RCJ: Development of a Perfectly Balanced Electrostatic Eliminator Utilizing an Intermittent Pulse

AC Voltage Power Supply *RCJ Invited Paper* 30

Katsuyuki Takahashi, Akira Goto, Shinichi Yamaguchi, Tomokatsu Saito, Kensuke Sakamoto, Hidemi Nagata, Shishido Electrostatic, Ltd.

1B.1 Analysis of Pulsed DC Ionizer Measurement Procedures with a CPM Using ESDA RP 3.11-2006.. 34

Lawrence Levit, LBL Scientific; William Vosteen, Monroe Electronics; Geoffrey Weil, Anodyne Research

1B.2 Manufacturing Changes Air Ionization Technology..... 38

Arnold Steinman, Electronics Workshop, Dangelmayer Associates LLC

1B.3 A Novel New Concept in Hybrid Alpha Ionization Systems 45

Lawrence Levit, LBL Scientific; Geoffrey Weil, Anodyne Research

2A: ESD Design in RF and Power Devices

Moderator: Christian Russ, Intel Mobile Communications

2A.1 An Electrostatic-Discharge-Protection Solution for Silicon-Carbide MESFET	50
T. Phulpin, D. Trémouilles, K. Isoird, P. Austin, CNRS, LAAS, Université de Toulouse; D. Tournier, Université de Lyon; P. Godignon, Universitat Autònoma de Barcelona	
2A.2 Self-ESD-Protected Transmission Line Broadband in CMOS28nm UTBB-FDSOI	57
Johan Bourgeat, Boris Heitz, Jean Jimenez, Philippe Galy, STMicroelectronics; Tekfouy Lim, Fraunhofer Research Institution	
2A.3 CDM-Reliable T-coil Techniques for High-Speed Wireline Receivers.....	64
Min-Sun Keel, Elyse Rosenbaum, University of Illinois at Urbana-Champaign	
2A.4 Robust ESD Clamp for Envelop Tracking Power Supply	74
Iqbal Chaudhry, Nathaniel Peachey, Qorvo	
2B: System Level ESD Design	
Moderator: Fabrice Caignet, LAAS/CNRS	
2B.1 Practical Methodology for Extraction of SEED Models.....	82
Collin Reiman, Nicholas Thomson, Yang Xiu, Robert Mertens, Elyse Rosenbaum, University of Illinois at Urbana-Champaign	
2B.2 ESD Induced Functional Upset in Magnetic Sensor ICs	92
Donald Dibra, Kai Esmark, Stefan Jahn, Mario Motz, Infineon Technologies	
2B.3 Secondary Discharge – A Potential Risk during System Level ESD Testing.....	99
Heinrich Wolf, Horst Gieser, Fraunhofer EMFT	
2B.4 A Passive Coupling Circuit for Injecting TLP-Like Stress Pulses into only one End of a Driver/Receiver System.....	106
Benjamin Orr, Missouri University of Science and Technology, Intel Mobile Communications; David Johnsson, Krzysztof Domanski, Harald Gossner, Intel Mobile Communications; David Pommerenke, Missouri University of Science and Technology	
3A: ESD Checking and Verification	
Moderator: Robert Gauthier, GLOBALFOUNDRIES	
3A.1 Essential – Integration of ESD Verification Methodologies.....	114
N. Trivedi, D. Alvarez, Infineon Technologies	
3A.2 Schematic-Level and Layout-Level ESD EDA Check Methodology Applied to Smart Power IC's – Initialization and Implementation.....	123

Eleonora Gevinti, Lorenzo Cerati, Leonardo Di Biccari, Giuseppe Ballarin, Antonio Andreini, Mauro Fragnoli, Antonio Bogani, STMicroelectronics

3A.3 A Comprehensive ESD Verification Flow at Transistor Level for Large SoC Designs 133
Jérôme Lescot, Patrice Dehan, Wahbi Boujarrar, STMicroelectronics; Dina Medhat, Sophie Billy, Mentor Graphics

3B: ESD Failure Case Study

Moderator: Scott Ruth, Freescale Semiconductor, Inc.

3B.1 HBM Failures Induced by ESD Cell Turn-Off and Circuit Interaction with ESD Protection..... 139
Yang Xiao, Ann Concannon, Rajkumar Sankaralingam, Texas Instruments

3B.2 Soft Fails Due to LU Stress of Virtual Power Domains 146
Krzysztof Domanski, Harald Gossner, Intel Mobile Communications

3B.3 ESD Failure Caused by Parasitic SCR in an Overvoltage Tolerant I/O 154
D. Alvarez, M. Wendel, A. Stuffer, Infineon Technologies

4A: TCAD Design and Simulation

Moderator: Vladislav Vashchenko, Maxim Integrated

4A.1 A Study of the Effect of Remote CDM Clamps in Integrated Circuits..... 163
Dolphin Abessolo-Bidzo, Theo Smedes, NXP Semiconductors; Peter C. de Jong, Synopsys, Inc.

4A.2 An Off-Chip ESD Protection for High-Speed Interfaces 171
Guido Notermans, Hans-Martin Ritter, Joachim Utzig, Steffen Holland, Zhihao Pan, Jochen Wynants, Paul Huiskamp, Wim Peters, Burkhard Laue, NXP Semiconductors

4A.3 Active Clamps with Hybrid BJT-CMOS Operation Mode 181
Vladislav Vashchenko, Blerina Aliaj, Augusto Tazzoli, Maxim Integrated Corp.; Andrei Shibkov, Angstrom Design Automation

4B: Tester and Testing Method I

Moderator: Mike Chaine, Micron Technology, Inc.

4B.1 TLP-Based Human Metal Model Stress Generator and Analysis Method of ESD Generators..... 188
Rémi Bèges, Freescale Semiconductor, Inc., CNRS, LAAS; Fabrice Caignet, Nicolas Nolhier, CNRS, LAAS, Univ. de Toulouse; Patrice Besse, Jean-Philippe Laine, Alain Salles, Freescale Semiconductor, Inc; Nicolas Mauran, Marise Bafleur, CNRS, LAAS

4B.2 ESD Protection of Open-Drain I²C using Fragile Devices in Embedded Systems..... 198

Farzan Farbiz, Muhammad Y. Ali, Raj Sankaralingam, Texas Instruments

4B.3 Using CC-TLP to get a CDM Robustness Value 205

Kai Esmark, Reinhold Gaertner, Stefan Seidl, Friedrich zur Nieden, Infineon Technologies; Heinrich Wolf, Horst Gieser, Fraunhofer EMFT

5A: 3D Chip Stacking ESD Protection

Moderator: Charles Chu, Maxim Integrated

5A.1 ESD Protection Design in Active-Lite Interposer for 2.5 and 3D Systems-in-Package..... 215

Mirko Scholz, Geert Hellings, Shih-Hung Chen, Dimitri Linten, Mikael Detalle, Cesar Roda Neve, Antonio La Manna, Geert van der Plas, Eric Beyne, imec; A. Shibkov, Angstrom Design Automation

5A.2 3D Integration ESD Protection Design and Analysis..... 225

Souvik Mitra, Ephrem Gebreselasie, You Li, Robert Gauthier, Joel Silberman, Christy Tyberg, Katsuyuki Sakuma, Thuy Tran-Quinn, Koushik Ramachandran, Matthew Angyal, IBM

5B: Factory Control II

Moderator: John Kinnear, IBM

5B.1 Multi-Physics Simulations for Triboelectric Charging of Display Panels during the Roller

Transfer Process 231

Ki-Hyuk Kim, Samsung Display, Co., Ltd., Missouri University of Science and Technology; David Pommerenke, Missouri University of Science and Technology; Yingjie Gan, Wuhan University of Technology, Missouri University of Science and Technology; Nam-Hee Goo, Seuk Whan Lee, Samsung Display, Co., Ltd.

5B.2 ESD and Disturbance Cases in Electrostatic Protective Areas 239

Pasi Tamminen, Prof. Leena Ukkonen, Prof. Lauri Sydänheimo, Tampere University of Technology; Toni Viheriäkoski, Cascade Metrology

6A: ESD Simulation and Verification

Moderator: Eleonora Gevinti, STMicroelectronics

6A.1 A Full-Chip ESD Simulation Flow 246

Steven S. Poon, Kushal Sreedhar, Chinmay Joshi, Marco Escalante, Intel Corporation

6A.2 A New Full-Chip Verification Methodology to Prevent CDM Oxide Failures..... 254

Melanie Etherton, Scott Ruth, James W. Miller, Rishabh Agarwal, Rishi Bhooshan, Freescale Semiconductor, Inc.; Maxim Ershov, Meruzhan Cadjan, Yuri Feinberg, Silicon Frontline Technology Inc.; Karthik Srinivasan, Norman Chang, Youlin Liao, ANSYS, Inc.

6A.3 Fast Circuit Simulator for Transient Analysis of CDM ESD 264

Kuo-Hsuan Meng, Elyse Rosenbaum, University of Illinois at Urbana-Champaign

6A.4 P2P and RMAP - New Software Tool for Quick and Easy Verification of Power Nets.....	274
Maxim Ershov, Meruzhan Cadjan, Yuri Feinberg, Silicon Frontline Technology; Thomas Jochum, Intersil; Scott Ruth, Melanie Etherton, Freescale Semiconductor, Inc.	

6B: Factory Control III

Moderator: Reinhold Gaertner, Infineon Technologies

6B.1 Benchmarking of Factory Level ESD Control	282
Toni Viheriäkoski, Cascade Metrology; Jari Kohtamäki, ABB Oy; Terttu Peltoniemi, Nokia; Pasi Tamminen, Microsoft	
6B.2 How Six Sigma Brought Saving and Improved Manufacturing Process by 98.9%	289
Kamil Drab, Mariusz Kwiatkowski, Philip Wasalaski, Nexteer Automotive	

6B.3 Uncertainties in Charge Measurements of ESD Risk Assessment	294
Toni Viheriäkoski, Cascade Metrology; Jari Kohtamäki, ABB Oy; Terttu Peltoniemi, Nokia; Pasi Tamminen, Microsoft	

6B.4 Probabilistic Analytical Benchmarking for ESD Manufacturing Process	302
L. H. Koh, Y. H. Goh, Everfeed Technology Pte, Ltd.; C. B. Goh, UTAC Manufacturing Services Singapore Pte, Ltd.	

7A: HV ESD Clamp Design

Moderator: Mototsugu Okushima, Renasas

7A.1 Design and Optimization on ESD Self-Protection Schemes for 700V LDMOS in High Voltage Power IC	307
Zhong Chen, Akram Salman, Guru Mathur, Gianluca Boselli, Texas Instruments, Inc.	

7A.2 Engineering of Dual-Direction SCR Cells for Component and System Level ESD, Surge, and Longer EOS Events.....	313
Augusto Tazzoli, Vladislav Vashchenko, Maxim Integrated Corp.	

7A.3 Investigation and Solution to the Early Failure of Parasitic NPN Triggered by the Adjacent PNP ESD Clamps	320
Ming-Fu Tsai, Jen-Chou Tseng, Kuo-Ji Chen, Ming-Hsiang Song, TSMC	

7A.4 Active Clamp Design for On-Chip GUN Protection	326
Andreas Rupp, Ulrich Glaser, Yiqun Cao, Infineon Technologies	

7B: System Level ESD Testing

Moderator: Harald Gossner, Intel Mobile Communications

7B.1 Air-Discharge Testing of Single Components	332
Hans-Martin Ritter, Lars Koch, Mark Schneider, Guido Notermans, NXP Semiconductors	

7B.2 The Effect of USB Ground Cable and Product Dynamic Capacitance on IEC61000-4-2 Qualification.....	339
Pasi Tamminen, Prof. Leena Ukkonen, Prof. Lauri Sydänheimo, Tampere University of Technology	

7B.3 Versatile Models and Expanded Application of the IEC 61000-4-2 Test	349
Timothy J. Maloney, Intel Corporation	
<i>This paper is co-copyrighted by Intel Corporation and the EOS/ESD Association</i>	

7B.4 S-Parameter Based Modeling of System-Level ESD Test Bed	358
Yang Xiu, Nicholas Thomson, Robert Mertens, Elyse Rosenbaum, University of Illinois at Urbana-Champaign	

8A: Tester and Testing Method II

Moderator: Heinrich Wolf, Fraunhofer EMFT

8A.1 Wear out Effects in ESD Characterization and Testing	368
T. Smedes, D. Abessolo-Bidzo, NXP Semiconductors	

8A.2 Low Impedance Contact CDM	376
Nathan Jack, Timothy J. Maloney, Intel Corporation	
<i>This paper is co-copyrighted by Intel Corporation and the EOS/ESD Association</i>	

8A.3 Practical HBM Testing with Statistical Pin Combinations	385
Wolfgang Stadler, Josef Niemesheim, Huelya Guerses, Oliver Hilbricht, Intel Mobile Communications; Andrea Boroni, Giuseppe Ballarin, STMicroelectronics; Evan Grund, Grund Technical Solutions	

8A.4 A Low-Impedance TLP Measurement System for Power Semiconductor Characterization up to 700V and 400A in the Microsecond Range	393
Gabriel Cretu, Marius Cenusu, Martin Pfost, Reutlingen University; Kevni Büyüktas, Uwe Wahl, Infineon Technologies	

9A: ESD Testing and Failure Analysis

Moderator: Peter de Jong, Synopsys Inc.

9A.1 Debug and Prediction of EOS Events Using Long Duration Transmission Line Pulse (TLP) Measurements	400
Dave Clarke, Stephen Heffernan, Analog Devices, Inc.	

9A.2 EOS Characterization Methodology Applied to Disable Feature of ESD Power Clamps	407
Jorge Loayza, STMicroelectronics, Université de Lyon; Nicolas Guitard, Blaise Jacquier, Alexandre Dray, Divya Agarwal, Vicky Batra, STMicroelectronics; Bruno Allard, Luong Viêt Phung, Université de Lyon	

9A.3 Source of Miscorrelation of Product Level HBM to TLP Test Results	416
Manjunatha Prabhu, Jian-Hsing Lee, Mahadeva Iyer Natarajan, Vasantha Kumar, Tsung-Che Tsai, Li Zhiqing, Dominic Thurmer, GLOBALFOUNDRIES	

Workshops

Workshops Chair – James Miller, Freescale Semiconductor, Inc.

Workshop Session A

A1. Strategies to Address Latch-up Test Program Complexity in Advanced Mixed Signal ICs	
Moderators: Marty Johnson, Texas Instruments; Scott Ruth, Freescale Semiconductor, Inc.	423
A2. Best Practices for ESD Robust SoC Integration of Commercial IP	
Moderators: Fabrice Blanc, ARM; Peter de Jong, Synopsys Inc.	424
A3. Implications of the New ANSI/ESD S2020 Specification	
Moderators: John Kinnear, IBM Corporation; David Swenson, Affinity Static Control Consulting; Scott Ward, Texas Instruments	425

Workshop Session B

B1. What Should Foundries Include in Their PDKs to Better Support Custom ESD Design?	
Moderators: Stephen Fairbanks, SRF Technologies; David Klein, Synaptics.....	426
B2. Is HBM-1000V/CDM-250V Now the Industry Default Qualification Target for IC Components?	
Moderators: Brett Carn, Intel; Rita Horner, Synopsys Inc.	427
B3. Component System Level ESD Design; Efforts by Auto Tier 1's to Define Standard Tests	
Moderators: Reinhold Gaertner, Infineon; Edgar Kuhn, Continental	428
Biographies	429
Past Awards and Presentations	465
2015 Exhibitors List	477