

2015 25th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS 2015)

**Salvador, Brazil
1 – 4 September 2015**



**IEEE Catalog Number: CFP15PAT-POD
ISBN: 978-1-4673-9420-8**

Table of Contents

Introductory Section

Foreword	vii
Organization Committee	viii
Steering Committee	ix
Paper Awards	x
Technical Program Committee	xi
2016 Call-for-Papers	xii

Tutorials

Low Power Design Essentials	xiv
<i>Jan Rabaey, University of California at Berkeley - UCB, USA</i>	
Ultra-Low-Voltage (ULV) IC Design: Designing for VDD below kT/q	xv
<i>Márcio Cherem Schneider, Universidade Federal de Santa Catarina - UFSC, Brazil</i>	
3D ICs - Moving from Silicon to Heterogeneous Technologies	xvi
<i>Maciej Ogorzalek, Jagiellonian University, Krakow, Poland</i>	
Cyber - Physical Systems: Reality, Dreams, and Fantasy	xvii
<i>Magdy A. Bayoumi, University of Louisiana at Lafayette, USA</i>	

Keynotes

Lessons from Brain Connectivity for Future Interconnect in ICs	xix
<i>Jan Rabaey, University of California at Berkeley - UCB, USA</i>	
Majority-based Synthesis for Digital Nano-technologies	xx
<i>Giovanni de Micheli, EPFL, Switzerland</i>	
A Path towards Average-Case Silicon via Asynchronous Resilient Bundled-Data Design	xxi
<i>Peter Beerel, University of Southern California (USC) in Los Angeles, USA</i>	

Invited Talks

Frame Free Vision	xxiii
<i>Teresa Serrano-Gotarredona, IMSECNM-CSIC, Sevilla; University of Sevilla, Spain</i>	
System-Level Design of Heterogeneous System-on-Chip Architectures	xxiv
<i>Luca Carloni, Columbia University, USA</i>	
Rethinking "Things" Design - The Missing Technology Link in the Internet of Things (IoT)	xxv
<i>Massimo Alioto, National Univ. of Singapore, Singapore</i>	

Session 1: Circuit and system optimization

Chair: Ran Ginosar, Technion-Israel Institute of Technology, Israel

- 1.1. **Response Time Schedulability Analysis for Hard Real-Time Systems Accounting DVFS Latency on Heterogeneous Cluster-based Platform** 1
Eduardo Bezerra Valentin, Mario Salvatierra, Rosiane Freitas and Raimundo Barreto, (Federal University of Amazonas, Brazil)
- 1.2. **Inferring Custom Architectures from OpenCL** 9
Krzysztof Kepa, Ritesh Soni and Peter Athanas, (Virginia Tech, USA)
- 1.3. **ABeeMap: A Mapping Algorithm based on Multi-Objective Artificial Bee Colony** 17
Viviane Souza and Abel Silva-Filho, (Federal University of Pernambuco, Brazil)
- 1.4. **Efficient Parallelization of the Discrete Wavelet Transform Algorithm using Memory-oblivious Optimizations** 25
Anastasis Keliris¹, Vasilis Dimitzas, Olympia Kremmyda², Dimitris Gizopoulos², and Michail Maniatakos¹, (¹NYU, USA and ²University of Athens, Greece)
- 1.5. **Calculation of Worst-Case Execution Time for Multicore Processors using Deterministic Execution** 33
Hamid Mushtaq¹, Zaid Al-Ars² and Koen Bertels¹, (¹TU Delft and ²Delft University, Netherlands)
- 1.6. **An Unconventional Computing Technique for Ultra- Fast and Ultra-low power Data Mining** 40
Vincent Canals, Antoni Morro, Antoni Oliver, Miquel Lleó Alomar and Josep L. Rosselló, (Universitat de les Illes Balears, Spain)

Session 2: System-Level Design and Management

Chair: Vincent Canals, Balearic Islands University, Spain

- 2.1. **Tejas: A Java based Versatile Micro-architectural Simulator** 47
Smruti R. Sarangi, Rajshekar Kalayappan, Prathmesh Kallurkar, Seep Goel and Eldhose Peter, (IIT Delhi, India)
- 2.2. **Dedicated Network for Distributed Configuration in a Mixed-Signal Wireless Sensor Node Circuit** 55
Soundous Chairat, Edith Beigné and Marc Belleville, (CEA LETI, France)
- 2.3. **Energy Management via PI Control for Data Parallel Applications with Throughput Constraints** 63
Anca Molnos, Warody Lombardi, Diego Puschini, Julien Mottin, Suzanne Lesecq, and Arnaud Tonda, (CEA LETI, France)
- 2.4. **VLSI Architecture Design and Implementation of a LDPC Encoder for the IEEE 802.22 WRAN Standard** 71
Nelson Alves Ferreira Neto¹, Wagner Luiz Alves de Oliveira², João Carlos Nunes Bittencourt³ and Joaquim Ranyere Santana de Oliveira², (¹LSITEC-NE, ²UFBA, ³UEFS, Brazil)

Special Session: Celebrating the 25th Anniversary of PATMOS

Chair: Ricardo Reis, UFRGS, Brazil

S.1. Presentation of PATMOS History

Ricardo Reis (UFRGS, Brazil) and Jorge Juan Chico (University of Sevilla, Spain)

S.2. How to Cope with the Power Wall

Reiner Hartenstein (TU Kaiserslautern, Germany)

S.3. Panel

Reiner Hartenstein (TU Kaiserslautern, Germany), Josep Rosseló (UIB, Spain), Jorge Juan Chico (University of Sevilla, Spain) and Ricardo Reis (UFRGS, Brazil)

Session 3: Low Power Design Techniques

Chair: Jose Luis Guntzel, UFSC, Brazil

- 3.1. Dynamic Current Reduction of CMOS Digital Circuits through Design and Process Optimization 77**
Jordan Innocenti¹, Loïc Welter¹, Nicolas Borrel¹, Franck Julien¹, Jean-Michel Portal², Jacques Sonzogni¹, Laurent Lopez¹, Pascal Masson³, Stephan Niel¹, Philippe Dreux¹ and Julia Castellan¹, (¹STMicroelectronics, ²Aix-Marseille University, ³Nice Sophia-Antipolis University, France)
- 3.2. Unified Power Format (UPF) Methodology in a Vendor Independent Flow 82**
Emilie Garat, David Coriat, Edith Beigné and Leandro Stefanazzi, (CEA LETI, Minatec, France)
- 3.3. Asynchronous Sub-Threshold Ultra-Low Power Processor 89**
Ron Diamant¹, Ran Ginosar¹ and Christos Sotiriou², (¹Technion IIT, Israel, ²University of Thessaly, Greece)
- 3.4. Constructing Stability-based Clock Gating with Hierarchical Clustering 97**
Bao Le¹, Djordje Maksimovic¹, Dipanjan Sengupta², Erhan Ergin³, Ryan Berryhill¹ and Andreas Veneris¹, (¹University of Toronto, Canada, ²Advanced Micro Devices, Inc., Canada, ³AMD, USA)
- 3.5. Adaptive Energy Minimization of Embedded Heterogeneous Systems using Regression-based Learning 103**
Sheng Yang¹, Rishad Shafik¹, Geoff Merrett¹, Ed Stott², Joshua Levine², James Davis² and Bashir Al-Hashimi¹, (¹University of Southampton, ²Imperial College, United Kingdom)
- 3.6. Evaluation and Mitigation of Aging Effects on a Digital On-Chip Voltage and Temperature Sensor 111**
Mauricio Altieri, Suzanne Lesecq, Diego Puschini, Olivier Heron, Edith Beigne and Jorge Rodas, (CEA LETI, France)

Session 4: Reliability, Noise Reduction And Robustness

Chair: Jorge Juan-Chico, Seville University, Spain

- 4.1. Exploration of Technology Parameter Values of Integrated Circuit Technologies** 118
Rodrigo Fonseca Rocha Soares¹, Frank Sill Torres^{1,2} and Dirk Timmermann³ (¹UFMG, Brazil, ²DELT, ³University of Rostock, Germany)
- 4.2. Frequency-Domain Modeling of Ground Bounce and Substrate Noise for Synchronous and GALS Systems** 126
Milan Babic, Xin Fan and Milos Krstic (IHP, Germany)
- 4.3. Better-than-Voltage Scaling Energy Reduction in Approximate SRAMs via Bit Dropping and Bit Reuse** 133
Fabio Frustaci¹, David Blaauw², Dennis Sylvester² and Massimo Alioto³, (¹University of Calabria, Italy, ²University of Michigan, USA, ³National University of Singapore, Singapore)
- 4.4. A Versatile and Reliable Glitch Filter for Clocks** 140
Robert Najvirt and Andreas Steininger, (TU Wien, Austria)

Session 5: Energy-Efficiency Systems

Chair: Frank Sill Torres, UFMG, Brazil

- 5.1. Energy-Efficient Level Shifter Topology** 148
Roger Llanos, Diego Sousa, Marco Terres, Guilherme Bontorin, Ricardo Reis and Marcelo Johann, (UFRGS, Brazil)
- 5.2. Energy efficiency of Zipf traffic distributions within Facebook's data center fabric architecture** 152
Lisa Durbeck¹, Nicholas Macias¹ and Joseph Tront², (¹Cell Matrix Corporation, USA, ²Clark College, USA)
- 5.3. Energy-Aware Mapping for Dependable Virtual Networks** 161
Victor Lira and Eduardo Tavares, (Federal University of Pernambuco, Brazil)
- 5.4. Reusing Smaller Optimized FFT Blocks for the Realization of Larger Power Efficient Radix-2 FFTs** 169
Sidinei Ghissoni¹, Eduardo Da Costa² and Ricardo Reis³, (¹Unipampa, ²UCPel, ³UFRGS, Brazil)
- 5.5. Combining Pel Decimation with Partial Distortion Elimination to Increase SAD Energy Efficiency** 177
Ismael Seidel, André Beims Bräscher and Jose Luis Güntzel, (UFSC, Brazil)
- 5.6. Wideband Dynamic Voltage Sensing Mechanism for EH Systems** 185
Kaiyuan Gao¹, Yuqing Xu¹, Delong Shang¹, Fei Xia¹ and Alex Yakovlev² (Newcastle University¹, University of Newcastle upon Tyne², United Kingdom)