

2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC 2016)

**Macao
25-28 January 2016**



**IEEE Catalog Number: CFP16ASP-POD
ISBN: 978-1-4673-9570-0**

**Copyright © 2016 by the Institute of Electrical and Electronic Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

******This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

| | |
|-------------------------|-------------------|
| IEEE Catalog Number: | CFP16ASP-POD |
| ISBN (Print-On-Demand): | 978-1-4673-9570-0 |
| ISBN (Online): | 978-1-4673-9569-4 |
| ISSN: | 2153-6961 |

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

| | |
|--|----|
| AN AUTOMATIC PLACE-AND-ROUTED TWO-STAGE FRACTIONAL-N INJECTION-LOCKED PLL USING SOFT INJECTION | 1 |
| <i>D. Yang ; W. Deng ; A. T. Narayanan ; K. Nakata ; T. Siriburanon ; K. Okada ; A. Matsuzawa</i> | |
| TIME-DOMAIN I/Q-LOFT COMPENSATOR USING A SIMPLE ENVELOPE DETECTOR FOR A SUB-GHZ IEEE 802.11AF WLAN TRANSMITTER | 3 |
| <i>C. F. Cheang ; K. F. Un ; P. I. Mak ; R. P. Martins</i> | |
| A NOISE REDUCTION TECHNIQUE FOR DIVIDER-LESS FRACTIONAL-N FREQUENCY SYNTHESIZER USING PHASE-INTERPOLATION TECHNIQUE | 5 |
| <i>A. T. Narayanan ; M. Katsuragi ; K. Nakata ; Y. Terashima ; K. Okada ; A. Matsuzawa</i> | |
| A 2.2μW 15B INCREMENTAL DELTA-SIGMA ADC WITH OUTPUT-DRIVEN INPUT SEGMENTATION | 7 |
| <i>Bo Wang ; Man Kay Law ; S. Mohamad ; A. Bernak</i> | |
| A 200-MHZ 4-PHASE FULLY INTEGRATED VOLTAGE REGULATOR WITH LOCAL GROUND SENSING DUAL LOOP ZDS HYSTERETIC CONTROL USING 6.5NH PACKAGE BONDWIRE INDUCTORS ON 65NM BULK CMOS | 9 |
| <i>M. K. Song ; J. Sankman ; J. Lee ; Dongsheng Ma</i> | |
| AN AC POWERED CONVERTER-FREE LED DRIVER WITH LOW FLICKER | 11 |
| <i>Y. Gao ; L. Li ; P. K. T. Mok</i> | |
| A VARIABLE-VOLTAGE LOW-POWER TECHNIQUE FOR DIGITAL CIRCUIT SYSTEM | 13 |
| <i>A. T. Xiao ; Y. S. Miao ; C. H. Cheng ; J. I. Guo</i> | |
| SUB-THRESHOLD VLSI LOGIC FAMILY EXPLOITING UNBALANCED PULL-UP/DOWN NETWORK, LOGICAL EFFORT AND INVERSE-NARROW-WIDTH TECHNIQUES | 15 |
| <i>M. Z. Li ; C. I. Jeong ; M. K. Law ; P. I. Mak ; M. I. Vai ; S. H. Pun ; R. P. Martins</i> | |
| A TESTABLE AND DEBUGGABLE DUAL-CORE SYSTEM WITH THERMAL-AWARE DYNAMIC VOLTAGE AND FREQUENCY SCALING | 17 |
| <i>L. Y. Lu ; C. Y. Chang ; Z. H. Chen ; B. T. Yeh ; T. H. Lu ; P. Y. Chen ; P. H. Tang ; K. J. Lee ; L. Y. Chiou ; S. J. Chang ; C. H. Tsai ; C. H. Chen ; J. M. Lin</i> | |
| RAPID PROTOTYPING OF MULTI-MODE QC-LDPC DECODER FOR 802.11N/AC STANDARD | 19 |
| <i>Q. Lu ; C. W. Sham ; F. C. M. Lau</i> | |
| SUB-μW QRS DETECTION PROCESSOR USING QUADRATIC SPLINE WAVELET TRANSFORM AND MAXIMA MODULUS PAIR RECOGNITION FOR POWER-EFFICIENT WIRELESS ARRHYTHMIA MONITORING | 21 |
| <i>C. I. Jeong ; P. I. Mak ; M. I. Vai ; R. P. Martins</i> | |
| DESIGN OF AN ENERGY-AUTONOMOUS, DISPOSABLE, SUPPLY-SENSING BIOSENSOR USING BIO FUEL CELL AND 0.23-V 0.25-μM ZERO-VTH ALL-DIGITAL CMOS SUPPLY-CONTROLLED RING OSCILLATOR WITH INDUCTIVE TRANSMITTER | 23 |
| <i>K. Niitsu ; A. Kobayashi ; Y. Ogawa ; M. Nishizawa ; K. Nakazato</i> | |
| PERFORMANCE-CENTRIC REGISTER FILE DESIGN FOR GPUS USING RACETRACK MEMORY | 25 |
| <i>Shuo Wang ; Yun Liang ; Chao Zhang ; Xiaolong Xie ; Guangyu Sun ; Yongpan Liu ; Yu Wang ; Xiuhong Li</i> | |
| IMPROVING READ PERFORMANCE OF STT-MRAM BASED MAIN MEMORIES THROUGH SMASH READ AND FLEXIBLE READ | 31 |
| <i>Lei Jiang ; Wujie Wen ; D. Wang ; L. Duan</i> | |
| STLAC: A SPATIAL AND TEMPORAL LOCALITY-AWARE CACHE AND NETWORK-ON-CHIP CODESIGN FOR TILED MANY-CORE SYSTEMS | 37 |
| <i>Mingyu Wang ; Zhaolin Li</i> | |
| A LIGHTWEIGHT OPENMP4 RUN-TIME FOR EMBEDDED SYSTEMS | 43 |
| <i>R. E. Vargas ; S. Royuela ; M. A. Serrano ; X. Martorell ; E. Quinones</i> | |
| IMPROVING TAG GENERATION FOR MEMORY DATA AUTHENTICATION IN EMBEDDED PROCESSOR SYSTEMS | 50 |
| <i>Tao Liu ; Hui Guo ; S. Parameswaran ; X. S. Hu</i> | |
| JTAG-BASED ROBUST PCB AUTHENTICATION FOR PROTECTION AGAINST COUNTERFEITING ATTACKS | 56 |
| <i>A. Hennessy ; Y. Zheng ; S. Bhunia</i> | |
| MAXIMIZING LEVEL OF CONFIDENCE FOR NON-EQUIDISTANT CHECKPOINTING | 62 |
| <i>D. Nikolov ; E. Larsson</i> | |

| | |
|---|-----|
| A MUTUAL AUDITING FRAMEWORK TO PROTECT IOT AGAINST HARDWARE TROJANS | 69 |
| <i>C. Liu ; P. Cronin ; C. Yang</i> | |
| SIMULTANEOUS TEMPLATE OPTIMIZATION AND MASK ASSIGNMENT FOR DSA WITH MULTIPLE PATTERNING | 75 |
| <i>J. Kuang ; Junjie Ye ; E. F. Y. Young</i> | |
| MASK OPTIMIZATION FOR DIRECTED SELF-ASSEMBLY LITHOGRAPHY: INVERSE DSA AND INVERSE LITHOGRAPHY | 83 |
| <i>Seongbo Shim ; Youngsoo Shin</i> | |
| CUT REDISTRIBUTION WITH DIRECTED SELF-ASSEMBLY TEMPLATES FOR ADVANCED 1-D GRIDDED LAYOUTS | 89 |
| <i>Z. W. Lin ; Y. W. Chang</i> | |
| CONTACT LAYER DECOMPOSITION TO ENABLE DSA WITH MULTI-PATTERNING TECHNIQUE FOR STANDARD CELL BASED LAYOUT | 95 |
| <i>Z. Xiao ; C. X. Lin ; M. D. F. Wong ; H. Zhang</i> | |
| LOGIC AND MEMORY DESIGN USING SPIN-BASED CIRCUITS | 103 |
| <i>Zhaoxin Liang ; M. Mankalale ; B. Del Bel ; S. S. Sapatmekar</i> | |
| ARCHITECTURE DESIGN WITH STT-RAM: OPPORTUNITIES AND CHALLENGES | 109 |
| <i>P. Chi ; S. Li ; Yuanqing Cheng ; Yu Lu ; S. H. Kang ; Y. Xie</i> | |
| PROSPECTS OF EFFICIENT NEURAL COMPUTING WITH ARRAYS OF MAGNETO-METALLIC NEURONS AND SYNAPSES | 115 |
| <i>A. Sengupta ; K. Yogendra ; D. Fan ; K. Roy</i> | |
| AUTOMATIC ABSTRACTION REFINEMENT OF TR FOR PDR | 121 |
| <i>K. Fan ; M. J. Yang ; C. Y. Huang</i> | |
| A COMPLETE APPROACH TO UNREACHABLE STATE DIAGNOSABILITY VIA PROPERTY DIRECTED REACHABILITY | 127 |
| <i>R. Berryhill ; A. Veneris</i> | |
| FORMALLY ANALYZING FAULT TOLERANCE IN DATAPATH DESIGNS USING EQUIVALENCE CHECKING | 133 |
| <i>P. Behnam ; B. Alizadeh ; S. Taheri ; M. Fujita</i> | |
| COUPLING REVERSE ENGINEERING AND SAT TO TACKLE NP-COMPLETE ARITHMETIC CIRCUITRY VERIFICATION IN $\sim O(\# \text{ OF GATES})$ | 139 |
| <i>Y. Diao ; X. Wei ; T. K. Lam ; Y. L. Wu</i> | |
| NVPSIM: A SIMULATOR FOR ARCHITECTURE EXPLORATIONS OF NONVOLATILE PROCESSORS | 147 |
| <i>Yizi Gu ; Y. Liu ; Y. Wang ; H. Li ; H. Yang</i> | |
| MCSSIM: A MEMORY CHANNEL STORAGE SIMULATOR | 153 |
| <i>R. Chen ; Z. Shao ; C. L. Yang ; Tao Li</i> | |
| TRACE-BASED CONTEXT-SENSITIVE TIMING SIMULATION CONSIDERING EXECUTION PATH VARIATIONS | 159 |
| <i>S. Otlık ; J. M. Borrmann ; S. Asbach ; A. Viehl ; W. Rosenstiel ; O. Bringmann</i> | |
| GENERATING HIGH COVERAGE TESTS FOR SYSTEMC DESIGNS USING SYMBOLIC EXECUTION | 166 |
| <i>Bin Lin ; Zhenkun Yang ; Kai Cong ; Fei Xie</i> | |
| CIRCULAR-CONTOUR-BASED OBSTACLE-AWARE MACRO PLACEMENT | 172 |
| <i>C. H. Chiou ; C. H. Chang ; S. T. Chen ; Y. W. Chang</i> | |
| LEARNING-BASED PREDICTION OF EMBEDDED MEMORY TIMING FAILURES DURING INITIAL FLOORPLAN DESIGN | 178 |
| <i>W. T. J. Chan ; Kun Young Chung ; A. B. Kahng ; N. D. MacDonald ; S. Nath</i> | |
| STITCH AWARE DETAILED PLACEMENT FOR MULTIPLE E-BEAM LITHOGRAPHY | 186 |
| <i>Yibo Lin ; B. Yu ; Yi Zou ; Z. Li ; C. J. Alpert ; D. Z. Pan</i> | |
| MINIMUM IMPLANT AREA-AWARE PLACEMENT AND THRESHOLD VOLTAGE REFINEMENT | 192 |
| <i>S. I. Lei ; W. K. Mak ; C. Chu</i> | |
| DESIGN AND VERIFICATION USING HIGH-LEVEL SYNTHESIS | 198 |
| <i>A. Takach</i> | |
| HIGH-LEVEL SYNTHESIS OF ACCELERATORS IN EMBEDDED SCALABLE PLATFORMS | 204 |
| <i>P. Mantovani ; G. Di Guglielmo ; L. P. Carloni</i> | |
| HIGH QUALITY IP DESIGN USING HIGH-LEVEL SYNTHESIS DESIGN FLOW | 212 |
| <i>Q. Zhu ; M. Tatsuoaka</i> | |
| DESIGNING HIGH-QUALITY HARDWARE ON A DEVELOPMENT EFFORT BUDGET: A STUDY OF THE CURRENT STATE OF HIGH-LEVEL SYNTHESIS | 218 |
| <i>Zelei Sun ; K. Campbell ; W. Zuo ; K. Rupnow ; S. Gurumani ; F. Doucet ; D. Chen</i> | |

| | |
|---|-----|
| CLOCK BUFFER POLARITY ASSIGNMENT UTILIZING USEFUL CLOCK SKEWS FOR POWER NOISE REDUCTION..... | 226 |
| <i>D. Joo ; T. Kim</i> | |
| BUFFER INSERTION TO REMOVE HOLD VIOLATIONS AT MULTIPLE PROCESS CORNERS..... | 232 |
| <i>Inhak Han ; Daijoon Hyun ; Youngsoo Shin</i> | |
| SPEED BINNING WITH HIGH-QUALITY STRUCTURAL PATTERNS FROM FUNCTIONAL TIMING ANALYSIS (FTA)..... | 238 |
| <i>L. Y. Z. Lin ; C. H. P. Wen</i> | |
| ELECTROMIGRATION RECOVERY MODELING AND ANALYSIS UNDER TIME-DEPENDENT CURRENT AND TEMPERATURE STRESSING..... | 244 |
| <i>X. Huang ; V. Sukharev ; T. Kim ; H. Chen ; S. X. D. Tan</i> | |
| A NOVEL LOW-COST DYNAMIC LOGIC RECONFIGURABLE STRUCTURE STRATEGY FOR LOW POWER OPTIMIZATION..... | 250 |
| <i>Y. G. Chen ; W. Y. Wen ; Y. T. Wang ; Y. L. Lee ; S. C. Chang</i> | |
| AN ENERGY-EFFICIENT RANDOM NUMBER GENERATOR FOR STOCHASTIC CIRCUITS..... | 256 |
| <i>K. Kim ; J. Lee ; K. Choi</i> | |
| DESIGN OF AN ALL-DIGITAL TEMPERATURE SENSOR IN 28 NM CMOS USING TEMPERATURE-SENSITIVE DELAY CELLS AND ADAPTIVE-1P CALIBRATION FOR ERROR REDUCTION..... | 262 |
| <i>S. Y. Li ; P. Y. Chou ; J. S. Wang</i> | |
| DESIGN AND ALLOCATION OF LOOSELY COUPLED MULTI-BIT FLIP-FLOPS FOR POWER REDUCTION IN POST-PLACEMENT OPTIMIZATION..... | 268 |
| <i>H. Moon ; T. Kim</i> | |
| THERMAL OPTIMIZATION FOR MEMRISTOR-BASED HYBRID NEUROMORPHIC COMPUTING SYSTEMS..... | 274 |
| <i>C. R. Wu ; W. Wen ; T. Y. Ho ; Y. Chen</i> | |
| AN ENERGY-EFFICIENT MATRIX MULTIPLICATION ACCELERATOR BY DISTRIBUTED IN-MEMORY COMPUTING ON BINARY RRAM CROSSBAR..... | 280 |
| <i>Leibin Ni ; Yuhao Wang ; H. Yu ; Wei Yang ; Chuliang Weng ; Junfeng Zhao</i> | |
| A RACETRACK MEMORY BASED IN-MEMORY BOOTH MULTIPLIER FOR CRYPTOGRAPHY APPLICATION..... | 286 |
| <i>T. Luo ; W. Zhang ; B. He ; D. Maskell</i> | |
| LOOK-AHEAD SCHEMES FOR NEAREST NEIGHBOR OPTIMIZATION OF 1D AND 2D QUANTUM CIRCUITS..... | 292 |
| <i>R. Wille ; O. Keszcze ; M. Walter ; P. Rohrs ; A. Chattopadhyay ; R. Drechsler</i> | |
| ENERGY-EFFICIENT SYSTEM DESIGN FOR IOT DEVICES..... | 298 |
| <i>H. Jayakumar ; A. Raha ; Y. Kim ; S. Sutar ; W. S. Lee ; V. Raghunathan</i> | |
| (INVITED PAPER) ENERGY DELIVERY FOR SELF-POWERED IOT DEVICES..... | 302 |
| <i>K. Z. Ahmed ; M. Kar ; S. Mukhopadhyay</i> | |
| EFFICIENT EMBEDDED LEARNING FOR IOT DEVICES..... | 308 |
| <i>S. Venkataramani ; K. Roy ; A. Raghunathan</i> | |
| COMPUTING WITH COUPLED SPIN TORQUE NANO OSCILLATORS..... | 312 |
| <i>K. Yogendra ; D. Fan ; Y. Shim ; M. Koo ; K. Roy</i> | |
| APPROXMAP: ON TASK ALLOCATION AND SCHEDULING FOR RESILIENT APPLICATIONS..... | 318 |
| <i>J. Yi ; Q. Zhang ; Y. Tian ; T. Wang ; W. Liu ; E. H. M. Sha ; Q. Xu</i> | |
| ENERGY OPTIMIZATION OF STOCHASTIC APPLICATIONS WITH STATISTICAL GUARANTEES OF DEADLINE AND RELIABILITY..... | 324 |
| <i>Xiong Pan ; Wei Jiang ; Ke Jiang ; Liang Wen ; Qi Dong</i> | |
| SMOSI: A FRAMEWORK FOR THE DERIVATION OF SLEEP MODE TRACES FROM RTL SIMULATIONS..... | 330 |
| <i>D. Peterson ; O. Bringmann</i> | |
| OPTIMIZATION OF BEHAVIORAL IPS IN MULTI-PROCESSOR SYSTEM-ON-CHIPS..... | 336 |
| <i>Y. Liu ; B. C. Schafer</i> | |
| A NOVEL PUF BASED ON CELL ERROR RATE DISTRIBUTION OF STT-RAM..... | 342 |
| <i>X. Zhang ; Guangyu Sun ; Y. Zhang ; Y. Chen ; Hai Li ; Wujie Wen ; Jia Di</i> | |
| DATA PRIVACY IN NON-VOLATILE CACHE: CHALLENGES, ATTACK MODELS AND SOLUTIONS..... | 348 |
| <i>N. Rathi ; S. Ghosh ; A. Iyengar ; H. Naeimi</i> | |
| PIN TUMBLER LOCK: A SHIFT BASED ENCRYPTION MECHANISM FOR RACETRACK MEMORY..... | 354 |
| <i>H. Zhang ; C. Zhang ; X. Zhang ; G. Sun ; Jiwu Shu</i> | |

| | |
|---|-----|
| ROUTING PATH REUSE MAXIMIZATION FOR EFFICIENT NV-FPGA RECONFIGURATION | 360 |
| <i>Y. Xue ; P. Cronin ; C. Yang ; J. Hu</i> | |
| MCMM CLOCK TREE OPTIMIZATION BASED ON SLACK REDISTRIBUTION USING A REDUCED SLACK GRAPH | 366 |
| <i>R. Ewetz ; C. K. Koh</i> | |
| DYNAMIC PLANNING OF LOCAL CONGESTION FROM VARYING-SIZE VIAS FOR GLOBAL ROUTING LAYER ASSIGNMENT | 372 |
| <i>D. Shi ; E. Tashjian ; A. Davoodi</i> | |
| NEGOTIATION-BASED TRACK ASSIGNMENT CONSIDERING LOCAL NETS | 378 |
| <i>M. P. Wong ; W. H. Liu ; T. C. Wang</i> | |
| ORDERED ESCAPE ROUTING FOR GRID PIN ARRAY BASED ON MIN-COST MULTI-COMMODITY FLOW | 384 |
| <i>Fengxian Jiao ; Sheqin Dong</i> | |
| EFFICIENT RELIABILITY MANAGEMENT IN SOCS - AN APPROXIMATE DRAM PERSPECTIVE | 390 |
| <i>M. Jung ; D. M. Mathew ; C. Weis ; N. Wehn</i> | |
| CROSS-LAYER VIRTUAL/PHYSICAL SENSING AND ACTUATION FOR RESILIENT HETEROGENEOUS MANY-CORE SOCS | 395 |
| <i>S. Sarma ; T. Muck ; M. Shoushtari ; A. BanaiyanMofrad ; N. Dutt</i> | |
| ON-CHIP MONITORING AND COMPENSATION SCHEME WITH FINE-GRAIN BODY BIASING FOR ROBUST AND ENERGY-EFFICIENT OPERATIONS | 403 |
| <i>A. K. M. M. Islam ; H. Onodera</i> | |
| EMBEDDED SOFTWARE RELIABILITY TESTING BY UNIT-LEVEL FAULT INJECTION | 410 |
| <i>P. R. Maier ; V. B. Kleeberger</i> | |
| THERMAL MODELING FOR ENERGY-EFFICIENT SMART BUILDING WITH ADVANCED OVERFITTING MITIGATION TECHNIQUE | 417 |
| <i>Wandi Liu ; Hai Wang ; Hengyang Zhao ; Shujuan Wang ; Haibao Chen ; Yuzhuo Fu ; Jian Ma ; Xin Li ; S. X. D. Tan</i> | |
| MODELING, ANALYSIS, AND OPTIMIZATION OF ELECTRIC VEHICLE HVAC SYSTEMS | 423 |
| <i>M. A. Al Faruque ; K. Vatanparvar</i> | |
| DISTRIBUTED RECONFIGURABLE BATTERY SYSTEM MANAGEMENT ARCHITECTURES | 429 |
| <i>S. Steinhorst ; Z. Shao ; S. Chakraborty ; M. Kauer ; S. Li ; M. Lukasiewicz ; S. Narayanaswamy ; M. U. Rafique ; Q. Wang</i> | |
| MINIMUM-ENERGY DRIVING SPEED PROFILES FOR LOW-SPEED ELECTRIC VEHICLES | 435 |
| <i>D. Baek ; J. Hong ; N. Chang</i> | |
| MULTI-VERSION CHECKPOINTING FOR FLASH FILE SYSTEMS | 436 |
| <i>S. C. Chou ; Y. H. Chang ; Yuan-Hung Kua ; P. C. Huang ; C. W. Tsao</i> | |
| RELAY-BASED KEY MANAGEMENT TO SUPPORT SECURE DELETION FOR RESOURCE-CONSTRAINED FLASH-MEMORY STORAGE DEVICES | 444 |
| <i>W. L. Wang ; Y. H. Chang ; P. C. Huang ; C. H. Tu ; H. W. Wei ; W. K. Shih</i> | |
| PEAK-TO-AVERAGE PUMPING EFFICIENCY IMPROVEMENT FOR CHARGE PUMP IN PHASE CHANGE MEMORIES | 450 |
| <i>H. Luo ; J. Hu ; Liang Shi ; C. J. Xue ; Q. Zhuge</i> | |
| EXPLOITING PARALLELISM OF IMPERFECT NESTED LOOPS WITH SIBLING INNER LOOPS ON COARSE-GRAINED RECONFIGURABLE ARCHITECTURES | 456 |
| <i>Xinhan Lin ; S. Yin ; L. Liu ; S. Wei</i> | |
| SLOWMO - ENHANCING MOBILE GESTURE-BASED AUTHENTICATION SCHEMES VIA SAMPLING RATE OPTIMIZATION | 462 |
| <i>K. W. Nixon ; Xiang Chen ; Z. H. Mao ; Yiran Chen</i> | |
| LATTICE-BASED BOOLEAN DIAGRAMS | 468 |
| <i>A. Nassar ; F. J. Kurdahi</i> | |
| BDD MINIMIZATION FOR APPROXIMATE COMPUTING | 474 |
| <i>M. Soeken ; D. GroBe ; A. Chandrasekharan ; R. Drechsler</i> | |
| MAJORSAT: A SAT SOLVER TO MAJORITY LOGIC | 480 |
| <i>Y. M. Chou ; Y. C. Chen ; C. Y. Wang ; C. Y. Huang</i> | |
| FAST SYNTHESIS OF THRESHOLD LOGIC NETWORKS WITH OPTIMIZATION | 486 |
| <i>Y. C. Chen ; R. Wang ; Y. P. Chang</i> | |
| POLYSYNCHRONOUS STOCHASTIC CIRCUITS | 492 |
| <i>M. H. Najafi ; D. J. Lilja ; M. Riedel ; K. Bazargan</i> | |
| MAJORITY-BASED SYNTHESIS FOR NANOTECHNOLOGIES | 499 |
| <i>L. Amaru ; P. E. Gaillardon ; G. De Micheli</i> | |

| | |
|--|------------|
| A SCALABLE COMMUNICATION-AWARE COMPILATION FLOW FOR PROGRAMMABLE ACCELERATORS | 503 |
| <i>J. Cong ; H. Huang ; M. A. Ghodrat</i> | |
| ENABLING MULTI-LAYER CYBER-SECURITY ASSESSMENT OF INDUSTRIAL CONTROL SYSTEMS THROUGH HARDWARE-IN-THE-LOOP TESTBEDS | 511 |
| <i>A. Keliris ; C. Konstantinou ; N. G. Tsoutsos ; R. Baiad ; M. Maniatakos</i> | |
| SECURITY ANALYSIS ON CONSUMER AND INDUSTRIAL IOT DEVICES | 519 |
| <i>J. Wurm ; K. Hoang ; O. Arias ; A. R. Sadeghi ; Y. Jin</i> | |
| COVERT CHANNELS USING MOBILE DEVICE'S MAGNETIC FIELD SENSORS..... | 525 |
| <i>N. Matyunin ; J. Szefer ; S. Biedermann ; S. Katzenbeisser</i> | |
| MULTI-VALUED ARBITERS FOR QUALITY ENHANCEMENT OF PUF RESPONSES ON FPGA IMPLEMENTATION | 533 |
| <i>S. S. Zaliwaka ; A. V. Puchkov ; V. P. Klybik ; A. A. Ivaniuk ; C. H. Chang</i> | |
| EVERY TEST MAKES A DIFFERENCE: COMPRESSING ANALOG TESTS TO DECREASE PRODUCTION COSTS | 539 |
| <i>S. N. Ahmadyan ; S. Natarajan ; S. Vasudevan</i> | |
| RE-THINKING POLYNOMIAL OPTIMIZATION: EFFICIENT PROGRAMMING OF RECONFIGURABLE RADIO FREQUENCY (RF) SYSTEMS BY CONVEXIFICATION | 545 |
| <i>F. Wang ; Shihui Yin ; M. Jun ; X. Li ; T. Mukherjee ; R. Negi ; L. Pileggi</i> | |
| AN EFFICIENT TRAJECTORY-BASED ALGORITHM FOR MODEL ORDER REDUCTION OF NONLINEAR SYSTEMS VIA LOCALIZED PROJECTION AND GLOBAL INTERPOLATION..... | 551 |
| <i>C. Yang ; F. Yang ; X. Zeng ; Dian Zhou</i> | |
| STORM: A NONLINEAR MODEL ORDER REDUCTION METHOD VIA SYMMETRIC TENSOR DECOMPOSITION | 557 |
| <i>Jian Deng ; H. Liu ; K. Batselier ; Y. K. Kwok ; N. Wong</i> | |
| FOOTFALL - GPS POLLING SCHEDULER FOR POWER SAVING ON WEARABLE DEVICES | 563 |
| <i>K. W. Nixon ; Xiang Chen ; Yiran Chen</i> | |
| CP-FPGA: COMPUTATION DATA-AWARE SOFTWARE/HARDWARE CO-DESIGN FOR NONVOLATILE FPGAS BASED ON CHECKPOINTING TECHNIQUES..... | 569 |
| <i>Zhe Yuan ; Yongpan Liu ; Hehe Li ; Huazhong Yang</i> | |
| DESIGN SPACE EXPLORATION OF FPGA-BASED DEEP CONVOLUTIONAL NEURAL NETWORKS..... | 575 |
| <i>M. Motamedi ; P. Gysel ; V. Akella ; S. Ghiasi</i> | |
| LRADNN: HIGH-THROUGHPUT AND ENERGY-EFFICIENT DEEP NEURAL NETWORK ACCELERATOR USING LOW RANK APPROXIMATION..... | 581 |
| <i>Jingyang Zhu ; Zhiliang Qian ; Chi-Ying Tsui</i> | |
| SEQUENCE-PAIR-BASED PLACEMENT AND ROUTING FOR FLOW-BASED MICROFLUIDIC BIOCHIPS..... | 587 |
| <i>Qin Wang ; Yizhong Ru ; H. Yao ; T. Y. Ho ; Y. Cai</i> | |
| CONGESTION- AND TIMING-DRIVEN DROPLET ROUTING FOR PIN-CONSTRAINED PAPER-BASED MICROFLUIDIC BIOCHIPS | 593 |
| <i>J. D. Li ; S. J. Wang ; K. S. M. Li ; T. Y. Ho</i> | |
| CHAIN-BASED PIN COUNT MINIMIZATION FOR GENERAL-PURPOSE DIGITAL MICROFLUIDIC BIOCHIPS..... | 599 |
| <i>Y. C. Lei ; C. S. Hsu ; J. D. Huang ; J. Y. Jou</i> | |
| A ROUTABILITY-DRIVEN FLOW ROUTING ALGORITHM FOR PROGRAMMABLE MICROFLUIDIC DEVICES..... | 605 |
| <i>Y. S. Su ; T. Y. Ho ; D. T. Lee</i> | |
| ADVANCED MULTI-PATTERNING AND HYBRID LITHOGRAPHY TECHNIQUES..... | 611 |
| <i>F. G. Pikus ; A. Torres</i> | |
| RECENT RESEARCH DEVELOPMENT AND NEW CHALLENGES IN ANALOG LAYOUT SYNTHESIS..... | 617 |
| <i>M. P. H. Lin ; Y. W. Chang ; C. M. Hung</i> | |
| TO DETECT, LOCATE, AND MASK HARDWARE TROJANS IN DIGITAL CIRCUITS BY REVERSE ENGINEERING AND FUNCTIONAL ECO | 623 |
| <i>X. Wei ; Y. Diao ; Y. L. Wu</i> | |
| AGING-AWARE HIGH-LEVEL PHYSICAL PLANNING FOR RECONFIGURABLE SYSTEMS..... | 631 |
| <i>Z. Ghaderi ; E. Bozorgzadeh</i> | |
| HARDWARE RELIABILITY MARGINING FOR THE DARK SILICON ERA | 637 |
| <i>L. Lai ; P. Gupta</i> | |
| ACR: ENABLING COMPUTATION REUSE FOR APPROXIMATE COMPUTING | 643 |
| <i>X. He ; G. Yan ; Y. Han ; X. Li</i> | |

| | |
|---|-----|
| WORK HARD, SLEEP WELL - AVOID IRREVERSIBLE IC WEAROUT WITH PROACTIVE REJUVENATION | 649 |
| <i>X. Guo ; M. R. Stan</i> | |
| NETLIST REVERSE ENGINEERING FOR HIGH-LEVEL FUNCTIONALITY RECONSTRUCTION | 655 |
| <i>T. Meade ; S. Zhang ; Y. Jin</i> | |
| ASSESSING CPA RESISTANCE OF AES WITH DIFFERENT FAULT TOLERANCE MECHANISMS | 661 |
| <i>H. Pahlevanzadeh ; J. Dofe ; Q. Yu</i> | |
| SPARTA: A SCHEDULING POLICY FOR THWARTING DIFFERENTIAL POWER ANALYSIS ATTACKS | 667 |
| <i>K. Jiang ; P. Eles ; Z. Peng ; S. Chattopadhyay ; L. Batina</i> | |
| LAPLACIAN EIGENMAPS AND BAYESIAN CLUSTERING BASED LAYOUT PATTERN SAMPLING AND ITS APPLICATIONS TO HOTSPOT DETECTION AND OPC | 679 |
| <i>T. Matsunawa ; B. Yu ; D. Z. Pan</i> | |
| BALANCING LIFETIME AND SOFT-ERROR RELIABILITY TO IMPROVE SYSTEM AVAILABILITY | 685 |
| <i>J. Zhou ; X. S. Hu ; Y. Ma ; T. Wei</i> | |
| A CLOSED-FORM STABILITY MODEL FOR CROSS-COUPLED INVERTERS OPERATING IN SUB-THRESHOLD VOLTAGE REGION | 691 |
| <i>T. Kamakari ; J. Shiomi ; T. Ishihara ; H. Onodera</i> | |
| DELAY UNCERTAINTY AND SIGNAL CRITICALITY DRIVEN ROUTING CHANNEL OPTIMIZATION FOR ADVANCED DRAM PRODUCTS | 697 |
| <i>S. Bang ; K. Han ; A. B. Kahng ; M. Luo</i> | |
| RELIABILITY, ADAPTABILITY AND FLEXIBILITY IN TIMING: BUY A LIFE INSURANCE FOR YOUR CIRCUITS | 705 |
| <i>U. Schlichtmann ; M. Hashimoto ; I. H. R. Jiang ; B. Li</i> | |
| A HIGH PERFORMANCE RELIABLE NOC E OUTER | 712 |
| <i>L. Wang ; S. Ma ; Z. Wang</i> | |
| DYNAMIC ADMISSION CONTROL FOR REAL-TIME NETWORKS-ON-CHIPS | 719 |
| <i>A. Kostrzewa ; S. Saidi ; L. Ecco ; R. Ernst</i> | |
| FOTONOC: A HIERARCHICAL MANAGEMENT STRATEGY BASED ON FOLDED LORUS-LIKE NETWORK-ON-CHIP FOR DARK SILICON MANY-CORE SYSTEMS | 725 |
| <i>L. Yang ; W. Liu ; W. Jiang ; M. Li ; J. Yi ; E. H. M. Sha</i> | |
| ANALYTICAL THRUPHIP INDUCTIVE COUPLING CHANNEL DESIGN OPTIMIZATION | 731 |
| <i>L. C. Hsu ; J. Kadomoto ; S. Hasegawa ; A. Kosuge ; Y. Take ; T. Kuroda</i> | |
| EXTENDING TRACE HISTORY THROUGH TAPERED SUMMARIES IN POST-SILICON VALIDATION | 737 |
| <i>S. Chandran ; P. R. Panda ; D. Chauhan ; S. Kumar ; S. R. Sarangi</i> | |
| NOVEL APPLICATIONS OF DEEP LEARNING HIDDEN FEATURES FOR ADAPTIVE TESTING | 743 |
| <i>B. Xiao ; J. Xiong ; Y. Shi</i> | |
| MIXED 01X-RSL-ENCODING FOR FAST AND ACCURATE ATPG WITH UNKNOWNNS | 749 |
| <i>D. Erb ; K. Scheibler ; M. A. Kochte ; M. Sauer ; H. J. Wunderlich ; B. Becker</i> | |
| TEST AND DIAGNOSIS PATTERN GENERATION FOR DYNAMIC BRIDGING FAULTS AND TRANSITION DELAY FAULTS | 755 |
| <i>C. H. Wu ; S. J. Lee ; K. J. Lee</i> | |
| FLEXIBLE TRANSITION METAL DICHALCOGENIDE FIELD-EFFECT TRANSISTORS: A CIRCUIT-LEVEL SIMULATION STUDY OF DELAY AND POWER UNDER BENDING, PROCESS VARIATION, AND SCALING | 761 |
| <i>Y. Y. Chen ; M. Gholipour ; D. Chen</i> | |
| NON-VOLATILE NON-SHADOW FLIP-FLOP USING SPIN ORBIT TORQUE FOR EFFICIENT NORMALLY-OFF COMPUTING | 769 |
| <i>R. Bishnoi ; F. Oboril ; M. B. Tahoori</i> | |
| OPTIMAL CO-SCHEDULING OF HVAC CONTROL AND BATTERY MANAGEMENT FOR ENERGY-EFFICIENT BUILDINGS CONSIDERING STATE-OF-HEALTH DEGRADATION | 775 |
| <i>T. Cui ; S. Chen ; Y. Wang ; Q. Zhu ; S. Nazarian ; M. Pedram</i> | |
| ACCURATE REMAINING RANGE ESTIMATION FOR ELECTRIC VEHICLES | 781 |
| <i>J. Hong ; S. Park ; N. Chang</i> | |
| Author Index | |