

2015 IEEE International Integrated Reliability Workshop (IIRW 2015)

**South Lake Tahoe, California, USA
11-15 October 2015**



**IEEE Catalog Number: CFP15IRW-POD
ISBN: 978-1-4673-7397-5**

**Copyright © 2015 by the Institute of Electrical and Electronic Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

******This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP15IRW-POD
ISBN (Print-On-Demand):	978-1-4673-7397-5
ISBN (Online):	978-1-4673-7396-8
ISSN:	1930-8841

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

contents

Foreword by J. Ryan	vii
Keynote address by Prasad Chaparala, "Defining reliability specifications for consumer electronic devices" [abstract]	ix

PLATFORM TECHNICAL PRESENTATIONS

Session 1 — Special Topics

(Invited) Engineering the Performance of MIM Tunnel Diodes and Capacitors with ALD Nanolaminated Bilayer Insulators [abstract] <i>John Conley</i>	1
--	---

(Invited) Defect Limited Reliability and Transport in Carbon Nanotube and Graphene Devices [abstract] <i>David Estrada</i>	2
---	---

Session 2 — Non-volatile Memories

(Invited) Solid-State-Drive (SSD) Qualification and Reliability Strategy <i>Todd Marquart</i>	3
--	---

(Invited) Reliability Challenges in Resistive Switching Memories Technology <i>Shweta Deora</i>	7
--	---

Investigation of the Reliability Degradation of Scaled SONOS Memory Transistors <i>J. Ocker, S. Slesazeck, R. Hoffmann, V. Beyer, A. Skouris, R. Srowik, S. Buschbeck, S. Günther, T. Mikolajick</i>	13
---	----

Advanced 1T1R Test Vehicle for RRAM Nanosecond-range Switching-time Resolution and Reliability Assessment <i>Clément Nguyen, Carlo Cagli, Elisa Vianello, Alain Persico, Gabriel Molas, Gilles Reimbold, Quentin Rafhay, Gérard Ghibaudo</i>	17
---	----

Session 3 — Random Telegraph Noise

(Invited) Defect-centric perspective for combined RTN and BTI time-dependent variability <i>Pieter Weckx, B. Kaczer, J. Franco, Ph. J. Roussel, E. Bury, A. Subirats, G. Groeseneken, F. Catthoor, D. Linten, P. Raghavan, A. Thean</i>	21
--	----

Further Understandings on Impacts of La incorporation in HfSiON/TiN nFETs Through Comprehensive Random Telegraph Noise Characterizations <i>Jiezhi Chen, Yuichiro Mitani</i>	29
---	----

Session 4 Late News I

(Late News) Effect of Dielectric Thickness and Annealing on Threshold Voltage Instability of Low Temperature Deposited High-k Oxides on ZnO TFTs <i>C. D. Young, R. Campbell, S. Daasa, S. Benton, R. Rodriguez Davila, I. Mejia, M. Quevedo-Lopez</i>	34
---	----

Session 5 III-V

(Invited) Oxide Defects and Reliability of High K/Ge and III-V based Gate Stacks <i>John Robertson, Yuzheng Guo</i>	37
--	----

Charge Feedback Mechanisms at Forward Threshold Voltage Stress in GaN/AlGaN HEMTs <i>A. Grill, G. Rzepa, P. Lagger, C. Ostermaier, Hajdin Ceric, T. Grasser</i>	41
--	----

Extraction of interface and border traps in beyond-Si devices by accounting for generation and recombination in the semiconductor <i>Gabriele Sereni, Luca Larcher</i>	46
---	----

Session 6 BEOL

(Invited) A Sampling Approach for Efficient BEOL TDDB Assessment <i>Andrew Kim, Cathryn Christiansen, Baozhen Li, Ernest Wu, Paul McLaughlin</i>	52
---	----

Session 7 Si MOSFET Reliability

(Invited) Aging Model Challenges in Deeply Scaled Tri-gate Technologies <i>S. Ramey, Y. Lu, I. Meric, S. Mudanai, S. Novak, C. Prasad, J. Hicks</i>	56
(Invited) Reliability Aging and Modeling of Chip-Package Interaction on Logic Technologies Featuring High-k Metal Gate Planar and FinFET Transistors <i>Jen-Hao Lee, Eliot S.H. Chen, Yung-Huei Lee, Chun-Hung Lin, Chun-Yu Wu, Ming-Han Hsieh, Kevin Huang, Jhong-Sheng Wang, Yung-Sheng Tsai, Ryan Lu, and Jiaw-Ren Shih</i>	63
(Invited) From WLR to Product Reliability and Qualifications in the 3D Transistor Era [abstract] <i>Sangwoo Pae.....</i>	68

Novel Charge Pumping Method Applied to Tri-Gate MOSFETs for Reliability Characterization <i>B. Bittel, S. Novak, S. Ramey, S. Padiyar, J.T. Ryan, J.P. Campbell, K.P. Cheung</i>	69
---	----

Session 8 Large statistics

Advanced MOSFET variability and reliability characterization array <i>M. Simicic, V. Putcha, B. Parvais, P. Weckx, B. Kaczer, G. Groeseneken, G. Gielen, D. Linten, A. Thean</i>	73
Wafer Level Test Arrays with Simple BIST to Expedite Process Development for Circuit Reliability <i>M.-H. Hsieh, T.-Y. Yew, Y.-C. Huang, Y.C. Wang, W. Wang, Y.-H. Lee, J.H. Lee</i>	77
Influence of MOSFET geometry on the statistical distribution of NBTI induced parameter degradation <i>Christian Schlünder, Fabian Proebster, Jörg Berthold, Wolfgang Gustin, Hans Reisinger</i>	81
Comparison between recoverable and permanent NBTI variability components <i>D.Nouguier, M. Rafik, X. Federspiel, G. Ghibaudo</i>	87
Massively Parallel TDDB testing : SiC Power devices <i>Z. Chbili, J. Chbili, J. P. Campbell, J. T. Ryan, M. Lahbab, D. E. Ioannou, K. P. Cheung</i>	91

Session 9 Late News II

(Late News)Smart-array for pipelined BTI characterization <i>Vamsi Putcha, Marko Simicic, Pieter Weckx, Bertrand Parvais, Jacopo Franco, Ben Kaczer, Dimitri Linten, Diederik Verkest, Aaron Thean, Guido Groeseneken</i>	95
(Late News) Field-Induced Generation of Electron Traps in the Tunnel Oxide of Flash Memory Cells <i>Yuri Tkachev</i>	99

POSTER PRESENTATIONS—REFEREED

Study of the impact of dielectric aging on coplanar waveguide performance <i>A.P. Nguyen, U. Lüders, F. Voiron</i>	103
Comparison of random telegraph noise, endurance and reliability in amorphous and crystalline hafnia-based ReRAM <i>K. Beckmann, J. Holt, N. Cady, J. Nostrand</i>	107
Polysilicon Resistor Degradation – Modeling and Mechanism <i>S. Jayanarayanan</i>	111
The Strength of BEOL Structures Fabricated using Low K Materials and its Impact on CPI Failures <i>T.M. Shaw, X-H Liu, E. Misra, D. Questad, G. Bonilla, T. Wassick, M. Lamorey, H. Shobha, G. Osborne, D. Kioussis, J. Wright, R. Bisson, I. Paquin, S.S. Bouchard, S. Tetreault, D. Stone, C. Muzzy, B. Sundløf, T. Daubenspeck</i>	115
Relaxation-free Characterization of Flash Programming Dynamics along P-E Cycling <i>J. Coignus, A. Vernhet, G. Torrente, S. Renard, D. Roy, G. Reimbold</i>	119
Using the charge pumping geometric component to extract NBTI induced mobility degradation <i>M. Boubaaya, H. Tahi, C. Tahanout, B. Djezzar, A. Benabdelmomene, A. Chenouf, D. Doumaz, A. Feraht Hemida</i>	122
Charge-based Stochastic Aging Analysis of CMOS Circuits <i>T. Hillebrand, N. Hellwege, N. Heidmann, S. Paul, and D. Peters-Drolshagen</i>	126
Memory Yield and Lifetime Estimation Considering Aging Errors <i>D-H Kim, L. S. Milor</i>	130

Hot Carrier Stress modeling: from degradation kinetics to trap distribution evolution <i>G. Torrente, X. Federspiel, D. Rideau, F. Monsieur, C. Tavernier, J. Coignus, D. Roy, G. Ghibaudo</i>	134
Combined Vramp and TDDB Analysis for Gate Oxide Reliability Assessment and Screening <i>T. Kopley, M. Ring, C. Choi, J. Colbath</i>	138
On the Temperature Behavior of Hot-Carrier Degradation <i>S. Tyaginov, M. Jech, P. Sharma, J. Franco, B. Kaczer, T. Grasser</i>	143

POSTER PRESENTATIONS—OPEN

NBTI Stress on power VDMOS Transistors under Low Magnetic Field <i>C. Tahanout, H. Tahi, M. Boubaaya , B. Djezzar, M. Marah, B. Nadji, N. Saoula</i>	147
Decay of magnetoresistance in a low-k dielectric upon application of electrical bias and temperature stress <i>B. McGowan , A. Kennedy, J. Lloyd</i>	151
Radiation Testing of Tantalum Oxide-based Resistive Memory <i>J. Holt, J. Yang-Scharlotta, N. Cady</i>	155

Tutorials

AgELESS: Aging Estimation and Lifetime Enhancement in Silicon Systems [abstract] <i>Sachin Sapatnekar</i>	159
Ionizing Radiation Effects in Electronic Devices with an Emphasis on Non-volatile Memories [abstract] <i>Marta Bagatin</i>	159
Modeling of Hot-carrier Degradation in GaN Transistors [abstract] <i>Yevgeniy S. Puzyrev</i>	160
FinFET Reliability [abstract] <i>Suresh Uppal</i>	160
Modeling and Characterization of Hot-Carrier Stress Degradation in Power MOSFETs [abstract] <i>Susanna Reggiani</i>	161
Nanoscopic techniques for studying dielectric breakdown and switching induced morphological changes and defects[abstract] <i>Kin-Leong Pey</i>	161

Discussion Group (DG) Summaries

RRAM Reliability, FinFET Reliability, Resilient Integrated Systems, Semiconductor integration for Automotive needs, Physics-based reliability models, SSD Reliability	162
--	-----

BIOGRAPHIES	175
PICTURES	179