

2016 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSIOI-ULIS 2016)

**Wien, Vienna, Austria
25 – 27 January 2016**



**IEEE Catalog Number: CFP1649D-POD
ISBN: 978-1-4673-8610-4**

**Copyright © 2016 by the Institute of Electrical and Electronic Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

******This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP1649D-POD
ISBN (Print-On-Demand):	978-1-4673-8610-4
ISBN (Online):	978-1-4673-8609-8

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2016 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon

Session I: SOI for Low Power and Sensors

Strain-Engineering for Improved Tunneling in Reconfigurable Silicon Nanowire Transistors <i>T. Baldauf, A. Heinzig, T. Mikolajick, J. Trommer, and W.M. Weber</i>	1
Reconfigurable Field Effect Transistor for Advanced CMOS: A Comparison with FDSOI Devices <i>C. Navarro, S. Barraud, S. Martinie, J. Lacord, M.-A. Jaud, and M. Vinet</i>	5

Session II: Tunnel FETs

III-V-based Hetero Tunnel FETs: A Simulation Study with Focus on Non-ideality Effects (invited) <i>A. Schenk, S. Sant, K. Moselund, and H. Riel</i>	9
Intrinsic Voltage Gain of Line-TFETs and Comparison with Other TFET and MOSFET Architectures <i>P. G. D. Agopian, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, A. Thean, and C. Claeys</i>	13
Optimization of GaSb/InAs TFET Exploiting Different Strain Configurations <i>M. Visciarelli, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani</i>	16
Assessment of Confinement-Induced Band-to-Band Tunneling Leakage in the FinEHBTFET <i>J. L. Padilla, C. Alper, F. Gámiz, and A.M. Ionescu</i>	20

Session III: Semiconductor Processing

Process Modules for GeSn Nanoelectronics with High Sn-contents <i>C. Schulte-Braucks, S. Glass, E. Hofmann, D. Stange, N. von den Driesch, Q.T. Zhao, D. Buca, S. Mantl, J.M. Hartmann, and Z. Ikonic</i>	24
Controlling the Physical and Electrical Properties of ALD Grown ZnO using Nb as a Dopant <i>A. Shaw, J. D. Jin, I. Z. Mitrovic, S. Hall, J. S. Wrench, and P. R. Chalker</i>	28
Single-electron Transistors featuring Silicon Nitride Tunnel Barriers prepared by Atomic Layer Deposition <i>G. Karbasian, A.O. Orlov, A.S. Mukasyan, and G.L. Snider</i>	32
On the Scaling of Lanthanum Oxide Gate Dielectric Film into the Subnanometer EOT Range <i>H. Wong, J. Zhang, X. Feng, D. Yu, H. Iwai, and K. Kakushima</i>	36

Session IV: Frequency Phenomena and Noise

Electrical Characterization of Random Telegraph Noise in Back-Biased Ultrathin Silicon-On-Insulator MOSFETs <i>C. Marquez, N. Rodriguez, F. Gámiz, and A. Ohata</i>	40
1/f -Noise Characteristics of AlGaIn/GaN Omega Shaped Nanowire FETs <i>S. Vodapally, C.-H. Won, I.-T. Cho, J.-H. Lee, Y. Bae, S. Cristoloveanu, K.-S. Im, and Ju.-H. Lee</i> ...	44
Simulation of Plasma Resonances in MOSFETs for THz-Signal Detection <i>C. Jungemann, K. Bittner, and H. G. Brachtendorf</i>	48

Session V: Modeling 1

Scaling/LER Study of Si GAA Nanowire FET using 3D Finite Element Monte Carlo Simulations <i>M.A. Elmessary, D. Nagy, M. Aldegunde, N. Seoane, G. Indalecio, J. Lindberg, W. Dettmer, D. Perić, A. J. García-Loureiro, and K. Kalna</i>	52
Simulation Analysis of the Electro-Thermal Performance of SOI FinFETs <i>L. Wang, T. Sadi, A. R. Brown, M. Nedjalkov, C. Alexander, B. Cheng, C. Millar, and A. Asenov</i>	56
Space-Average Impurity-Limited Resistance and Self-Averaging in Quasi-1D Nanowires <i>N. Sano</i>	60
Numerical Analysis and Analytical Modeling of RDF in DG Tunnel-FETs <i>M. Graef, F. Hain, F. Hosenfeld, F. Horst, A. Farokhnejad, B. Iñiguez, and A. Kloes</i>	64

Session VI: Advanced Memory

Capacitor-less Memory: Advances and Challenges (invited) <i>F. Gámiz</i>	68
Inverse-magnetostriction-induced Switching Current Reduction of STT-MTJs and its Application for Low-voltage MRAMs <i>Y. Takamura, Y. Shuto, S. Yamamoto, H. Funakubo, M.K. Kurosawa, S. Nakagawa, and S. Sugahara</i>	72
A Consistent Picture of Cycling Dispersion of Resistive States in HfO_x Resistive Random Access Memory <i>F.M. Puglisi and P. Pavan</i>	76
Performance and Reliability Comparison of 1T-1R RRAM Arrays with Amorphous and Polycrystalline HfO₂ <i>A. Grossi, E. Perez, C. Zambelli, P. Olivo, and C. Wenger</i>	80
Intra-device Statistical Parameters in Variability-aware Modelling of Resistive Switching Devices <i>A. Crespo-Yepes, J. Martin-Martinez, I. Rama, M. Maestro, R. Rodriguez, M. Nafria, X. Aymerich, M. B. Gonzalez, and F. Campabadal</i>	84

Session VII: Design, Characterization, and Performance

Impact of the Design Layout on Threshold Voltage in SiGe Channel UTBB-FDSOI pMOSFET <i>R. Berthelon, F. Andrieu, S. Ortolland, R. Nicolas, T. Poiroux, E. Baylac, D. Dutartre, E. Josse, A. Claverie, and M. Haond</i>	88
Drain Current Local Variability from Linear to Saturation Region in 28nm Bulk NMOSFETs <i>T. A. Karatsori, C. G. Theodorou, S. Haendler, C. A. Dimitriadis, and G. Ghibaudo</i>	92
Investigation of BSIM4 Parameter Extraction and Characterization for Multi Gate Oxide-Dual Work Function (MGO-DWF)-MOSFET <i>C. Tanaka, K. Matsuzawa, T. Miyata, K. Adachi, and A. Hokazono</i>	96
Confinement Orientation Effects in S/D Tunneling <i>C. Medina-Bailon, C. Sampedro, F. Gámiz, A. Godoy, and L. Donetti</i>	100
Volume and Interface Conduction in InGaAs Junctionless Transistors <i>L. Pirro, H. J. Park, I. Ionica, M. Bawedin, S. Cristoloveanu, L. Czornomaz, V. Djara, and V. Deshpande</i>	104

Session VIII: Modeling 2

VDD Scaling of Ultra-thin InAs MOSFETs: A full-quantum Study <i>C. Grillet and M. Pala</i>	108
Contact Resistances in Trigate Devices in a Non-Equilibrium Green's Functions Framework <i>L. Bourdet, J. Li, J. Pelloux-Prayer, F. Triozon, M. Cassé, S. Barraud, S. Martinie, D. Rideau, and Y.-M. Niquet</i>	112
Analysis and Modelling of Temperature Effect on DIBL in UTBB FD SOI MOSFETs <i>A. S. N. Pereira, G. de Streel, N. Planes, M. Haond, R. Giacomini, D. Flandre, and V. Kilchytska</i>	116
Using One-dimensional Radiosity to Model Neutral Particle Flux in High Aspect Ratio Holes <i>P. Manstetten, L. Filipovic, A. Hössinger, J. Weinbub, and S. Selberherr</i>	120

Session IX: Advanced Devices and Three-Dimensional Integration

SOI Platform for Spin Qubits (invited) <i>S. De Franceschi, R. Maurand, A. Corna, D. Kotekar-Patil, X. Jehl, M. Sanquer, R. Lavieville, L. Hutin, S. Barraud, M. Vinet, and Y.-M. Niquet</i>	124
First RF Characterization of InGaAs Replacement Metal Gate (RMG) nFETs on SiGe-OI FinFETs Fabricated by 3D Monolithic Integration <i>V. Deshpande, V. Djara, E. O'Connor, D. Caimi, M. Sousa, L. Czornomaz, J. Fompeyrine, P. Hashemi, and K. Balakrishnan</i>	127
A Sharp-Switching Gateless Device (Z3-FET) in Advanced FDSOI Technology <i>H. El Dirani, Y. Solaro, P. Fonteneau, C. A Legrand, D. Marin-Cudraz, D. Golanski, P. Ferrari, and S. Cristoloveanu</i>	131

Session X: End of Scaling and Beyond CMOS

Robust EOT and Effective Work Function Extraction for 14 nm Node FDSOI Technology <i>B. Mohamad, C. Leroux, D. Rideau, M. Haond, G. Reimbold, and G. Ghibaudo</i>	135
Benchmarks of a III-V TFET Technology Platform against the 10-nm CMOS Technology node Considering 28T Full-Adders <i>S. Strangio, P. Palestri, M. Lanuzza, D. Esseni, F. Crupi, and L. Selmi</i>	139
Improved Voltage Gain in Mechanically Stacked Bilayer Graphene Field Effect Transistors <i>H. Pandey, S. Kataria, V. Passi, M. Iannazzo, E. Alarcon, and M.C. Lemme</i>	143
Simulation Study on the Feasibility of Si as Material for Ultra-Scaled Nanowire Field-Effect Transistors <i>Z. Stanojevic, O. Baumgartner, M. Karner, F. Mitterbauer, H. Demel, and C. Kernstock</i>	147

Session XI: Advanced Devices

GDNMOS: A New High Voltage Device for ESD Protection in 28nm UTBB FD-SOI Technology <i>S. Athanasiou, C.-A. Legrand, S. Cristoloveanu, and Ph.Galy</i>	151
Operation of Suspended Lateral SOI PIN Photodiode with Aluminum Back Gate <i>G. Li, N. André, O. Poncelet, P. Gérard, S. Zeeshan Ali, F. Udrea, L.A. Francis, Y. Zeng, and D. Flandre</i>	155
RF SOI CMOS Technology on 1st and 2nd Generation Trap-Rich High Resistivity SOI Wafers <i>B. Kazemi Esfeh, V. Kilchytska, D. Flandre, and J.-P. Raskin</i>	159
Effective Hole Mobility and Low-Frequency Noise Characterization of Ge pFinFETs <i>A.V. Oliveira, P. G. D. Agopian, J. A. Martino, E. Simoen, J. Mitard, L. Witters, R. Langer, N. Collaert, C. Claeys, and A. Thean</i>	162

Session XII: Posters

A Novel 3D Pixel Concept for Geiger-mode Detection in SOI Technology <i>M. M. Vignetti, F. Calmon, P. Lesieur, F. Dubois, T. Graziosi, and A. Savoy-Navarro</i>	166
Analog Performance of n- and p-FET SOI Nanowires Including Channel Length and Temperature Influence <i>B.C. Paz, M.A. Pavanello, M. Cassé, S. Barraud, G. Reimbold, M. Vinet, and O. Faynot</i>	170
Body Factor Scaling in UTBB SOI with Supercoupling Effect <i>K.R.A.Sasaki, J.A.Martino, C.Navarro, M.Bawedin, F. Andrieu, and S.Cristoloveanu</i>	174
Current Mirrors with Strained Si Single Nanowire Gate All Around Schottky Barrier MOSFETs <i>K. Narimani, G. V. Luong, C. Schulte-Braucks, S. Trelenkamp, Q.T. Zhao, S. Mantl, and M. F. Chowdhury</i>	178

A Method for Combined Characterization of MOSFET Threshold Voltage and Junction Capacitance Eliminating Channel Current Effect <i>D. Tomaszewski, G. Gluszek, and J. Malesińska</i>	182
Gated SiGe PIN Diodes Exposed to Visible Light Spectrum and Heavy-Ion Radiation <i>R. T. Bühler, C. D. Novo, M. A. G. Silveira, and R. Giacomini</i>	186
Recrystallization and Oxidation - Competing Processes during PECVD Ultrathin Silicon Layer High Temperature Annealing <i>R.B. Beck and K. Ber</i>	190
Effect of Inner Interface Traps on High-K Gate Stack Admittance Characteristics <i>A. Mazurak, J. Jasiński, and B. Majkusiak</i>	194
Comparative Study of Vertical GAA TFETs and GAA MOSFETs in Function of the Inversion Coefficient <i>V. B. Sivieri, P. G. D. Agopian, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, A. Thean, and C. Claeys</i>	198
Influence of Spin Relaxation on Trap-assisted Resonant Tunneling in Ferromagnet-Oxide-Semiconductor Structures <i>V. Sverdlov and S. Selberherr</i>	202
Modeling Heat Dissipation in an SOI Device - Finite Element Analysis at Semiconductor Die Level <i>George P. Hosey</i>	206
Conductivity Type Switching in Semiconductor Nanowires <i>A. Yesayan, S. Petrosyan, and F. Prégaldiny</i>	210
Fabrication and Characterization of InGaAs-on-insulator Lateral N+/n/N+ Structures <i>L. Czornomaz, V. Djara, V. Deshpande, D. Caimi, L. Pirro, S. Cristoloveanu, and J. Fompeyrine</i> .	214
Enhancing Electrical Performances of Metallic DG-SET based Circuits by Tunnel Junction Engineering <i>K.G. El Hajjam, M.A. Bounouar, D. Drouin, and F. Calmon</i>	218
Transient Second Harmonic Generation and Correlation with Ψ-MOSFET in SOI Wafers <i>D. Damianos, I. Ionica, A. Kaminski-Cachopo, G. Vitrant, S. Cristoloveanu D. Blanc Pelissie, M. Kryger, and J. Changala</i>	222
Direction Dependent Three-Dimensional Silicon Carbide Oxidation Growth Rate Calculations <i>V. Šimonka, G. Nawratil, A. Hössinger, J. Weinbub, and S. Selberherr</i>	226
On the Influence of the Back-gate Bias on InGaAs Trigate MOSFETs <i>E.G. Marin, F.G. Ruiz, A. Godoy, J.M. Gonzalez-Medina, I. M. Tienda-Luna, A. Toral, and F. Gámiz</i>	230
Influence of Quantum Confinement Effects and Device Electrostatic Driven Performance in Ultra-scaled Si_xGe_{1-x} Nanowire Transistors <i>Talib Al-Ameri, V. P. Georgiev, F. Adamu-Lema, X. Wang, and A. Asenov</i>	234
Scanning Microwave Microscopy for Non-Destructive Characterization of SOI Wafers <i>L. Michalas, I. Ionica, E. Brinciotti, L. Pirro, F. Kienberger, S. Cristoloveanu, and R. Marcelli</i>	238

Influence of the Ge Amount at Source on Transistor Efficiency of Vertical Gate All Around TFET for Different Conduction Regimes

C. C. M. Bordallo, V. B. Sivieri, J. A. Martino, P. G. D. Agopian, R. Rooyackers, A. Vandooren, E. Simoen, A. Thean, and C. Claeys 242

Analysis of TFET and FinFET Differential Pairs with Active Load from 300K to 450K

M.D.V. Martino, J.A. Martino, and P.G D. Agopian 246

Numerical Simulation of Gunn Oscillation in AlGaAs/InGaAs High-Electron Mobility Transistor

S.-M. Hong and J.-H. Jang 250

Metal-Graphene Contact Capacitance

A.M. Slobodyan, S.I. Tiagulskiy, Yu.V. Gomeniuk, and A.N. Nazarov 254