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Detailed Technical Program

Day 2 – November 28, 2015

09.30 – 10.30 : Inaugural Session

10.30 – 10.45 : Tea Break

10.45 – 11.45 : Plenary Talk by Pramod Kumar Meher

11.45 – 13.15 : SESSION A

Track: VLSI for Digital Communication Systems

Session Co – Chairs: Pramod K Meher and P.V. Ananda Mohan

Time	Paper	Title/Author
11.45 – 12.00	A1	1.2 mW 2.4GHz PLL for ZigBee and BLE standard in Single-Well 0.18um CMOS with efficient divider architecture (ID :18) Purushothama Chary P, Rizwan Shaik Peerla, Sesha Sairam Renulagadda, Mohd Abdul Naseeb, Amit Acharyya, Rajalakshmi P, Ashudeb Dutta (IIT, Hyderabad), Debashis Mandal (Arizona State University)
12.00 – 12.15	A2	Noise Figure Analysis of 2.5 GHz Folded Cascode LNA using High-Q Layout Optimized Inductors (ID:103) Shashank, Jayanta Mukherjee (IIT, Bombay), Venkata Narayana Rao Vanukuru (Global Foundries, Bangalore)
12.15 – 12.30	A3	Design of Current Reuse based Differential Merged LNA-Mixer (DMLNAM) and Two-stage Dual Band LNA with two Gain modes in 65nm technology(ID : 104) Ganesh Lakshmana Kumar M, Sesha Sairam (IIT, Hyderabad), Jitendra Kumar Das (KIIT University), Ashudeb Dutta (IIT, Hyderabad)
12.30 – 12.45	A4	Solar-powered spike-based communication system with analog back scatter (ID: 121) Javed S Gaggatur, Manjunath Machnoor (IISc, Bangalore)
12.45 – 13.00	A5	DCT and CORDIC on a Novel Configurable Hardware (ID:066) Nupur Jain, Biswajit Mishra (DhirubhaiAmbani Institute of Information and Communication Technology)
13.00 – 13.15	A6	Implementation of Turbo codes using Verilog-VHDL and estimation of its error correction capability.(094) Tepoju Vivek Vardhan, Bandi Neeraja (CBIT), Boya Pradeep Kumar, Chandra Sekhar Paidimarry (Osmania University)

13.15 – 14.00 : Lunch

Day 2 – November 28, 2015

14.00 – 15.00 : Plenary Talk by Ravinder Dahiya

15.00 – 15.45 : Session B

Analog to Digital Converters

Session Co - Chairs: Ravinder Dahiya and P.A. Govindacharyulu

Time	Paper	Title/Author
15.00 – 15.15	B1	A 43-nW 10-bit 1-KS/s SAR ADC in 180nm CMOS for Biomedical Application (ID:037) Kunal Yadav, Pravanjan Patra, Ashudeb Dutta (IITH)
15.15 – 15.30	B2	A Design of 2nd Order Discrete-Time Sigma-Delta Modulator For Medical Implants(ID: 007) M A Raheem (Muffakham Jah College of Engineering and Technology), K. Manjunatha Chari (GITAM University), Mohammed Arifuddin Sohel, M A Mushahhid Majeed (Muffakham Jah College of Engineering and Technology).
15.30 – 15.45	B3	A Low Hardware Complexity Time Domian Quantizer for Wideband Multibit ΣΔ ADCs.(ID:114) Pankaj Jha, Pravanjan Patra, Ashudeb Dutta (IITH)

15.45 – 16.00 : Tea Break

16.00 – 17.15 : Session C

Analog Circuits

Session Co - Chairs: M.B. Srinivas and A.G. Krishna Kanth

Time	Paper	Title/Author
16.00 – 16.15	C1	Current Mode Biquadratic Universal Filter (ID:049) Ajay Kumar Kushwaha, Sajal K. Paul (Indian School of Mines, Dhanbad)
16.15 – 16.30	C2	A novel FPGA based digital octa-rate clock and data recovery circuit(ID:087) Burugula Sai Sankalp (CBIT), Boya Pradeep Kumar, Chandra Sekhar Paidimarry (Osmania University), Jagan Mohan Reddy N (CBIT)
16.30 – 16.45	C3	Stimulation driver circuits for non-rectangular stimuli in biomedical implants (ID:118) Rathna C (Anna University, Chennai)
16.45 – 17.00	C4	Charge Pump Circuit with Improved Absolute Current Deviation and Increased Dynamic Output Voltage Range across PVT variations(ID: 039) Suraj Gupta, Sabir Ali Mondal, Hafiz ur Rahman (IIEST, Shibpur, Howrah)
17.00 – 17.15	C5	Design and simulation of Programmable Band-gap Reference circuit(ID:093) Mohd Ziauddin Jahangir (CBIT), Chandra Shekhar Paidimarry (Osmania University), N.V Koteswara Rao (CBIT).

Technical Program

Day 3 - November 29, 2015

9.30 – 10.15 : Session D

Session Co - Chairs: P. Chandrashekhar and Mohammed Arifuddin Sohel

Time	Paper	Title/Author
9.30 – 9.45	D1	A Novel Control Strategy for Cascaded Multilevel Converter based STATCOM(ID: 45) Ch. Lokeshwar Reddy (CVR College of Engineering), M. Sushama (JNTU College of Engineering), P. Satish Kumar (Osmania University), N.N.V. Surendra Babu (CVR College of Engineering).
9.45 – 10.00	D2	A Comparative Study on Single Phase TCR Reactive Power Compensator(ID:117) Mohammed Imran, Shafeen Azeez (MJCET)
10.00 – 10.15	D3	Modeling and Design of 700W Digital Average Current Mode Controlled Multiphase Bidirectional DC-DC Converter (ID:135) Suryanarayana K(NMAM Institute of Technology, Nitte), H N Nagaraja (Noble Group of Institutions, Junagadh)

10.15 – 11.15 : Keynote Talk

Title: Future Research in Avionics for Defence Applications
Speaker: B. H. V. S. Narayana Murthy

11.15 - 11.30 : Tea Break

Technical Program

Day 3 - November 29, 2015

11.30 – 13.00 : Session E

Logic Circuits & Memories

Session Co - Chairs: Hanuma Sai and Kaleem Fatima

Time	Paper	Title/Author
11.30 – 11.45	E1	Characterization of BE-SONOS Flash Memory using Rare-Earth Materials in Tunnel Barrier with Improved Memory Dynamics(ID: 003) Mansimran Kaur, Vaibhav Neem,(Institute of Engineering and Technology Indore),Deepika Gupta, Vikas Vijayvargiya, Santosh kumar Vishvakarma (IIT Indore)
11.45 – 12.00	E2	Tunnel Transistors with Circuit Co-Design in Designing Reliable Logic Gates for Energy Efficient Computing(ID: 098) Sadulla Shaik (VFSTR University, AP), K. Sri Rama Krishna (V.R. Siddhartha Engg. College, AP), Ramesh Vaddi (IIIT, Naya Raipur)
12.00 – 12.15	E3	Ultra-Low Power 128 byte Memory Design based on D-latch in 0.18 _m process (ID: 100) Saurabh Tripathi, Nupur Jain, Biswajit Mishra, (Dhirubhai Ambani Institute of Information and Communication Technology, Gujarat)
12.15 – 12.30	E4	Design and Implementation of 15-4 compressor using 1-bit semi domino full adder at 28nm Technology (ID -38) G. Raju, S. Aruna (MVSR Engineering College), G. Ranjith Kumar (SM Silicon India Pvt. Ltd.), S. Vasu Krishna (Geethanjali College of Engineering & Technology)
12.30 – 12.45	E5	A comparative study of 6T-SRAM Cell designed using Symmetrical Double Gate MOSFET and Symmetrical Double Gate Ferroelectric FET (ID- 058) Mulaka Haranadha Reddy, Srivatsava Jandhyala (IIIT, Hyderabad).
12.45 – 13.00	E6	An Area Efficient Q-format Multiplier with High Performance for Digital Processing Applications (ID- 131) Vaddempudi Koteswara Rao, Karnati Lavanya (QIS Institute of Technology, A.P)

13.00 – 14.00 : Lunch

Technical Program

Day 3 - November 29, 2015

14.00 – 15.00 : Keynote Talk – Title: Technology -Safe Society, Speaker: Rajesh Kumar

15.00 – 15.45 : Session F

Session Co - Chairs: K. Jayashankarand Dhiraj Sunehra

Time	Paper	Title/Author
15.00 – 15.15	F1	Clutter reduction using Background Subtraction of Ground Penetrating Radar for Landmine Detection(ID: 012) Smitha N, Vipula Singh (RNS Institute of Technology, Banglore)
15.15 – 15.30	F2	H-shaped microstrip antenna for broadband communications at 60GHz(ID:095) A. Mehta, R. Ramer, L. Gong(The University of South Wales, Sydney, Australia), S. Sachdeva (ITM University, Gurgaon)
15.30 – 15.45	F3	Verilog Implementation of Adaptive Compression of RGB images at low bit rates (ID:124) Arjun T V, Pranose J Edavoor, Sithara Raveendran, Sumesh K P, Nithin Kumar Y. B, Vasantha M.H (NIT, Goa)
15.45 – 16.00	F4	Radiation Hardened High Resolution Timing Generator (ID- 115) S Balaji, Loyola – IACM College of Engineering and Technology, (LICET) Chennai
16.00 – 16.15	F5	An Improved Block Based EZW Technique for Low Dynamic Range Image Compression(ID – 90) Naveen Cheggoju; Vishal Ramesh Satpute; Avinash Keskar, VNIT Nagpur

16.15 – 16.30: Tea Break

16.30 – 17.00: Valedictory Session