

2016 International Conference on Microelectronic Test Structures (ICMTS 2016)

**Yokohama, Japan
28 – 31 March 2016**



**IEEE Catalog Number: CFP16MTS-POD
ISBN: 978-1-4673-8794-1**

**Copyright © 2016 by the Institute of Electrical and Electronic Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

******This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16MTS-POD
ISBN (Print-On-Demand):	978-1-4673-8794-1
ISBN (Online):	978-1-4673-8793-4
ISSN:	1071-9032

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

SESSION 1: MEMS and Sensors

2016 March 29, 9:00 – 10: 20

Co-Chairs: Stewart Smith, *The University of Edinburgh, UK*

- 9:00 An Efficient Method to Evaluate 4 million Micro-bump Interconnection Resistances for**
1.1 3D Stacked 16-Mpixel Image Sensor 2
Yoshiaki Takemoto, Hideki Kato, Toru Kondo, Naohiro Takazawa, Mitsuhiro Tsukimura, Haruhisa Saito, Kenji Kobayashi, Jun Aoki, Shunsuke Suzuki, Yuichi Gomi, Seisuke Matsuda, and Yoshitaka Tadaki, *Olympus Corporation, Japan*
- 9:20 An End-point Visualization Test Structure for All Plasma Dry Release of Deep-RIE**
1.2 MEMS 6
Yuki Okamoto, Eric Lebrasseur, Isao Mori, and Yoshio Mita,
The University of Tokyo, Japan
- 9:40 Spring-constant measurement methods for RF-MEMS capacitive switches** 10
1.3 Jiahui Wang, Jeroen Bielen, Cora Salm, and Jurriaan Schmitz,
University of Twente, The Netherlands
- 10:00 Microfabricated test structures for thermal resonant gas sensor** 16
1.4 Matthieu Denoual¹, M. Pouliquen¹, Julien Grand¹, Hussein Awala¹, Sveltana Mintova¹, O. de Sagazan², Shu Inoue³, Agnes Tixier-Mita³, Yoshio Mita³, and D. Robbes¹
¹ENSICAEN, *University of Caen, France*, ²The University of Rennes, *France*,
³The University of Tokyo, *Japan*

SESSION 2: Thermal Issues

2016 Mar 29, 11:00 – 12:20

Co-Chairs: Anthony J. Walton, *University of Edinburgh, UK*

Hi-Deok Lee, *Chungnam National University, Korea*

- 11:00 A Test Structure for Analysis of Metal Wire Effect on Temperature Distribution in**
2.1 Stacked IC 22
Toshihiro Matsuda¹, Haruka Demachi¹, Hideyuki Iwata¹, Tomoyuki Hatakeyama¹, and Takashi Ohzone²,
¹Toyama Prefectural University, *Japan*, ²Dawn Enterprise, *Japan*
- 11:20 Dedicated test-structures for investigation of the thermal impact of the BEOL in**
2.2 advanced SiGe HBTs in time and frequency domain 28
Rosario D'Esposito¹, Sebastien Fregonese¹, Anjan Chakravorty², and Thomas Zimmer¹,
¹University of Bordeaux, *France*, ²IIT Madras, *India*
- 11:40 Hotspot test structures for evaluating carbon nanotube microfin coolers and**
2.3 graphene-like heat spreaders..... 32
Kjell Jeppson¹, Jie Bao², Shirong Huang², Yong Zhang², Shuangxi Sun², Yifeng Fu², and Johan Liu², ¹Chalmers University, *Sweden*, ²Shanghai University, *China*

12:00	Transistor Self-Heating Correction and Thermal Conductance Extraction using Only	
2.4	DC Data	38
	Colin C. McAndrew ¹ , Alexandra Lorenzo-Cassagnes ¹ , and Olin L. Hartin ² ,	
	¹ NXP Semiconductors, AZ, USA, ² Arizona State University, AZ, USA	

SESSION 3: Arrayed Test Structures

2016 Mar 29, 14:10 – 15:40

Co-Chairs: Tatsuya Ohguro, *Toshiba, Japan*
Christopher Hess, *PDF Solutions, USA*

14:10	[Invited] Random Telegraph Noise Measurement and Analysis based on Arrayed Test	
3.1	Circuit toward High S/N CMOS Image Sensors	46
	Rihito Kuroda, Akinobu Teramoto, and Shigetoshi Sugawa, <i>Tohoku University, Japan</i>	
14:40	Proposal of a New Array Structure to Enable the Detection of Soft Failure and the Aging	
3.2	Test with Overcurrent of Resistive Element	52
	Shingo Sato and Yasuhisa Omura, <i>Kansai University, Japan</i> ,	
15:00	Advanced Ioff Measureable MOSFET Array with Eliminating Leakage Current of	
3.3	Peripheral Circuits	58
	Tsuyoshi Suzuki, Shigetaka Mori, Hidetoshi Oishi, Masaaki Bairo, Manabu Tomita, Kazuhisa Ogawa, Yuzo Fukuzaki, and Hidetoshi Ohnuma, <i>Sony Corporation, Japan</i>	
15:20	Design and use of an array-based test structure to characterize mechanical stress effects	
3.4	caused by WLCSP solder bumps	62
	Hans Tuinhout and Rob van Dalen, <i>NXP Semiconductors, The Netherlands</i>	

SESSION 4: Parameter Extraction

2016 Mar 29 16:10 – 17:10

Co-Chairs: Kjell Jeppson, *Chalmers University, Sweden*

16:10	New access resistance extraction methodology for 14nm FD-SOI technology	70
4.1	Jean-Baptiste Henry ¹ , Antoine Cros ¹ , Quentin Rafhay ² , Gerard Ghibaudo ² , and Julien Rosa ¹ ,	
	¹ STMicroelectronics, France, ² IMEP-LAHC, France,	
16:30	Test Structures for CMOS RF Reliability Assessment	76
4.2	Leonhard HeiB ^{1,2} , Andreas Lachmann ² , Reiner Schwab ² , Georgos Panagopoulos ² , Peter Baumgartner ² , Mamatha Yakkegondi Virupakshappa ² , and Doris Schmitt-Landsiedel ^{1,2} ,	
	¹ Technical University of Munich, Germany, ² Intel Deutschland GmbH, Germany,	
16:50	Statistical Analysis and Modeling of Random Telegraph Noise Based on Gate Delay	
4.3	Variation Measurement	82
	A.K.M. Mahfuzul Islam, Tatsuya Nakai, and Hidetoshi Onodera, <i>Kyoto University, Japan</i>	

SESSION 5: RF and Power Devices

2016 Mar 30 9:20 – 10:20

Co-Chairs: Colin McAndrew, *NXP Semiconductors, USA*

- 9:20 A High Power Curve Tracer for Characterizing Full Operational Range of SiC Power**
5.1 Transistors 90
Yohei Nakamura, Michihiro Shintani, Takashi Sato, and Takashi Hikihara,
Kyoto University, Japan
- 9:40 A Test Structure Set for on-wafer 3D-TRL calibration** 96
5.2 Manuel Potéreau, Arnaud Curutchet, Rosario D’Esposito, Magali De Matos, Sebastien
Fregonese, and Thomas Zimmer, *University of Bordeaux, France*
- 10:00 Test Structures of LASCR Device for RF ESD Protection in Nanoscale CMOS Process**
5.3 100
Chun-Yu Lin and Rong-Kun Chang, *National Taiwan Normal University, Taiwan*

SESSION 6: Capacitances

2016 Mar 30 10:50 – 11:50

Co-Chairs: Hans P. Tuinhout, *NXP Semiconductor, The Netherlands*
Chadwin Young, *University of Texas at Dallas, USA*

- 10:50 Highly Effective and Versatile Test Structure for Evaluating Dielectric Properties using**
6.1 Flexible Pulse Generator on Chip 106
Shigetaka Mori, Ken Sawada, Manabu Tomita, Kazuhisa Ogawa, Tsuyoshi Suzuki, Hidetoshi
Oishi, Masaaki Bairo, Yuzo Fukuzaki, and Hidetoshi Ohnuma, *Sony Corporation, Japan*
- 11:10 Extraction of Floating-Gate Capacitive Parameters in Split-Gate Flash Memory Cells**
6.2 110
Yuri Tkachev, *Silicon Storage Technology, Inc., CA, USA*
- 11:30 Demonstration of MOS Capacitor Measurement for Wafer Manufacturing using a**
6.3 Direct Charge Measurement 116
Kenichi Takano¹, Masaharu Goto¹, Ernesto Shiling², Arthur Gasasira³, and Jiun-Hsin Liao³,
Keysight Technologies, ¹Japan, ²CA, USA, ³GLOBALFOUNDRIES, NY, USA

SESSION 7: Memories

2016 Mar 30 13:40 – 14:40

Co-Chairs: Yuzo Fukuzaki, *Sony Corporation, Japan*
Carlo Cagli, *CEA/LETI, France*

- 13:40 Test circuits to characterize setup/hold/access times, minimum voltage and maximum frequency of operation for memory compilers 122**
7.1 Nitin Dhamija, Gaurav Lalani, Mike Nelson, Joe Brown, Henning Spruth, and Puneet Sharma, *Freescale Semiconductor, India*
- 14:00 A New Write Stability Metric Using Extended Write Butterfly Curve for Yield Estimation in SRAM Cells at Low Supply Voltage 126**
7.2 Hao Qiu, Kiyoshi Takeuchi, Tomoko Mizutani, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto, *The University of Tokyo, Japan*
- 14:20 Measurement of SRAM Power-On State for PUF Applications Using an Addressable SRAM Cell Array Test Structure 130**
7.3 Kiyoshi Takeuchi, Tomoko Mizutani, Hirofumi Shinohara, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto, *The University of Tokyo, Japan*

SESSION 8: Non-Volatile Memories

2016 Mar 30 15:30 – 17:00

Co-Chairs: Jurriaan Schmitz, *University of Twente, The Netherlands*
Satoshi Habu, *Keysight Technologies, Japan*

- 15:30 [Invited] New power-gating architectures using nonvolatile retention: Comparative study of nonvolatile power-gating (NVPg) and normally-off architectures for SRAM 136**
8.1 Yusuke Shuto, Shuu'ichirou Yamamoto, and Satoshi Sugahara, *Tokyo Institute of Technology, Japan*
- 16:00 Challenges of Modeling the Split-Gate SuperFlash® Memory Cell with 1.1V Select Transistor 142**
8.2 M. Tadayoni¹, S. Martinie², O. Rozeau², S. Hariharan¹, C. Raynaud², and N. Do¹,
¹*Silicon Storage Technology, Inc., CA, USA*, ²*CEA-LETI, France*
- 16:20 Ultra-small and Ultra-reliable Innovative Fuses Scalable from 0.35µm to 28nm 148**
8.3 Shine Chung, Wen-Kuan Fang, YC Hsu, JY Hsiao, Lupin Lin, and Wen-Hua Yu, *Attopsemi Technology Corporation, Taiwan*
- 16:40 Impact of a Laser Pulse On HfO₂-based RRAM Cells Reliability and Integrity 152**
8.4 A. Krakovinsky^{1,2}, M. Bocquet², R. Wacquez¹, J. Coignus¹, D. Deleruyelle², C. Djaou², G. Reimbold¹, and J-M. Portal², ¹*CEA-LETI, France*, ²*Aix-Marseille University, France*

SESSION 9: Process and Device Characterization

2016 Mar 31 9:00 – 10:20

Co-Chairs: Larg Weiland, *PDF Solutions, USA*

Bing-Yue Tsui, *National Chiao Tung University, Taiwan*

- 9:00 Test Structures to support the Development and Process Verification of Microelectrodes**
9.1 for High Temperature Operation in Molten Salts 158
E.O. Blair, D.K. Corrigan, I. Schmueser, J.G. Terry, S. Smith, A.R. Mount, and A.J. Walton,
The University of Edinburgh, UK
- 9:20 Interface Trap Density Estimation in FinFETs from the Subthreshold Current** 164
9.2 J. Schmitz, B. Kaleli, P. Kuipers, N. van den Berg, S.M. Smits, and R.J.E. Hueting,
University of Twente, The Netherlands
- 9:40 Novel Test Structure for Evaluating Dynamic Dopant Activation after Ion Implantation**
9.3 168
Jung-Ruey Tsai¹, Ruey-Dar Chang², Cheng-Hui Chou², Hsueh-Chun Liao², Sz-Kai Huang^{1,2},
Sung-Hung Lin^{1,2}, and Jui-Chang Lin^{1,2},
¹*Asia University, Taiwan*, ²*Chang Gung University, Taiwan*
- 10:00 Top-Gated MoS₂ Capacitors and Transistors with High-k Dielectrics for Interface Study**
9.4 172
Peng Zhao¹, A. Azcatl¹, P. Bolshakov-Barrett¹, P.K. Hurley², R.M. Wallace¹, and C.D. Young¹,
¹ *The University of Texas at Dallas*, ²*University of College Cork, Ireland*

SESSION 10: Materials Characterization

2016 Mar 31 10:50 – 12:10

Co-Chairs: Bill Verzi, *Agilent Technologies, USA*

- 10:50 Chip level characterisation studies of Ni and NiFe electrochemical deposition using test**
10.1 structures 178
J. Murray, R. Perry, J.G. Terry, S. Smith, A.R. Mount, and A.J. Walton,
The University of Edinburgh, UK
- 11:10 Test Structures for the Characterisation of Conductive Carbon Produced from**
10.2 Photoresist 184
S. Scarfi, S. Smith, A. Tabasnikov, I. Schmueser, E. Blair, A.S. Bunting, A.J. Walton,
A.F. Murray and J.G. Terry, *The University of Edinburgh, UK*
- 11:30 Comparing Current Flows in Ultrashallow pn- / Schottky-like Diodes with 2-Diode Test**
10.3 Method 190
X. Liu and L.K. Nanver, *University of Twente, The Netherlands*
- 11:50 A Reliable Schottky Barrier Height Extraction Procedure** 196
10.4 Bing-Yue Tsui and Fu-Tze Yu, *National Chiao-Tung University*