

# **2016 IEEE 20th Workshop on Signal and Power Integrity (SPI 2016)**

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## TECHNICAL PROGRAM: ORAL PAPERS

### Session 1: Behavioral Modeling

#### *Robust nonlinear models for CMOS buffers* "%%%

C. Diouf (1), M. Telescu (2), N. Tanguy (2), I.S. Stievano (3), F.G. Canavero (3)

(1) École Nationale d'Ingénieurs de Brest, France; (2) Université de Bretagne Occidentale, France;

(3) Politecnico di Torino, Italy

#### *Discrete controlled pre-driver FIR model for hybrid IBIS model AMS simulation* "%%)

W. Dghais (1), F.H. Bellamine (2)

(1) Université de Sousse, Tunisia; (2) Université de Carthage, Tunisia

### Session 2: Measurements and Characterization

#### *Characterization of high-frequency interconnects: comparison between time- and frequency-domain methods* "%%-

M. Bieler, U. Arz

Physikalisch-Technische Bundesanstalt Braunschweig, Germany

#### *Signal propagation properties of anisotropic conducting polymers up to 110 GHz and their applicability in test fixtures* "%%%

M. Sippel, G. Gold, K. Helmreich

Friedrich-Alexander-University Erlangen-Nuremberg, Germany

### Session 3: Optical and Nano Interconnects

#### *An adjoint method based approach for optical waveguide design in thin glass sheets using ion-exchange processes* "%%+

D. Zhang, T. Kühler, E. Griese

University of Siegen, Germany

#### *Electrothermal modeling and characterization of carbon interconnects with negative temperature coefficient of the resistance* "%%&%

A. Maffucci (1), F. Micciulla (2), A. Cataldo (2), S. Bellucci (2), G. Miano (3)

(1) University of Cassino and Southern Lazio, Italy; (2) INFN-LNF Frascati, Italy; (3) University Federico II, Italy

#### *Propagation of surface plasmon polaritons on graphene nano-interconnects* "%%&)

R. Araneo (1), G. Lovat (1), S. Celozzi (1), P. Burghignoli (1), G.W. Hanson (2)

(1) Sapienza University of Rome, Italy; (2) University of Wisconsin-Milwaukee, USA

### Session 4: Stochastic Analysis and Uncertainty Quantification

#### *Impact of continuous time linear equalizer variability on eye opening of high-speed links* "%%&-

J.B. Preibisch, T. Reuschel, K. Scharff, C. Schuster

Technische Universität Hamburg-Harburg, Germany

#### *Hyperbolic polynomial chaos expansion (HPCE) and its application to statistical analysis of nonlinear circuits* "%% '

M. Ahadi, A. Krishna Prasad, S. Roy

Colorado State University, USA

#### *A big-data approach to handle process variations: uncertainty quantification by tensor recovery* "%% +

Z. Zhang, T.-W. Weng, L. Daniel

Massachusetts Institute of Technology, USA

#### *Application of Taylor models to the worst-case analysis of stripline interconnects* "%%( %

P. Manfredi (1), R. Trinchero (2), F.G. Canavero (3), I.S. Stievano (3)

(1) Ghent University, Belgium; (2) Istituto Nazionale di Fisica Nucleare (INFN) – Sezione di Torino,

Italy; (3) Politecnico di Torino, Italy

## **Session 5: Noise Analysis and Reduction Techniques**

***Simulation-based analysis on EMI effect in LPDDR interface for mitigating RFI in a mobile environment***"'"( )

S. Kim, S. Moon, S. Lee, D. Yi, G. Park, S. Shin, S. Pae  
Samsung Electronics, South Korea

***Novel absorptive design of common-mode filter at desired frequency band***"'"( -

P.-J. Li, C.-H. Cheng, Y.-C. Tseng, T.-L. Wu  
National Taiwan University, Taiwan

***Higher-order virtual ground fence design for filtering power plane noise***"'"' '

A.E. Engin (1), I. Ndip (2), K.-D. Lang (2)  
(1) San Diego State University, USA; (2) Fraunhofer-Institut fuer Zuverlaessigkeit und Mikrointegration (IZM), Germany

## **Session 6: Power Distribution Networks**

***Effect of via-transitions on signal integrity using power transmission lines***"'"\* \*

D.C. Zhang, M. Swaminathan, D. Keezer  
Georgia Institute of Technology, USA

***Power delivery impedance impact of power gating schemes***"'"\$

S. Shekhar (1), A.K. Jain (1), N. Winer (2)  
(1) Intel Corporation, USA; (2) Intel Corporation, Israel

***A clustering technique for fast electrothermal analysis of on-chip power distribution networks***"'"(

A. Magnani (1), M. de Magistris (1), A. Maffucci (2), A. Todri-Sanial (3)  
(1) University Federico II, Italy; (2) University of Cassino and Southern Lazio, Italy; (3) University of Montpellier, France

## **Session 7: Special Session on Model Order Reduction**

***Stability preserving post-processing methods applied in the Loewner framework***"'"\*,

I.V. Gosea (1), A.C. Antoulas (2)  
(1) Jacobs University Bremen, Germany; (2) Rice University, USA

***Efficient time-domain variability analysis using parameterized model-order reduction***"'"&

Y. Tao, B. Nouri, M. Nakhla, R. Achar  
Carleton University, Canada

***Transfer function modeling for the buck converter***"'""+\*

S. Lefteriu, C. Labarre  
Ecole des Mines de Douai, France

***Accelerating time domain simulations of PLLs***"'"\$, \$

G. De Luca (1), W.H.A. Schilders (1), P. Bolcato (2), R. Larcheveque (2), J. Rommes (2)  
(1) TU Eindhoven, The Netherlands; (2) Mentor Graphics, France

## **Session 8: Electromagnetic Modeling**

***IR drop analysis of high-speed PCBs using 3D planar EM technology***"'"(

J. Sercu  
Keysight Technologies, Belgium

***Extension of 2.5D PEEC for coplanar structures in power distribution network analysis***"'"', ,

B.P. Nayak, S.R. Vedicherla, D. Gope  
Indian Institute of Science, India

***Digital wave formulation of quasi-static partial element equivalent circuit method***"'"- &

P. Belforte (1), L. Lombardi (2), D. Romano (2), G. Antonini (2)  
(1) Independent Researcher; (2) Università degli Studi dell'Aquila, Italy

## Session 9: Novel Techniques for Signal and Power Integrity

### ***Investigation of the power-clock network impact on adiabatic logic*** \*\*\*\*L \*

N. Jeanniot (1), A. Todri-Sanial (1), P. Nouet (1), G. Pillonnet (2), H. Fanet (2)  
(1) University of Montpellier, France; (2) CEA-LETI-MINATEC, France

### ***Navigating PCB stackup layer assignments for optimized SI and PI performance in high speed, high power designs*** \*\*\*\*\$S\$

C.M. Smutzer, M.J. Degerstrom, B.K. Gilbert  
Mayo Clinic, USA

### ***Ripple analysis: identify and quantify reflective interference through ISI decomposition*** \*\*\*\*%\$(

R.J. Allred (1,2), B. Katz (2), C. Furse (1)  
(1) University of Utah, USA; (2) SiSoft, USA

### ***Pessimism removal in a system analysis of a 28Gbps SERDES link*** \*\*\*\*%\$,

O. Bayet (1), M. Cereda (2)  
(1) STMicroelectronics, France; (2) STMicroelectronics, Italy

### ***SPI co-extraction and SPICE co-simulation for package on-die decap optimization*** \*\*\*\*%&

A. Ciccomancini Scogna (1), L.K. Teoh (2)  
(1) CST, Germany; (2) eASIC, Malaysia

## Session 10: TSV and 3DIC

### ***TSVs embedded in a microfluidic heat sink: high-frequency characterization and thermal modeling*** \*\*\*\*%%

H. Oh, Y. Zhang, T.E. Sarvey, G.S. May, M.S. Bakir  
Georgia Institute of Technology, USA

### ***On the upper bound of total uncorrelated crosstalk in large through silicon via arrays*** \*\*\*\*%&\$

D. Dahl (1), T. Reuschel (1), X. Duan (2), I. Ndip (3), K.-D. Lang (3), C. Schuster (1)  
(1) Technische Universität Hamburg-Harburg, Germany; (2) IBM, Germany; (3) Fraunhofer Institute for Reliability and Microintegration (IZM), Germany

### ***Impact of voltage bias on through silicon vias (TSV) depletion and crosstalk*** \*\*\*\*%&

S. Piersanti (1), F. de Paulis (1), A. Orlandi (1), J. Fan (2), J. Drewniak (2), B. Achkir (3)  
(1) University of L'Aquila, Italy; (2) Missouri University of Science and Technology, USA; (3) Cisco System Inc., USA

### ***High frequency modeling of through silicon capacitors (TSC) architectures in silicon interposer*** \*\*\*\*%&

K. Dieng (1), C. Bermond (1), P. Artillan (1), O. Guiller (2), T. Lacreva (1), S. Joblot (2), G. Houzet (1), A. Farcy (2), Y. Lamy (3), B. Fléchet (1)  
(1) Université de Savoie Mont-Blanc, France; (2) STMicroelectronics, France; (3) Université Grenoble Alpes, France

## TECHNICAL PROGRAM: POSTER PAPERS

### ***High-speed flip chip package co-design with optimization of anti-pad size variations on metal plane layout*** \*\*\*\*% &

H.J. Lim (1), J.K. Yang (2), H.Y. Ku (2), C.G. Ahn (2), T.Y. Lee (2), B.J. Kim (2), J.Y. Chung (2)  
(1) Amkor Technology Inc., South Korea; (2) Amkor Technology Inc., USA

### ***Eye-diagram estimation using equivalent circuit model of coupled microstrip channel on high-speed and wide I/O channel for 2.5D and 3D IC*** \*\*\*\*% \*

S. Choi, H. Kim, D.H. Jung, J.J. Kim, J. Lim, H. Lee, K. Cho, J. Kim  
Korea Advanced Institute of Science and Technology, South Korea

### ***Pole residue equivalent system solver (PRESS)*** \*\*\*\*% \$

V. Avula, A. Zadehgol  
University of Idaho, USA

**An analysis of power supply induced jitter for a voltage mode driver in high speed serial links** (J.N. Tripathi (1), V.K. Sharma (2), H. Advani (3), P.N. Singh (1), H. Shrimali (2), R. Malik (1))  
(1) STMicroelectronics, India; (2) Indian Institute of Technology Mandi, India; (3) Synopsys Inc., India

**Power-aware signal integrity analysis of DDR4 data bus in onboard memory module**, A.K. Pandey  
Keysight Technologies, India

**Achievements and challenges in power and signal integrity analyses of set-top box products** & X. Lecoq, E. Terlain, E. Dralez, D. Auchere  
STMicroelectronics, France

**System-level practical dynamic voltage drop simulation with IC internal VRM** \* J. Jo, S. Kim, S. Lee, S. Pae  
Samsung Electronics

**Accurate prediction of interconnect capacitance in self-aligned quadruple patterning** \$ T. Kanamoto (1,6), H. Ammo (2,6), T. Hasegawa (3,6), S. Kobayashi (4,6), T. Fukuda (4,6), M. Kawano (5,6)  
(1) Renesas System Design, Japan; (2) Sony, Japan; (3) Sony LSI Design, Japan; (4) Toshiba, Japan; (5) Ricoh, Japan; (6) JEITA EDA Technical Committee, Japan

**Frequency dependent and nonuniform parameters transmission line model** (A. Wardzinska, W. Bandurski  
Poznan University of Technology, Poland

**A new EMI-noise reduction method in LSI-package-board system** , T. Hasegawa (1,7), T. Kanamoto (2,7), H. Ammo (3,7), M. Kawano (4,7), T. Fukuda (5,7), S. Kobayashi (5,7), A. Kurokawa (6,7)  
(1) Sony LSI Design, Japan; (2) Renesas System Design, Japan; (3) Sony, Japan; (4) Ricoh, Japan; (5) Toshiba, Japan; (6) Hirosaki University, Japan; (7) JEITA EDA Technical Committee, Japan

**Power delivery network simulation methodology including integrated circuit behavior** & B. Goral (1), C. Gautier (1), A. Amedeo (2)  
(1) Ecole Normale Supérieure de Cachan, France; (2) Thales Communication and Security, France

**Common-mode noise reduction of right-angled coupled stripline using timing-offset differential signal** \* C.-C. Yeh, C.-L. Wang  
National Taiwan University of Science and Technology, Taiwan

**Fast transient thermal simulation of 2.5-D packages on through silicon via interposer** \$ Q. Feng, M. Tang, G. Fu, J. Mao  
Shanghai Jiao Tong University, China

**Generalized anisotropic polynomial chaos approach for expedited statistical analysis of nonlinear radio-frequency (RF) circuits** (I. Kapse, A. Krishna Prasad, S. Roy  
Colorado State University, USA

**On the use of digital predistortion to compensate the nonlinear effects of semiconductor optical amplifiers** ""% +

S. Azou (1), S. Bejan (1), P. Morel (1), C. Diouf (1), A. Sharaiha (1), M. Telescu (2), N. Tanguy (2)  
(1) École Nationale d'Ingénieurs de Brest, France; (2) Université de Bretagne Occidentale, France

**System level estimation of a PCB electromagnetic radiated emission** ""% -

S. Heidari, M. Mehri, N. Masoumi  
University of Tehran, Tehran, Iran

**The analysis of EMI effects on the performance of electronic systems implemented on a PCB** ""% '

M. Mehri, S. Heidari, N. Masoumi  
University of Tehran, Tehran, Iran

**Addressing PCB effects in the design of a buck converter** ""% +

I. Erdin (1), R. Achar (2)  
(1) Celestica Inc., Canada; (2) Carleton University, Canada

**Filter design method for GaN-buck converter taking into account of the common-mode propagation paths** ""%&\$

J.L. Kotny, T. Duquesne, N. Idir  
Université de Lille, France

**High-frequency modelling of surface-mount power inductor used in switching dc-dc converters** ""%&(

J. Bacmaga (1), R. Blebic (1,2), R. Gillon (3), A. Baric (1)  
(1) University of Zagreb, Croatia; (2) KU Leuven, Belgium; (3) ON Semiconductor, Belgium

**Analysis of coupled exponential microstrip lines by means of a multi-step perturbation technique** ""%&,

P. Manfredi, D. De Zutter, D. Vande Ginste  
Ghent University/iMinds, Belgium

**Adaptive algorithm for sampling nonlinear circuit behaviour in time-domain** ""%&%&

M. Magerl (1), C. Stockreiter (2), O. Eisenberger (2), A. Baric (1)  
(1) University of Zagreb, Croatia; (2) ams AG, Austria

**Optical directional coupler for graded index waveguides in thin glass sheets for PCB integration** ""%&%

J.H. Stosch, T. Kühler, E. Griese  
University of Siegen, Germany

**Radiation of synchronous buck converter modelled by three magnetic moments and combined with SPICE simulations** ""%&&

R. Blebic (1,2), R. Gillon (3), B. Nauwelaers (2), A. Baric (1)  
(1) University of Zagreb, Croatia; (2) KU Leuven, Belgium; (3) ON Semiconductor, Belgium

**Finite difference schemes for transient simulation of transmission lines exhibiting uncertainties** ""%&&

X. Chen, J.E. Schutt-Ainé, A.C. Cangellaris  
University of Illinois at Urbana-Champaign, USA

**High-fidelity, high-performance full-wave computational algorithms for intra-system EMI analysis of IC and electronics** ""%&&

S. Lin, H.-W. Gao, Z. Peng  
University of New Mexico, USA

**Characterize server platform voltage regulator performance beyond power conversion** ""%&%

J. He, W. Xu, C. Guo, D. Figueiroa  
Intel Corporation, USA