

2016 International Conference on FPGA Reconfiguration for General-Purpose Computing (FPGA4GPC 2016)

**Hamburg, Germany
9-10 May 2016**



**IEEE Catalog Number: CFP16DUK-POD
ISBN: 978-1-5090-1360-9**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

******This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16DUK-POD
ISBN (Print-On-Demand):	978-1-5090-1360-9
ISBN (Online):	978-1-5090-1359-3

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Table of Contents

Keynote I	1
1 Model-based development of distributed embedded controller — rapid prototyping using IOPT-Tools and FPGAs <i>Luis Gomes</i>	
Session 1	7
7 Generic Operating-System Support for FPGAs <i>Dominik Meyer, Jan Haase, Marcel Eckert, Bernd Klauer</i>	
13 An In-Kernel NOSQL Cache for Range Queries Using FPGA NIC <i>Korechika Tamura, Hiroki Matsutani</i>	
19 A Self-Adaptive Dynamic Partial Reconfigurable Architecture for Online Data Stream Compression <i>Seyyed Mahdi Najmabadi, Zhe Wang, Yousef Baroud, Sven Simon</i>	
Keynote II	
Beyond traditional HPC — An Industrial Perspective on Massively Parallel Reconfigurable Computing in Scientific Applications <i>Stefan Baumgart, SciEngines, Kiel, Germany</i>	
Session 2	25
25 μ Streams: A Tool for Automated Streaming Pipeline Generation on Soft-core Processors <i>Kris Heid, Christian Hochberger, Jan Weber</i>	
31 High-Speed Decompression Architecture of Compressed HTTP Streams for the Internet Routers <i>Hironori Okano, Hayato Yamaki, Hiroaki Nishi</i>	
37 Architectural Requirements for Constructing Hardware Supported Sandboxes <i>Marcel Eckert, Jan Haase, Dominik Meyer, Bernd Klauer</i>	
Tutorial	
Introduction to Linux device driver development for embedded FPGA-Designs <i>Marcel Eckert, Dominik Meyer, Helmut-Schmidt University Hamburg, Germany</i>	
List of Authors	43