2015 16th International Workshop on Microprocessor and SOC Test and Verification (MTV 2015)

Austin, Texas, USA 3-4 December 2015



IEEE Catalog Number: ISBN:

CFP15MTV-POD 978-1-5090-0886-5

Copyright © 2015 by the Institute of Electrical and Electronics Engineers, Inc All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP15MTV-POD

 ISBN (Print-On-Demand):
 978-1-5090-0886-5

 ISBN (Online):
 978-1-5090-0885-8

ISSN: 1550-4093

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400

Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com



2015 16th International Workshop on Microprocessor and SOC Test and Verification

MTV 2015

Table of Contents

Preface	vii
Acknowledgment	viii
Conference Organization	ix
Program Committee	x
Corporate Sponsors	xi
Innovative Verification Methodologies	
Specification-Based Test Program Generation for ARM VMSAv8-64 Memory Management Units	1
Mikhail Chupilko, Alexander Kamkin, Artem Kotsynyak, Alexander Protsenko, Sergey Smolov, and Andrei Tatarnikov	
Enhancing the Stress and Efficiency of RIS Tools Using Coverage Metrics	7
SoC Development and Prototype with VDK	10
Leveraging Virtual Prototype Models for Hardware Verification of an Accelerated Network Packet Processing Engine	15
Debug and Test Coverage	
A Topological Approach to Hardware Bug Triage	20
Automatic Bug Fixing Daniel Hansson	26
Novel MC/DC Coverage Test Sets Generation Algorithm, and MC/DC Design Fault Detection Strength Insights	32
Mohamed A. Salem and Kerstin I. Eder	

Hybrid Post Silicon Validation Methodology for Layerscape SoCs
involving Secure Boot: Boot (Secure & Non-secure) and Kernel Integration
with Randomized Test
Amandeep Sharan and Ashish Gupta
Security and Verification
Harnessing Nanoscale Device Properties for Hardware Security
Bicky Shakya, Fahim Rahman, Mark Tehranipoor, and Domenic Forte
Hierarchy-Preserving Formal Verification Methods for Pre-silicon Security
Assurance
Xiaolong Guo, Raj Gautam Dutta, and Yier Jin
Modeling and Analysis of Trusted Boot Processes Based on Actor Network
Procedures
Mark Nelson and Peter-Michael Seidel
Performance and Characterization
Performance of a SystemVerilog Sudoku Solver with VCS
Characterizing Processors for Energy and Performance Management
Author Index