

# **2016 38th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD 2016)**

**Garden Grove, California, USA  
11-16 September 2016**



**IEEE Catalog Number: CFP16413-POD  
ISBN: 978-1-4673-8926-6**

**Copyright © 2016, EOS/ESD Association Inc.  
All Rights Reserved**

***\*\*\*This publication is a representation of what appears in the IEEE  
Digital Libraries. Some format issues inherent in the e-media version may  
also appear in this print version.***

IEEE Catalog Number:	CFP16413-POD
ISBN (Print-On-Demand):	978-1-4673-8926-6
ISBN (Online):	978-1-58537-289-8
ISSN:	0739-5159

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# TABLE OF CONTENTS

## 1A: High Voltage I

Moderator: Farzan Farbiz, Texas Instruments

### 1A.1 ESD Protection Design in a-IGZO TFT Technologies 1

M. Scholz, S. Steudel, K. Myny, S. Chen, G. Hellings, D. Linten, imec; R. Boschke, imec, KU Leuven

### 1A.2 ESD Robust 800V SCR-JFET with p+ Ballast Structure 8

Shuji Fujiwara, Richard Burton, ON Semiconductor

### 1A.3 Predictive High Voltage ESD Device Design Methodology 14

Jian-Hsing Lee, Natarajan Mahadeva Iyer, Ruchil Jain, Manjunatha Prabhu, GLOBALFOUNDRIES, Inc.

### 1A.4 PNP-eSCR ESD Protection Device with Tunable Trigger and Holding Voltage for High Voltage Applications 22

Da-Wei Lai, Shuang Zhao, Jian Gao, Theo Smedes, NXP Semiconductors

## 2A: On Chip Physics I

Moderator: Dolphin Abessolo-Bidzo, NXP Semiconductors

### 2A.1 HV ESD Diodes Investigation under vf-TLP Stresses: TCAD Approach 30

Leonardo Di Biccari, Lorenzo Cerati, Lucia Zullino, Antonio Andreini, STMicroelectronics

### 2A.2 Unique Current Conduction Mechanism through Multi Wall CNT Interconnects under ESD Conditions 40

Abhishek Mishra, Mayank Srivastava, Indian Institute of Science

### 2A.3 Dielectric Breakdown of TMR Sensors and the Role of Joule Heating 46

Icko Eric Timothy Iben, IBM

### 2A.4 Low Voltage SCR Clamp with High-V<sub>T</sub> Reference 55

Vladislav Vashchenko, Slavica Malobabic, Maxim Integrated Corp.; Andrei Shibkov, Angstrom Design Automation

## 2B: Factory Control I

Moderator: Wolfgang Stadler, Intel Corporation

### 2B.1 Electrostatic Shock Risks in Assembly of Large Wind Turbine Blades 61

Jörg Thürmer, EPA Design & Control; Jeremy Smallwood, Electrostatic Solutions, Ltd.

### 2B.2 Product Qualification & Degradation of Steel Toe ESD Footwear 68

Steve Lim, Royal Muar City; L. H. Koh, Muhammad Hamizan Bin Abdul Samad, W. F. Wong, Y.H. Goh, Everfeed Technology Pte. Ltd.

## **2B.3 Charge Relaxation of Slowly Dissipative Polymers 75**

Toni Viheriäkoski, Cascade Metrology; Eira Kärjä, Premix Oy; Jukka Hillberg, Ion PhasE; Pasi Tamminen, Tampere University of Technology

## **3A: Advanced CMOS I**

Moderator: Teruo Suzuki, SocioNext

### **3A.1 Area-Efficient ESD Design Using Power Clamps Distributed Outside I/O Cell Ring 84**

Satoshi Maeda, Masanori Tanaka, Yoko Otsuka, Akinobu Watanabe, Masayuki Tsukuda, Yasuyuki Morishita, Renesas System Design Co., Ltd.

### **3A.2 An On-Chip Combo Clamp for Surge and Universal ESD Protection in Bulk FinFET Technology 91**

Ming-Fu Tsai, Jen-Chou Tseng, Chung-Yu Huang, Tzu-Heng Chang, Kuo-Ji Chen, Ming-Hsiang Song, TSMC

### **3A.3 Novel Insights into the Power-off and Power-on Transient Performance of Power-Rail ESD Clamp Circuit 98**

Guangyi Lu, Yuan Wang, Yize Wang, Jian Cao, Xing Zhang, Peking University

## **3B: System Level ESD I**

Moderator: Benjamin Orr, Missouri University of Science and Technology

### **3B.1 Measurement of Discharging Currents through an IC due to the Charged Board Event Using a Shielded Rogowski Coil 105**

Junsik Park, Jingook Kim, Ulsan National Institute of Science and Technology (UNIST); Jongsung Lee, Seongmoo Kim, Cheolgu Jo, Byongsu Seol, Samsung Electronics Co.

### **3B.2 Case Study of DPI Robustness of a MOS-SCR Structure for Automotive Applications 111**

Yang Xiu, Elyse Rosenbaum, University of Illinois at Urbana-Champaign; Farzan Farbiz, Akram Salman, Yue Zu, Mariano Dissegna, Gianluca Boselli, Texas Instruments

### **3B.3 HMM Single Site Testing: Can We Reproduce Component Failure Level with the HMM Document? 117**

Mirko Scholz, imec; Robert Ashton, ON Semiconductor; Theo Smedes, Richard Derikx, NXP Semiconductors; Marcel Dekker, MASER Engineering; Jon Barth, Barth Electronics

## **4A: Tester and Testing Methods**

Moderator: Timothy Maloney, Intel Corporation

### **4A.1 Improving CDM Measurements with Frequency Domain Specifications 125**

Jon Barth, John Richner, Barth Electronics, Inc.; Leo G. Henry, ESD/TLP Consultants, LLC

## **4A.2 JS-002 Module and Product CDM Result Comparison to JEDEC and ESDA CDM Methods 135**

A. Righter, Analog Devices Inc.; R. Ashton, ON Semiconductor; B. Carn, Intel; M. Johnson, S. Ward, Texas Instruments; B. Reynolds, GLOBALFOUNDRIES Inc.; T. Smedes, NXP Semiconductors; H. Wolf, Fraunhofer EMFT

## **4A.3 Predict the Product Specific CDM Stress Using Measurement-Based Models of CDM Discharge Heads 142**

Friedrich zur Nieden, Kai Esmark, Stefan Seidl, Reinhold Gärtner, Infineon Technologies AG

## **4B: Factory Control II**

Moderator: Marcus Koh, Everfeed Technology, Pte. Ltd.

### **4B.1 An ESD Control Method Considering the Semiconductor Device Charged Voltage 152**

*RCJ Invited Paper*

Nobuyuki Wakai, Takashi Setoya, Toshiba Corporation Storage & Electronic Devices Solutions, Co.; Kunihiro Maki, Futoshi Kaku, Kenji Hirose, Japan Semiconductor Corporation

### **4B.2 Reducing EOS Current in Hot Bar Process in Manufacturing of Fiber Optics Components 158**

Jeffrey Salisbury, Finisar Corp.; Vladimir Kraz, OnFILTER, Inc.

### **4B.3 Influence of Machine Configuration on EOS Damage during Wafer Cleaning Process 165**

KK Ng, KP Yan, Reinhold Geartner, Stefan Seidl, Infineon Technologies

## **5A: High Voltage II**

Moderator: Yiqun Cao, Infineon Technologies

### **5A.1 Dynamic Aspects to Current Spreading in GGNmosts During Current Ramp-up 170**

Gijs de Raad, NXP Semiconductors

### **5A.2 Impact of Sub-Threshold SOA on ESD Protection Schemes 180**

Krishna Rajagopal, Aravind Appaswamy, Mariano Dissegna, Ann Concannon, Lihui Wang, Antonio Gallerano, Texas Instruments

### **5A.3 ESD Power Clamp with Adjustable Trigger Voltage for RF Power Amplifier Integrated Circuit 190**

Iqbal Chaudhry, Nathaniel Peachey, Qorvo

### **5A.4 Design of ESD Protection for Fault Tolerant Interface Applications with EMC Immunity 197**

S. Parthasarathy, J.A. Salcedo, A. Jeffry, R. Gobbi, J-J. Hajjar, Analog Devices, Inc.

## **5B: EDA Tools**

Moderator: Kai Esmark, Infineon Technologies

### **5B.1 Empirical ESD Simulation Flow for ESD Protection Circuits Based on Snapback Devices 203**

Efraim Aharoni, TOWERJAZZ, Kinneret College on the Sea of Galilee; Avi Parvin, Yosi Vaserman, TOWERJAZZ; Evan Grund, Grund Technical Solutions, Inc.

## **5B.2 An Automated Tool for Chip-Scale ESD Network Exploration and Verification 213**

Benjamin Viale, STMicroelectronics, CNRS-UMR; Mathieu Fer, Lionel Courau, Philippe Galy, Blaise Jacquier, Jérôme Lescot, STMicroelectronics; Bruno Allard, CNRS-UMR

## **5B.3 EDA Approaches in Identifying Latch-up Risks 223**

Michael Khazhinsky, Silicon Labs; Krzysztof Domanski, Harald Gossner; Intel; Guido Quax, Scott Ruth, NXP Semiconductors; Farzan Farbiz, Texas Instruments; Nitesh Trivedi, Infineon

## **5B.4 Spice Modeling Flow for ESD Simulation of CMOS ICs 233**

Gernot Langguth, Adrien Ille, Infineon Technologies AG

# **6A: Advanced CMOS II**

Moderator: Mirko Scholz, imec

## **6A.1 Ultra-Low Standby Current ESD Clamp MOSFET with P/N Hybrid Gate 243**

Katsuhiko Fukasaku, Daisuke Nakagawa, Toshihiko Miyazaki, Takaaki Tatsumi, Hidetoshi Ohnuma, Sony Corporation

## **6A.2 VFTLP Characteristics of ESD Devices in Si Gate-All-Around (GAA) Nanowires 248**

Shih-Hung Chen, Dimitri Linten, Geert Hellings, Anabela Veloso, Mirko Scholz, Nadine Collaert, Naoto Horiguchi, Aaron Thean, imec; Roman Boschke, Guido Groeseneken, imec, KU Leuven

## **6A.3 Gain-Product on pnpn-Structures at High Current Densities and the Impact on the IV-Characteristic 255**

Vadim Valentinovic Vendt, Technical University of Munich, Infineon Technologies AG; Joost Willemen, Infineon Technologies AG; Korbinian Reiser, Technische Universität München, Infineon Technologies AG; Doris Schmitt-Landsiedel, Technical University of Munich

## **6A.4 CDM Protection Design using Internal Power Node for Cross Power Domain in 16nm CMOS Technology 265**

Koki Narita, Mototsugu Okushima, Renesas Electronics Corporation

# **6B: ESD Failure Case Studies**

Moderator: Christian Russ, Intel Corporation

## **6B.1 PMOS Arrays Self-Protection Capability Limitation 273**

Vladislav Vashchenko, Augusto Tazzoli, Maxim Integrated Corp.; Andrei Shibkov, Angstrom Design Automation

## **6B.2 Charged Cable–System ESD Event 283**

Pasi Tamminen, Tampere University of Technology; Toni Viheriäkoski, Cascade Metrology

## **6B.3 Gun Tests of a USB3 Host Controller Board 290**

Guido Notermans, Hans-Martin Ritter, Burkhard Laue, Stefan Seider, NXP Semiconductors

## **7A: On Chip Physics II**

Moderator: Shih-Hung Chen, imec

### **7A.1 Physics of SOA Degradation Phenomena in Power Transistors under ESD Conditions 299**

Jian-Hsing Lee, Natarajan Mahadeva Iyer, Haojun Zhang, Manjunatha Prabhu, Patrick Cao Li, Guowei Zhang, Tsung-Che Tsai, GLOBALFOUNDRIES, Inc.

### **7A.2 Unified Model of 1-D Pulsed Heating, Combining Wunsch-Bell with the Dwyer Curve 308**

Timothy J. Maloney, Intel Corporation

*This paper is co-copyrighted by Intel Corporation.*

### **7A.3 From Quasi-Static to Transient System Level ESD Simulation: Extraction of Turn-on Elements 316**

Fabien Escudié, Fabrice Caignet, Nicolas Nolhier, Marise Bafleur, LAAS-CNRS

## **8A: System Level ESD II**

Moderator: Pasi Tamminen, Researcher, Tampere University of Technology (TUT)

### **8A.1 Mirrored Power Distribution Network Noise Injection for Soft Failure Root Cause Analysis 326**

Suyu Yang, Benjamin Orr, David Pommerenke, Missouri S&T EMC Laboratory; Hideki Shumiya, Junji Maeshima, Taketoshi Sekine, Yuzo Takita, Kenji Araki, Sony EMCS Corporation

### **8A.2 Application Level Investigation of System-Level ESD-Induced Soft Failures 331**

Sandeep Vora, Rui Jiang, Shobha Vasudevan, Elyse Rosenbaum, University of Illinois at Urbana-Champaign

### **8A.3 TLP IV Characterization of a 40 nm CMOS IO Protection Concept in the Powered State 341**

Benjamin Orr, David Pommerenke, Missouri University of Science and Technology; Krzysztof Domanski, Harald Gossner, Intel Corporation

## **Workshops**

Workshops Chair – Guido Notermans, NXP Semiconductors

## **Workshop Session A**

### **A1. Should the Industry Council Address Adequate IEC 61000-4-2 Levels? 347**

*Moderators: David Pommerenke, Missouri University of Science and Technology; Harald Gossner, Intel Corporation*

### **A2. EOS Issues in Automotive Industry – What Information Needs to be Exchanged to Solve the Issue? 348**

*Moderator: Reinhold Gaertner, Infineon Technologies*

### **A3. EDA ESD Verification Tools Utilized in Industry Today. Good, Bad, or Just Plain Ugly? 349**

*Moderators: Robert Gauthier, GLOBALFOUNDRIES, Inc.; Stephen Fairbanks, SRF Technologies, LLC*

## **Workshop Session B**

### **B1. Compliance Verification - TR 53 350**

*Moderators: John Kinnear, IBM; Ron Gibson, Advanced Static Control Consulting*

### **B2. High Pin Count ESD Device Qualification 351**

*Moderator: Wolfgang Stadler, Intel Corporation*

### **B3. Correlation Between Component and System Level ESD Testing 352**

*Moderator: Younes Benlakhoui, NXP Semiconductors*

### **B4. EOS Analysis and Diagnosis - “Techniques and Methods for Dealing with EOS Induced Damage” 353**

*Moderators: Theo Smedes, David Eppes, Michael Stevens, NXP Semiconductors*